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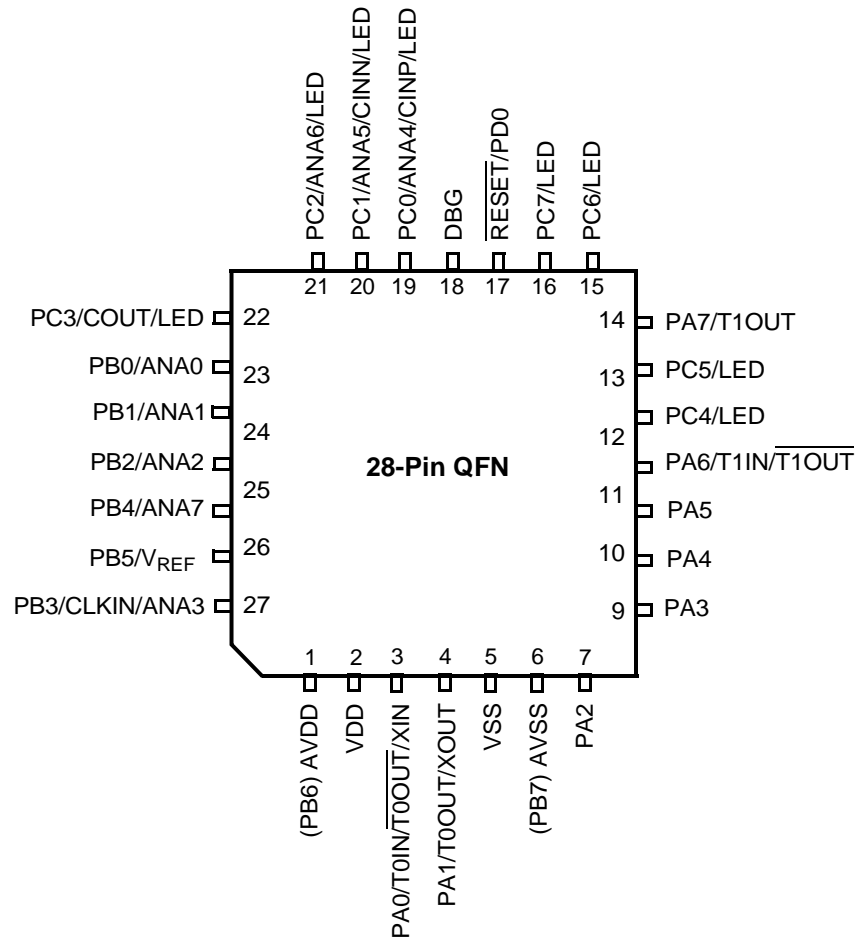
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	25
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0231hj020sg">https://www.e-xfl.com/product-detail/zilog/z8f0231hj020sg</a>

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**Figure 5. Z8F0830 Series in 28-Pin QFN Package**

## Pin Characteristics

Table 5 provides detailed characteristics of each pin available on the Z8 Encore! F0830 Series 20- and 28-pin devices. Data in Table 5 are sorted alphabetically by the pin symbol mnemonic.

**Table 5. Pin Characteristics (20- and 28-pin Devices)**

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-Up or Pull-Down	Schmitt- Trigger Input	Open Drain Output	5V Tolerance
AV <sub>DD</sub>	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
AV <sub>SS</sub>	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA
DBG	I/O	I	N/A	Yes	No	Yes	Yes	Yes
PA[7:0]	I/O	I	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PA[7:2] only
PB[7:0]	I/O	I	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PB[7:6] only
PC[7:0]	I/O	I	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PC[7:3] only
RESET/PD0	I/O	I/O (defaults to RESET)	Low (in RESET mode)	Yes (PD0 only)	Programma- ble for PD0; always on for RESET	Yes	Programma- ble for PD0; always on for RESET	Yes
V <sub>DD</sub>	N/A	N/A	N/A	N/A			N/A	N/A
V <sub>SS</sub>	N/A	N/A	N/A	N/A			N/A	N/A

► **Note:** PB6 and PB7 are available only in devices without an ADC function.

## ***Reset and Stop Mode Recovery***

The reset controller in the Z8 Encore! F0830 Series controls RESET and Stop Mode Recovery operations. In a typical operation, the following events can cause a reset:

- Power-On Reset (POR)
- Voltage Brown-Out (VBO)
- Watchdog Timer time-out (when configured by the WDT\_RES Flash option bit to initiate a reset)
- External  $\overline{\text{RESET}}$  pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-Chip Debugger initiated reset (OCDCTL[0] set to 1)

When the device is in STOP Mode, a Stop Mode Recovery event is initiated by either of the following occurrences:

- A Watchdog Timer time-out
- A GPIO port input pin transition on an enabled Stop Mode Recovery source

The VBO circuitry on the device generates a VBO reset when the supply voltage drops below a minimum safe level.

### **Reset Types**

The Z8 Encore! F0830 Series provides different types of Reset operations. Stop Mode Recovery is considered a form of reset. Table 9 lists the types of resets and their operating characteristics. The duration of a system reset is longer if the external crystal oscillator is enabled by the Flash option bits; the result is additional time for oscillator startup.

## Port A–D Control Registers

The Port A–D Control registers, shown in Table 20, set the GPIO port operation. The value in the corresponding Port A–D Address Register determines which subregister is read from or written to by a Port A–D Control Register transaction.

**Table 20. Port A–D Control Registers (PxCTL)**

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD1H, FD5H, FD9H, FDDH							

Bit	Description
[7:0] PCTL	<b>Port Control</b> The Port Control Register provides access to all subregisters that configure the GPIO port operation.

## Port A–D Data Direction Subregisters

The Port A–D Data Direction Subregister, shown in Table 21, is accessed through the Port A–D Control Register by writing 01H to the Port A–D Address Register.

**Table 21. Port A–D Data Direction Subregisters (PxDD)**

Bit	7	6	5	4	3	2	1	0
Field	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 01H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0] DDx	<b>Data Direction</b> These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction Register setting. 0 = Output. Data in the Port A–D Output Data Register is driven onto the port pin. 1 = Input. The port pin is sampled and the value written into the Port A–D Input Data Register. The output driver is tristated.

Note: x indicates the specific GPIO port pin number (7–0).

**Port A–D Stop Mode Recovery Source Enable Subregisters**

The Port A–D Stop Mode Recovery Source Enable Subregister, shown in Table 25, is accessed through the Port A–D Control Register by writing 05H to the Port A–D Address Register. Setting the bits in the Port A–D Stop Mode Recovery Source Enable subregisters to 1 configures the specified port pins as a Stop Mode Recovery source. During STOP Mode, any logic transition on a port pin enabled as a Stop Mode Recovery source initiates a Stop Mode Recovery event.

**Table 25. Port A–D Stop Mode Recovery Source Enable Subregisters (PxSMRE)**

Bit	7	6	5	4	3	2	1	0
Field	PSMRE7	PSMRE6	PSMRE5	PSMRE4	PSMRE3	PSMRE2	PSMRE1	PSMRE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 05H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0]	<b>Port Stop Mode Recovery Source Enable</b>
PSMREx	0 = The port pin is not configured as a Stop Mode Recovery source. Transitions on this pin during STOP Mode do not initiate Stop Mode Recovery. 1 = The port pin is configured as a Stop Mode Recovery source. Any logic transition on this pin during STOP Mode initiates Stop Mode Recovery.

Note: x indicates the specific GPIO port pin number (7–0).

## Port A–D Output Data Register

The Port A–D Output Data Register, shown in Table 30, controls the output data to the pins.

**Table 30. Port A–D Output Data Register (PxOUT)**

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD3H, FD7H, FDBH, FDFH							

Bit	Description
[7:0]	<b>Port Output Data</b>
PxOUT	These bits contain the data to be driven to the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for Alternate function operation. 0 = Drive a logical 0 (Low). 1 = Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding port output Control Register bit to 1.

Note: x indicates the specific GPIO port pin number (7–0).









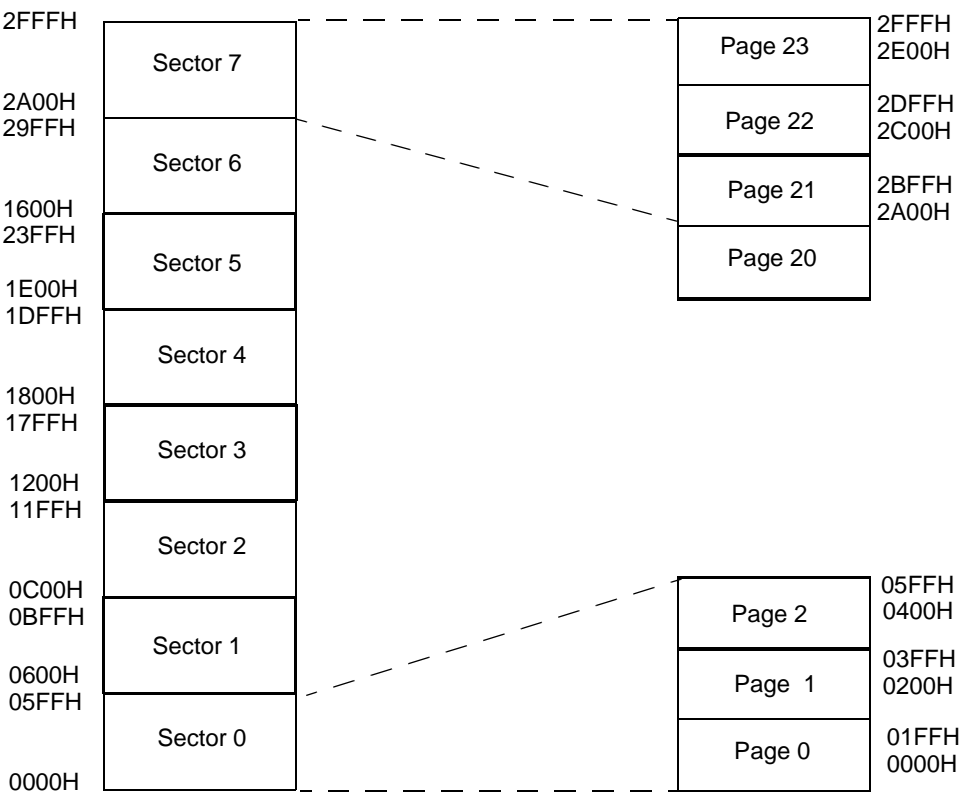


Figure 18. 12K Flash without NVDS

## Data Memory Address Space

The Flash information area, including Zilog Flash option bits, are located in the data memory address space. The Z8 Encore! MCU is configured by these proprietary Flash option bits to prevent the user from writing to the eZ8 CPU data memory address space.

## Flash Information Area

The Flash information area is physically separate from program memory and is mapped to the address range FE00H to FE7FH. Not all of these addresses are user-accessible. Factory trim values for the VBO, Internal Precision Oscillator and factory calibration data for the ADC are stored here.

Table 70 describes the Flash information area. This 128-byte information area is accessed by setting the bit 7 of the Flash Page Select Register to 1. When access is enabled, the

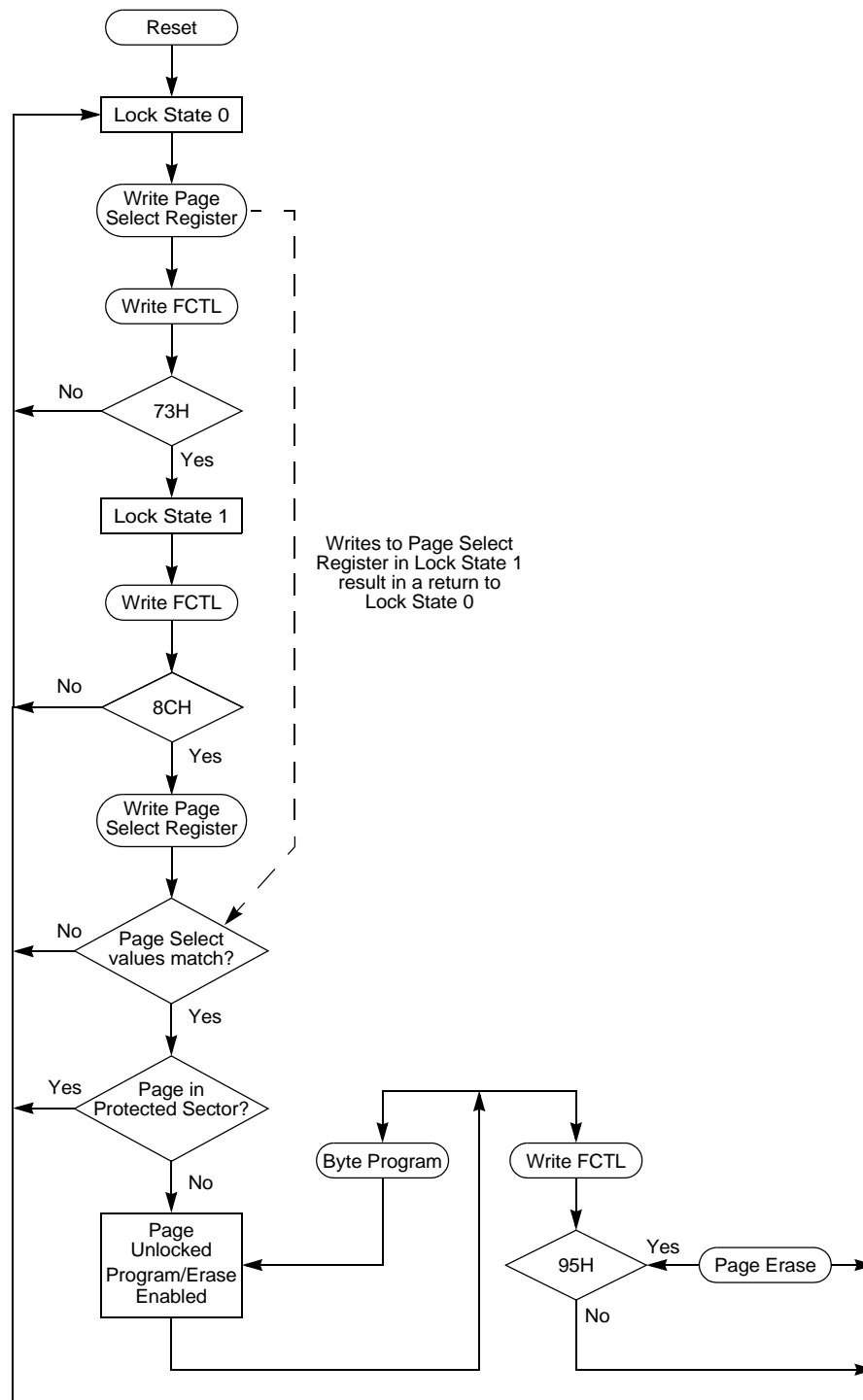


Figure 19. Flash Controller Operation Flow Chart

## Flash Option Bit Control Register Definitions

This section briefly describes the features of the Trim Bit Address and Data registers.

### Trim Bit Address Register

The Trim Bit Address Register, shown in Table 78, contains the target address to access the trim option bits. Trim bit addresses in the range 00h–1Fh map to the information area at addresses 20h–3Fh, as shown in Table 79.

**Table 78. Trim Bit Address Register (TRMADR)**

Bit	7	6	5	4	3	2	1	0
Field	TRMADR: Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF6H							

**Table 79. Trim Bit Address Map**

Trim Bit Address	Information Area Address
00h	20h
01h	21h
02h	22h
03h	23h
:	:
1Fh	3Fh

### Trim Bit Data Register

The Trim Bit Data Register, shown in Table 80, contains the read or write data to access the trim option bits.



The bit values used in Table 85 are set at the factory; no calibration is required.

**Table 86. Trim Option Bits at 0002H (TIPO)**

Bit	7	6	5	4	3	2	1	0
Field	IPO_TRIM							
RESET	U							
R/W	R/W							
Address	Information Page Memory 0022H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:0]	<b>Internal Precision Oscillator Trim Byte</b>
IPO_TRIM	Contains trimming bits for the Internal Precision Oscillator.

The bit values used in Table 86 are set at the factory; no calibration is required.

**Table 87. Trim Option Bits at 0003H (TVBO)**

Bit	7	6	5	4	3	2	1	0
Field	Reserved			Reserved		VBO_TRIM		
RESET	U			U		1	0	0
R/W	R/W			R/W		R/W		
Address	Information Page Memory 0023H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:3]	<b>Reserved</b> These bits are reserved and must be programmed to 11111.
[2]	<b>VBO Trim Values</b>
VBO_TRIM	Contains factory-trimmed values for the oscillator and the VBO.





ory size and is approximately equal to the system clock period multiplied by the number of bytes in program memory.

```
DBG ← 0EH
DBG → CRC[15:8]
DBG → CRC[7:0]
```

**Step Instruction (10H).** The step instruction command, steps one assembly instruction at the current program counter (PC) location. If the device is not in DEBUG Mode or the Flash read protect option bit is enabled, the OCD ignores this command.

```
DBG ← 10H
```

**Stuff Instruction (11H).** The stuff instruction command, steps one assembly instruction and allows specification of the first byte of the instruction. The remaining 0–4 bytes of the instruction are read from program memory. This command is useful for stepping over instructions where the first byte of the instruction has been overwritten by a breakpoint. If the device is not in DEBUG Mode or the Flash read protect option bit is enabled, the OCD ignores this command.

```
DBG ← 11H
DBG ← opcode[7:0]
```

**Execute Instruction (12H).** The execute instruction command allows sending an entire instruction to be executed to the eZ8 CPU. This command can also step over breakpoints. The number of bytes to send for the instruction depends on the opcode. If the device is not in DEBUG Mode or the Flash read protect option bit is enabled, this command reads and discards one byte.

```
DBG ← 12H
DBG ← 1-5 byte opcode
```

## On-Chip Debugger Control Register Definitions

This section describes the features of the On-Chip Debugger Control and Status registers.

### OCD Control Register

The OCD Control Register controls the state of the On-Chip Debugger. This register is used to enter or exit DEBUG Mode and to enable the BRK instruction. It can also reset the Z8 Encore! F0830 Series device.

A reset and stop function can be achieved by writing 81H to this register. A reset and go function can be achieved by writing 41H to this register. If the device is in DEBUG Mode, a run function can be implemented by writing 40H to this register.





**Hex Address: F01**

**Table 131. Timer 0 Low Byte Register (T0L)**

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H							

**Hex Address: F02**

**Table 132. Timer 0 Reload High Byte Register (T0RH)**

Bit	7	6	5	4	3	2	1	0
Field	TRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F02H							

**Hex Address: F03**

**Table 133. Timer 0 Reload Low Byte Register (T0RL)**

Bit	7	6	5	4	3	2	1	0
Field	TRL							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F03H							

**Hex Address: F04**

**Table 134. Timer 0 PWM High Byte Register (T0PWMH)**

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F04H							