

Welcome to **E-XFL.COM** 

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0231ph020sg

# **Table of Contents**

List of Tables       xi         Overview       xi         Features       Part Selection Guide         Block Diagram       20         CPU and Peripheral Overview       30         General Purpose Input/Output       40         Flash Controller       41         Nonvolatile Data Storage       41         Internal Precision Oscillator       51         External Crystal Oscillator       51         External Crystal Oscillator       51         Internal Precision Oscillator       51         Interrupt Controller       51         Analog Comparator       52         Interrupt Controller       52         Reset Controller       60         On-Chip Debugger       60         Acronyms and Expansions       60         Pin Description       60         Available Packages       7         Pin Configurations       7         Signal Descriptions       11         Address Space       12         Register File       14         Program Memory       15         Data Memory       16         Flash Information Area       16         Register Map       17 <t< th=""><th>Revision Historyii</th></t<>	Revision Historyii
Overview Features Part Selection Guide Block Diagram CPU and Peripheral Overview General Purpose Input/Output Flash Controller Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Address Space Register File Program Memory 1 Data Memory Flash Information Area Register Map Reset Types Reset Types 2 Reset Types 2 Reset Types 2 Reset Types 2 Reset Sources 2	List of Figures
Features Part Selection Guide Block Diagram CPU and Peripheral Overview General Purpose Input/Output Flash Controller Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Address Space Register File Program Memory 1 Data Memory Flash Information Area Reset and Stop Mode Recovery Reset Types Reset Types Reset Types Reset Sources 2 Reset Types Reset Sources 2 Reset Sourc	List of Tables
Part Selection Guide         Block Diagram           CPU and Peripheral Overview         General Purpose Input/Output           Flash Controller         4           Nonvolatile Data Storage         Internal Precision Oscillator           External Crystal Oscillator         5           10-Bit Analog-to-Digital Converter         4           Analog Comparator         7           Timers         1           Interrupt Controller         6           Reset Controller         6           On-Chip Debugger         6           Acronyms and Expansions         6           Pin Description         7           Available Packages         7           Pin Configurations         7           Signal Descriptions         1           Pin Characteristics         1           Address Space         1           Register File         14           Program Memory         15           Data Memory         16           Flash Information Area         16           Reset and Stop Mode Recovery         2           Reset Types         2           Reset Sources         2	Overview
Block Diagram CPU and Peripheral Overview General Purpose Input/Output Flash Controller Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Register File Program Memory 1 Data Memory 1 Flash Information Area 1 Register Map Reset Types 2 Reset Types 1 Reset Types 2 Reset Types 2 Reset Types 2 Reset Sources 2 2	Features
CPU and Peripheral Overview General Purpose Input/Output Flash Controller Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions  Pin Description Available Packages Pin Configurations Signal Descriptions Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File Program Memory Data Memory Flash Information Area  Register Map 1 Reset and Stop Mode Recovery Reset Types Reset Types Reset Sources 2 Reset Sources	Part Selection Guide
General Purpose Input/Output       4         Flash Controller       4         Nonvolatile Data Storage       5         Internal Precision Oscillator       5         External Crystal Oscillator       6         10-Bit Analog-to-Digital Converter       6         Analog Comparator       7         Timers       7         Interrupt Controller       6         On-Chip Debugger       6         Acronyms and Expansions       6         Pin Description       7         Available Packages       7         Pin Configurations       7         Signal Descriptions       1         Pin Characteristics       1         Address Space       1         Register File       1         Program Memory       1         Data Memory       1         Flash Information Area       1         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	Block Diagram
Flash Controller       4         Nonvolatile Data Storage       1         Internal Precision Oscillator       2         External Crystal Oscillator       10-Bit Analog-to-Digital Converter         Analog Comparator       2         Timers       3         Interrupt Controller       4         Reset Controller       6         On-Chip Debugger       6         Acronyms and Expansions       6         Pin Description       7         Available Packages       7         Pin Configurations       1         Signal Descriptions       1         Pin Characteristics       1         Address Space       14         Register File       14         Program Memory       15         Data Memory       10         Flash Information Area       16         Register Map       17         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	CPU and Peripheral Overview
Nonvolatile Data Storage       Internal Precision Oscillator         External Crystal Oscillator       20-Bit Analog-to-Digital Converter         Analog Comparator       3-Bit Analog-to-Digital Converter         Analog Comparator       3-Bit Analog-to-Digital Converter         Analog Comparator       3-Bit Analog-to-Digital Converter         Timers       3-Bit Analog-to-Digital Converter         Interrupt Controller       3-Bit Analog-to-Digital Converter         On-Chip Debugger       3-Bit Acronyms and Expansions         Pin Description       3-Bit Analog-to-Digital Converter         Available Packages       3-Bit Analog-to-Digital Converter         Pin Description       3-Bit Analog-to-Digital Converter         Available Packages       3-Bit Analog-to-Digital Converter         Pin Description       3-Bit Analog-to-Digital Converter         Available Packages       3-Bit Analog-to-Digital Converter         Pin Description       3-Bit Analog-to-Digital Converter         Available Packages       3-Bit Analog-to-Digital Converter         Pin Description       3-Bit Analog-to-Digital Converter         Acronyms and Expansions       3-Bit Analog-to-Digital Converter         Acronyms and Expansions       3-Bit Analog-to-Digital Converter         Pin Description       3-Bit Analog-to-Digital Converter	General Purpose Input/Output
Internal Precision Oscillator         External Crystal Oscillator           10-Bit Analog-to-Digital Converter         Analog Comparator           Timers         Interrupt Controller           Reset Controller         On-Chip Debugger           Acronyms and Expansions         On-Chip Debugger           Acronyms and Expansions         On-Chip Debugger           Available Packages         Pin Configurations           Signal Descriptions         1           Pin Characteristics         1           Address Space         1           Register File         14           Program Memory         15           Data Memory         16           Flash Information Area         16           Register Map         17           Reset and Stop Mode Recovery         2           Reset Types         2           Reset Sources         25	Flash Controller
External Crystal Oscillator  10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 11 Pin Characteristics 12 Address Space Register File Program Memory Data Memory Flash Information Area  Register Map Reset and Stop Mode Recovery Reset Types Reset Types Reset Sources 22 Reset Sources 22	Nonvolatile Data Storage
External Crystal Oscillator  10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 11 Pin Characteristics 12 Address Space Register File Program Memory Data Memory Flash Information Area  Register Map Reset and Stop Mode Recovery Reset Types Reset Types Reset Sources 22 Reset Sources 22	Internal Precision Oscillator
10-Bit Analog-to-Digital Converter       Analog Comparator         Timers       State of Controller         Reset Controller       On-Chip Debugger         Acronyms and Expansions       On-Chip Debugger         Pin Description       Available Packages         Pin Configurations       1         Signal Descriptions       1         Pin Characteristics       1         Address Space       1         Register File       1         Program Memory       1         Data Memory       1         Flash Information Area       1         Register Map       1         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	
Analog Comparator       1         Timers       2         Interrupt Controller       3         Reset Controller       4         On-Chip Debugger       5         Acronyms and Expansions       6         Pin Description       7         Available Packages       7         Pin Configurations       1         Signal Descriptions       1         Pin Characteristics       1         Address Space       1         Register File       1         Program Memory       1         Data Memory       1         Flash Information Area       1         Register Map       1         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	
Timers       Interrupt Controller         Reset Controller       6         On-Chip Debugger       6         Acronyms and Expansions       6         Pin Description       7         Available Packages       7         Pin Configurations       1         Signal Descriptions       1         Pin Characteristics       1         Address Space       1         Register File       14         Program Memory       12         Data Memory       16         Flash Information Area       16         Register Map       1         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	
Interrupt Controller       Reset Controller         On-Chip Debugger       On-Chip Debugger         Acronyms and Expansions       On-Chip Debugger         Acronyms and Expansions       On-Chip Debugger         Pin Description       Available Packages         Pin Configurations       1         Signal Descriptions       1         Pin Characteristics       1         Address Space       1         Register File       1         Program Memory       1         Data Memory       1         Flash Information Area       1         Register Map       1         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	
Reset Controller On-Chip Debugger Acronyms and Expansions  Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File Program Memory Data Memory 1 Flash Information Area 1 Register Map 1 Reset and Stop Mode Recovery Reset Types Reset Sources 2 Reset Sources 2 2 Reset Sources 2 2 2 2 2 2 3 3 4 3 4 4 4 7 5 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	
On-Chip Debugger Acronyms and Expansions  Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Address Space 14 Register File 14 Program Memory 15 Data Memory 16 Flash Information Area 16 Register Map 17 Reset and Stop Mode Recovery Reset Types 2 Reset Sources 22	
Acronyms and Expansions       6         Pin Description       7         Available Packages       7         Pin Configurations       1         Signal Descriptions       1         Pin Characteristics       1         Address Space       1         Register File       1         Program Memory       1         Data Memory       1         Flash Information Area       1         Register Map       1         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	
Pin Description Available Packages Pin Configurations Signal Descriptions Pin Characteristics 12 Address Space Register File Program Memory Data Memory Flash Information Area 16 Register Map 17 Reset and Stop Mode Recovery Reset Types Reset Sources 22 Reset Sources 23	
Available Packages Pin Configurations Signal Descriptions Pin Characteristics 1 Address Space Register File Program Memory Data Memory Flash Information Area 1 Register Map 1 Reset and Stop Mode Recovery Reset Types Reset Sources 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	•
Pin Configurations7Signal Descriptions1Pin Characteristics1Address Space14Register File12Program Memory15Data Memory16Flash Information Area16Register Map17Reset and Stop Mode Recovery2Reset Types2Reset Sources2	
Signal Descriptions1Pin Characteristics1Address Space14Register File14Program Memory15Data Memory16Flash Information Area16Register Map17Reset and Stop Mode Recovery2Reset Types2Reset Sources2	<u> </u>
Pin Characteristics15Address Space14Register File14Program Memory15Data Memory16Flash Information Area16Register Map17Reset and Stop Mode Recovery2Reset Types2Reset Sources2	
Address Space       12         Register File       12         Program Memory       15         Data Memory       16         Flash Information Area       16         Register Map       17         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	7
Register File       14         Program Memory       15         Data Memory       16         Flash Information Area       16         Register Map       17         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	Pin Characteristics
Register File       14         Program Memory       15         Data Memory       16         Flash Information Area       16         Register Map       17         Reset and Stop Mode Recovery       2         Reset Types       2         Reset Sources       2	Address Space
Data Memory 10 Flash Information Area 110 Register Map 117 Reset and Stop Mode Recovery 21 Reset Types 22 Reset Sources 22	Register File
Flash Information Area	Program Memory
Flash Information Area	Data Memory
Reset and Stop Mode Recovery	
Reset Types	Register Map
Reset Types	Reset and Stop Mode Recovery
Reset Sources	
	• •

PS025113-1212 Table of Contents

Master Interrupt Enable	55
Interrupt Vectors and Priority	56
Interrupt Assertion	56
Software Interrupt Assertion	57
Interrupt Control Register Definitions	57
Interrupt Request 0 Register	58
Interrupt Request 1 Register	59
Interrupt Request 2 Register	60
IRQ0 Enable High and Low Bit Registers	60
IRQ1 Enable High and Low Bit Registers	62
IRQ2 Enable High and Low Bit Registers	63
Interrupt Edge Select Register	
Shared Interrupt Select Register	
Interrupt Control Register	67
Timers	68
Architecture	68
Operation	69
Timer Operating Modes	69
Reading the Timer Count Values	82
Timer Pin Signal Operation	82
Timer Control Register Definitions	83
Timer 0–1 High and Low Byte Registers	83
Timer Reload High and Low Byte Registers	85
Timer 0–1 PWM High and Low Byte Registers	
Timer 0–1 Control Registers	87
Watchdog Timer	92
Operation	
Watchdog Timer Refresh	93
Watchdog Timer Time-Out Response	93
Watchdog Timer Reload Unlock Sequence	94
Watchdog Timer Control Register Definitions	95
Watchdog Timer Control Register	95
Watchdog Timer Reload Upper, High and Low Byte Registers	96
Analog-to-Digital Converter	98
Architecture	
Operation	
ADC Timing	
ADC Interrupt	
Reference Buffer	
Internal Voltage Reference Generator	101

PS025113-1212 Table of Contents

## Z8 Encore!® F0830 Series Product Specification

vii

Calibration and Compensation	101
ADC Control Register Definitions	101
ADC Control Register 0	102
ADC Data High Byte Register	103
ADC Data Low Bits Register	103
Sample Settling Time Register	104
Sample Time Register	105
Comparator	106
Operation	106
Comparator Control Register Definitions	107
Flash Memory	108
Data Memory Address Space	111
Flash Information Area	111
Operation	112
Flash Operation Timing Using the Flash Frequency Registers	114
Flash Code Protection Against External Access	114
Flash Code Protection Against Accidental Program and Erasure	114
Byte Programming	116
Page Erase	117
Mass Erase	117
Flash Controller Bypass	117
Flash Controller Behavior in Debug Mode	117
NVDS Operational Requirements	118
Flash Control Register Definitions	118
Flash Control Register	119
Flash Status Register	
Flash Page Select Register	121
Flash Sector Protect Register	
Flash Frequency High and Low Byte Registers	
Flash Option Bits	124
Operation	124
Option Bit Configuration by Reset	124
Option Bit Types	
Flash Option Bit Control Register Definitions	
Trim Bit Address Register	
Trim Bit Data Register	
Flash Option Bit Address Space	
Trim Bit Address Space	
Nonvolatile Data Storage	134

PS025113-1212 Table of Contents

# **Block Diagram**

Figure 1 displays a block diagram of the Z8 Encore! F0830 Series architecture.

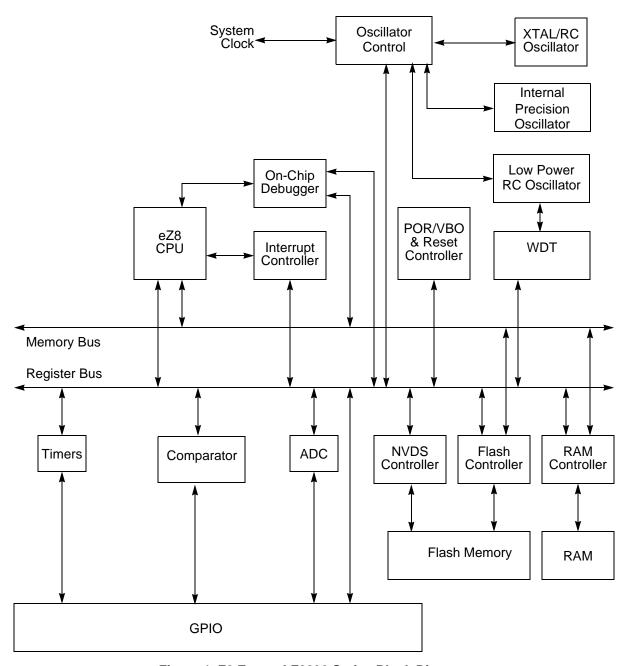


Figure 1. Z8 Encore! F0830 Series Block Diagram

PS025113-1212 Block Diagram

# Pin Description

The Z8 Encore! F0830 Series products are available in a variety of package styles and pin configurations. This chapter describes the signals and the pin configurations for each of the package styles. For information about the physical package specifications, see the <u>Packaging</u> chapter on page 199.

## **Available Packages**

Table 3 lists the package styles that are available for each device in the Z8 Encore! F0830 Series product line.

Part 20-pin 20-pin 28-pin 28-pin 28-pin niq-02 20-pin 28-pin Number **PDIP** ADC **QFN** SOIC **SSOP PDIP** QFN SOIC **SSOP** Z8F1232 Yes Χ Χ Χ Χ Χ Χ Χ Χ Z8F1233 Χ Χ Χ Χ Χ Χ Χ Χ No Z8F0830 Χ Χ Χ Χ Χ Χ Χ Χ Yes Z8F0831 Χ Χ Χ Χ Χ Χ Χ Χ No Χ Χ Χ Χ Χ Z8F0430 Χ Χ Χ Yes Χ Χ Χ Χ Χ Χ Χ Z8F0431 No Χ Z8F0230 Χ Χ Χ Χ Yes Χ Χ Χ Χ Χ Χ Z8F0231 Χ Χ Χ Χ Χ Χ No Z8F0130 Yes Χ Χ Χ Χ Χ Χ Χ Χ Z8F0131 Χ Χ Χ Χ Χ No Χ Χ Χ

Table 3. Z8 Encore! F0830 Series Package Options

# **Pin Configurations**

Figures 2 and 3 display the pin configurations of all of the packages available in the Z8 Encore! F0830 Series. See <u>Table 4</u> on page 11 for a description of the signals. Analog input alternate functions (ANAx) are not available on the following devices:

- Z8F0831
- Z8F0431
- Z8F0131
- Z8F0231
- Z8F1233

PS025113-1212 Pin Description

### **Pin Characteristics**

Table 5 provides detailed characteristics of each pin available on the Z8 Encore! F0830 Series 20- and 28-pin devices. Data in Table 5 are sorted alphabetically by the pin symbol mnemonic.

Table 5. Pin Characteristics (20- and 28-pin Devices)

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-Up or Pull-Down	Schmitt- Trigger Input	Open Drain Output	5V Tolerance
$AV_{DD}$	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
AV <sub>SS</sub>	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA
DBG	I/O	I	N/A	Yes	No	Yes	Yes	Yes
PA[7:0]	I/O	I	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PA[7:2] only
PB[7:0]	I/O	I	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PB[7:6] only
PC[7:0]	I/O	I	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PC[7:3] only
RESET/PD0	I/O	I/O (defaults to RESET)	Low (in RESET mode)	Yes (PD0 only)	Programma- ble for PD0; always on for RESET	Yes	Programma- ble for PD0; always on for RESET	Yes
$V_{DD}$	N/A	N/A	N/A	N/A			N/A	N/A
V <sub>SS</sub>	N/A	N/A	N/A	N/A			N/A	N/A

Note: PB6 and PB7 are available only in devices without an ADC function.

PS025113-1212 Pin Characteristics

**Table 16. Port Alternate Function Mapping (Continued)** 

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C <sup>3</sup>	ort C <sup>3</sup> PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or comparator input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or comparator input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6	ADC analog input	AFS1[2]: 1
PC3	PC3	COUT	Comparator output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1
Port D <sup>1</sup>	PD0	RESET	Default to be Reset function	N/A

#### Notes:

- Because there is only a single alternate function for each Port A and Port D (PD0) pin, the Alternate Function Set registers are not implemented for Port A and Port D (PD0). Enabling alternate function selections (as described in the <u>Port A–D Alternate Function Subregisters</u> section on page 42) automatically enables the associated alternate function.
- 2. Because there are at most two choices of alternate functions for any Port B pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the <a href="Port A-D Alternate Function Subregisters">Port A-D Alternate Function Subregisters</a> section on page 42) must also be enabled.
- 3. Because there are at most two choices of alternate functions for any Port C pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the <a href="Port A-D Alternate Function Subregisters">Port A-D Alternate Function Subregisters</a> section on page 42) must also be enabled.

### **Interrupt Request 2 Register**

The Interrupt Request 2 (IRQ2) Register, shown in Table 37, stores interrupt requests for both vectored and polled interrupts. When a request is sent to the Interrupt Controller, the corresponding bit in the IRQ2 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the Interrupt Controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 Register to determine if any interrupt requests are pending.

Table 37. Interrupt Request 2 Register (IRQ2)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				PC3I	PC2I	PC1I	PC0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC6H							

Bit	Description	
[7:4]	Reserved	
	These registers are reserved and must be programmed to 0000.	
[3]	Port C Pin x Interrupt Request	
PCxI	0 = No interrupt request is pending for GPIO Port C pin x.	
	1 = An interrupt request from GPIO Port C pin $x$ is awaiting service.	
Note:	x indicates the specific GPIO port pin number (3–0).	

### IRQ0 Enable High and Low Bit Registers

Table 38 lists the priority control values for IRQ0. The IRQ0 Enable High and Low Bit registers, shown in Tables 39 and 40, form a priority-encoded enabling service for interrupts in the Interrupt Request 0 Register. Priority is generated by setting the bits in each register.

Table 38. IRQ0 Enable and Priority Encoding

IRQ0ENH[x]	Q0ENH[x] IRQ0ENL[x]		Description				
0	0	Disabled	Disabled				
0	1	Level 1	Low				
1	0	Level 2	Nominal				
1	1	Level 3	High				
Note: <i>x</i> indicates the register bits in the range 7–0.							

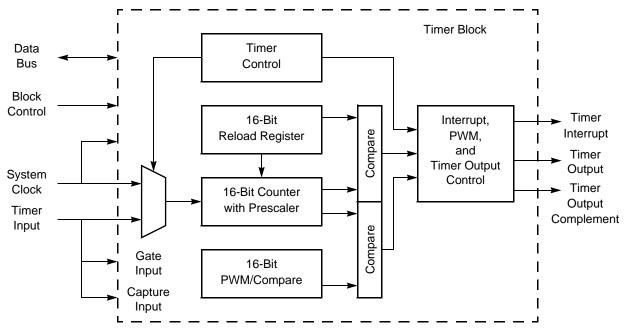


Figure 10. Timer Block Diagram

## **Operation**

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer resets back to 0000H and continues counting.

### **Timer Operating Modes**

The timers can be configured to operate in the following modes:

#### **ONE-SHOT Mode**

In ONE-SHOT Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

Additionally, if the timer output alternate function is enabled, the timer output pin changes state for one system clock cycle (from Low to High or from High to Low) upon timer

PS025113-1212 Operation

reload. For the timer output to make a state change at a ONE-SHOT time-out (rather than a single cycle pulse), first set the TPOL bit in the Timer Control Register to the start value before enabling ONE-SHOT Mode. After starting the timer, set TPOL to the opposite bit value.

Observe the following steps for configuring a timer for ONE-SHOT Mode and for initiating the count:

- 1. Write to the Timer Control Register to:
  - Disable the timer
  - Configure the timer for ONE-SHOT Mode
  - Set the prescale value
  - Set the initial output level (High or Low) if using the timer output Alternate function
- 2. Write to the Timer High and Low Byte registers to set the starting count value.
- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the timer output function, configure the associated GPIO port pin for the timer output alternate function.
- 6. Write to the Timer Control Register to enable the timer and initiate counting.

In ONE-SHOT Mode, the system clock always provides the timer input. The timer period is calculated with the following equation:

$$One-Shot\ Mode\ Time-Out\ Period\ (s)\ =\ \frac{(Reload\ Value-Start\ Value)\times Prescale}{System\ Clock\ Frequency\ (Hz)}$$

#### **CONTINUOUS Mode**

In CONTINUOUS Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and the counting resumes. Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps for configuring a timer for CONTINUOUS Mode and for initiating the count:

1. Write to the Timer Control Register to:

PS025113-1212 Operation

#### **PWM SINGLE OUTPUT Mode**

In PWM SINGLE OUTPUT Mode, the timer outputs a pulse width modulated (PWM) output signal through a GPIO port pin. The timer input is the system clock. The timer first counts up to 16-bit PWM match value stored in the timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the timer output toggles. The timer continues counting until it reaches the reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the timer output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The timer output signal returns to a High (1) after the timer reaches the reload value and is reset to 0001H.

If the TPOL bit in the Timer Control Register is set to 0, the timer output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The timer output signal returns to a Low (0) after the timer reaches the reload value and is reset to 0001H.

Observe the following steps for configuring a timer for PWM SINGLE OUTPUT Mode and for initiating PWM operation:

- 1. Write to the Timer Control Register to:
  - Disable the timer
  - Configure the timer for PWM Mode
  - Set the prescale value
  - Set the initial logic level (High or Low) and PWM High/Low transition for the timer output alternate function
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This value only affects the first pass in PWM Mode. After the first timer reset in PWM Mode, counting always begins at the reset value of 0001H.
- 3. Write to the PWM High and Low Byte registers to set the PWM value.
- 4. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.
- 5. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 6. Configure the associated GPIO port pin for the timer output alternate function.
- 7. Write to the Timer Control Register to enable the timer and initiate counting.

The PWM period is represented by the following equation:

PS025113-1212 Operation

### **Timer Control Register Definitions**

This section defines the features of the following Timer Control registers.

<u>Timer 0–1 High and Low Byte Registers</u>: see page 83

Timer Reload High and Low Byte Registers: see page 85

<u>Timer 0–1 PWM High and Low Byte Registers</u>: see page 86

Timer 0–1 Control Registers: see page 87

### Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers, shown in Tables 50 and 51, contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register content when the timer is enabled; however, when the timer is disabled, a read from the TxL reads the TxL Register content directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations; therefore, simultaneous 16-bit writes are not possible. If either the timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low byte) at the next clock edge. The counter continues counting from the new value.

Table 50. Timer 0–1 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0	
Field		TH							
RESET	0	0	0	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	F00H, F08H								

Table 51. Timer 0–1 Low Byte Register (TxL)

Bit	7	6	5	4	3	2	1	0
Field		TL						
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H, F09H							

### **ADC Data High Byte Register**

The ADC Data High Byte Register, listed in Table 64, contains the upper eight bits of the ADC output. Access to the ADC Data High Byte Register is read-only. Reading the ADC Data High Byte Register latches data in the ADC Low Bits Register.

Table 64. ADC Data High Byte Register (ADCD\_H)

Bit	7	6	5	4	3	2	1	0		
Field	ADCDH									
RESET		X								
R/W	R									
Address		F72H								

Bit	Description
[7:0]	ADC High Byte
ADCDH	00h–FFh = The last conversion output is held in the data registers until the next ADC conver-
	sion is completed.

### **ADC Data Low Bits Register**

The ADC Data Low Bits Register, shown in Table 65, contains the lower bits of the ADC output. Access to the ADC Data Low Bits Register is read-only. Reading the ADC Data High Byte Register latches lower bits of the ADC in the ADC Data Low Bits Register.

Table 65. ADC Data Low Bits Register (ADCD\_L)

Bit	7	6	5	4	3	2	1	0	
Field	ADCDL		Reserved						
RESET	Х		X						
R/W	R		R						
Address			F73H						

Bit	Description
[7:6] ADCDL	ADC Low Bits  00–11b = These bits are the two least-significant bits of the 10-bit ADC output. These bits are undefined after a reset. The low bits are latched into this register whenever the ADC Data High Byte Register is read.
[5:0]	Reserved These bits are reserved and must be programmed to 000000.

# Comparator

The Z8 Encore! F0830 Series devices feature a general purpose comparator that compares two analog input signals. A GPIO (CINP) pin provides the positive comparator input. The negative input (CINN) can be taken from either an external GPIO pin or from an internal reference. The output is available as an interrupt source or can be routed to an external pin using the GPIO multiplex. The comparator includes the following features:

- Positive input is connected to a GPIO pin
- Negative input can be connected to either a GPIO pin or a programmable internal reference
- Output can be either an interrupt source or an output to an external pin

### **Operation**

One of the comparator inputs can be connected to an internal reference that is a user-selectable reference and is user-programmable with 200 mV resolution.

The comparator can be powered down to save supply current. For details, see the <u>Power Control Register 0</u> section on page 31.

**Caution:** As a result of the propagation delay of the comparator, Zilog does not recommend enabling the comparator without first disabling interrupts and waiting for the comparator output to settle. This delay prevents spurious interrupts after comparator enabling.

The following example shows how to safely enable the comparator:

```
di
ld cmp0,r0; load some new configuration
nop
nop ; wait for output to settle
clr irq0 ; clear any spurious interrupts pending
ei
```

PS025113-1212 Comparator

# **Comparator Control Register Definitions**

The Comparator Control Register (CMP0) configures the comparator inputs and sets the value of the internal voltage reference. The GPIO pin is always used as positive comparator input.

Table 68. Comparator Control Register (CMP0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	INNSEL	REFLVL Reserv					erved
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F90H							

Bit	Description
[7]	Reserved This bit is reserved and must be programmed to 0.
[6] INNSEL	Signal Select for Negative Input 0 = internal reference disabled, GPIO pin used as negative comparator input. 1 = internal reference enabled as negative comparator input.
[5:2] REFLVL	Internal Reference Voltage Level This reference is independent of the ADC voltage reference.  0000 = 0.0 V. 0001 = 0.2 V. 0010 = 0.4 V. 0011 = 0.6 V. 0100 = 0.8 V. 0101 = 1.0 V (Default). 0110 = 1.2 V. 0111 = 1.4 V. 1000 = 1.6 V. 1001 = 1.8 V. 1010-1111 = Reserved.
[1:0]	Reserved These bits are reserved and must be programmed to 00.

**Note:** The bit values used in Table 85 are set at the factory; no calibration is required.

### Table 86. Trim Option Bits at 0002H (TIPO)

Bit	7	6	5	4	3	2	1	0
Field		IPO_TRIM						
RESET		U						
R/W		R/W						
Address	Information Page Memory 0022H							
Note: U =	Note: U = Unchanged by Reset. R/W = Read/Write.							

Bit	Description
[7:0]	Internal Precision Oscillator Trim Byte
IPO_TRIM	Contains trimming bits for the Internal Precision Oscillator.

**Note:** The bit values used in Table 86 are set at the factory; no calibration is required.

#### Table 87. Trim Option Bits at 0003H (TVBO)

Bit	7	6	5	4	3	2	1	0
Field		Rese	erved		Reserved	VBO_TRIM		
RESET		l	J		U	1	0	0
R/W		R	W		R/W		R/W	
Address	Information Page Memory 0023H							
Note: U =	Note: U = Unchanged by Reset. R/W = Read/Write.							

Bit	Description
[7:3]	Reserved
	These bits are reserved and must be programmed to 11111.
[2]	VBO Trim Values
VBO_TRIM	Contains factory-trimmed values for the oscillator and the VBO.

Bit	Description (Continued)
[4]	Primary Oscillator Failure Detection Enable
POFEN	1 = Failure detection and recovery of primary oscillator is enabled.
	0 = Failure detection and recovery of primary oscillator is disabled.
[3]	Watchdog Timer Oscillator Failure Detection Enable
WDFEN	1 = Failure detection of Watchdog Timer Oscillator is enabled.
	0 = Failure detection of Watchdog Timer Oscillator is disabled.
[2:0]	System Clock Oscillator Select
SCKSEL	000 = Internal Precision Oscillator functions as system clock at 5.53MHz.
	001 = Internal Precision Oscillator functions as system clock at 32 kHz.
	010 = Crystal oscillator or external RC oscillator functions as system clock.
	011 = Watchdog Timer Oscillator functions as system clock.
	100 = External clock signal on PB3 functions as system clock.
	101 = Reserved.
	110 = Reserved.
	111 = Reserved.

# eZ8 CPU Instruction Set

This chapter describes the following features of the eZ8 CPU instruction set:

Assembly Language Programming Introduction: see page 162

<u>Assembly Language Syntax</u>: see page 163

<u>eZ8 CPU Instruction Notation</u>: see page 164

<u>eZ8 CPU Instruction Classes</u>: see page 166

eZ8 CPU Instruction Summary: see page 171

# **Assembly Language Programming Introduction**

The eZ8 CPU assembly language provides a means for writing an application program without concern for actual memory addresses or machine instruction formats. A program written in assembly language is called a source program. Assembly language allows the use of symbolic addresses to identify memory locations. It also allows mnemonic codes (op codes and operands) to represent the instructions themselves. The op codes identify the instruction while the operands represent memory locations, registers or immediate data values.

Each assembly language program consists of a series of symbolic commands called statements. Each statement contains labels, operations, operands and comments.

Labels can be assigned to a particular instruction step in a source program. The label identifies that step in the program as an entry point for use by other instructions.

The assembly language also includes assembler directives that supplement the machine instruction. The assembler directives, or pseudo-ops, are not translated into a machine instruction. Rather, these pseudo-ops are interpreted as directives that control or assist the assembly process.

The source program is processed (assembled) by the assembler to obtain a machine language program called the object code. The object code is executed by the eZ8 CPU. An example segment of an assembly language program is provided in the following example.

PS025113-1212 eZ8 CPU Instruction Set

Table 128. Z8 Encore! XP F0830 Series Ordering Matrix

				ADC	
Part Number	Flash	RAM	NVDS	Channels	Description
Z8F0430QH020EG	4KB	256	Yes	7	QFN 20-pin
Z8F0431SH020EG	4KB	256	Yes	0	SOIC 20-pin
Z8F0431HH020EG	4KB	256	Yes	0	SSOP 20-pin
Z8F0431PH020EG	4KB	256	Yes	0	PDIP 20-pin
Z8F0431QH020EG	4KB	256	Yes	0	QFN 20-pin
Z8F0430SJ020EG	4KB	256	Yes	8	SOIC 28-pin
Z8F0430HJ020EG	4KB	256	Yes	8	SSOP 28-pin
Z8F0430PJ020EG	4KB	256	Yes	8	PDIP 28-pin
Z8F0430QJ020EG	4KB	256	Yes	8	QFN 28-pin
Z8F0431SJ020EG	4KB	256	Yes	0	SOIC 28-pin
Z8F0431HJ020EG	4KB	256	Yes	0	SSOP 28-pin
Z8F0431PJ020EG	4KB	256	Yes	0	PDIP 28-pin
Z8F0431QJ020EG	4KB	256	Yes	0	QFN 28-pin
Z8 Encore! F0830 with	2KB Flash	1			
Standard Temperature	e: 0°C to 70°	,C			
Z8F0230SH020SG	2KB	256	Yes	7	SOIC 20-pin
Z8F0230HH020SG	2KB	256	Yes	7	SSOP 20-pin
Z8F0230PH020SG	2KB	256	Yes	7	PDIP 20-pin
Z8F0230QH020SG	2KB	256	Yes	7	QFN 20-pin
Z8F0231SH020SG	2KB	256	Yes	0	SOIC 20-pin
Z8F0231HH020SG	2KB	256	Yes	0	SSOP 20-pin
Z8F0231PH020SG	2KB	256	Yes	0	PDIP 20-pin
Z8F0231QH020SG	2KB	256	Yes	0	QFN 20-pin
Z8F0230SJ020SG	2KB	256	Yes	8	SOIC 28-pin
Z8F0230HJ020SG	2KB	256	Yes	8	SSOP 28-pin
Z8F0230PJ020SG	2KB	256	Yes	8	PDIP 28-pin
Z8F0230QJ020SG	2KB	256	Yes	8	QFN 28-pin
Z8F0231SJ020SG	2KB	256	Yes	0	SOIC 28-pin
Z8F0231HJ020SG	2KB	256	Yes	0	SSOP 28-pin
Z8F0231PJ020SG	2KB	256	Yes	0	PDIP 28-pin
Z8F0231QJ020SG	2KB	256	Yes	0	QFN 28-pin

PS025113-1212 Ordering Information

page select register 121, 122	indexed 165
FPS register 121, 122	indirect address prefix 165
FSTAT register 120	indirect register 164
•	indirect register pair 164
	indirect working register 164
G	indirect working register pair 164
gated mode 89	instruction set, ez8 CPU 162
general-purpose I/O 33	instructions
GPIO 4, 33	ADC 166
alternate functions 34	ADCX 166
architecture 34	ADD 166
control register definitions 39	ADDX 166
input data sample timing 195	AND 169
interrupts 39	ANDX 169
port A-C pull-up enable sub-registers 46, 47, 48	arithmetic 166
port A-H address registers 40	BCLR 167
port A-H address registers 40 port A-H alternate function sub-registers 42	BIT 167
port A-H control registers 41	bit manipulation 167
port A-H data direction sub-registers 41	block transfer 167
port A-H high drive enable sub-registers 44	BRK 169
port A-H input data registers 49	BSET 167
port A-H output control sub-registers 43	BSWAP 167, 169
port A-H output data registers 50, 51	BTJ 169
port A-H stop mode recovery sub-registers 45	BTJNZ 166, 169
port availability by device 33	BTJZ 169
port input timing 195	CALL 169
port output timing 196	CCF 167, 168
port output timing 170	CLR 168
	COM 169
Н	CP 166
H 165	CPC 166
HALT 168	CPCX 166
halt mode 31, 168	CPU control 168
hexadecimal number prefix/suffix 165	CPX 166
nexadecimal number prenty/surnx 103	DA 166
	DEC 166
1	DECW 166
IM 164	DI 168
IM 164	DJNZ 169
immediate data 164	EI 168
immediate operand prefix 165	HALT 168
INC 166 increment 166	INC 166
	INCW 167
increment word 167 INCW 167	IRET 169
INCW 10/	