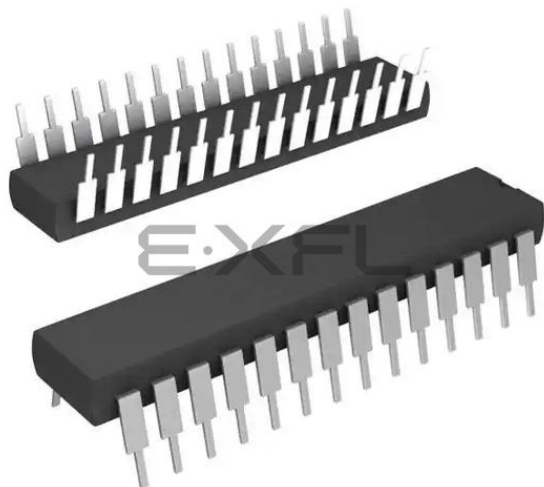




Welcome to E-XFL.COM

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	25
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0231pj020sg

List of Figures

Figure 1.	Z8 Encore! F0830 Series Block Diagram	3
Figure 2.	Z8F0830 Series in 20-Pin SOIC, SSOP, PDIP Package	8
Figure 3.	Z8F0830 Series in 28-Pin SOIC, SSOP, PDIP Package	8
Figure 4.	Z8F0830 Series in 20-Pin QFN Package	9
Figure 5.	Z8F0830 Series in 28-Pin QFN Package	10
Figure 6.	Power-On Reset Operation	24
Figure 7.	Voltage Brown-Out Reset Operation	25
Figure 8.	GPIO Port Pin Block Diagram	34
Figure 9.	Interrupt Controller Block Diagram	55
Figure 10.	Timer Block Diagram	69
Figure 11.	Analog-to-Digital Converter Block Diagram	99
Figure 12.	ADC Timing Diagram	100
Figure 13.	ADC Convert Timing	100
Figure 14.	1K Flash with NVDS	108
Figure 15.	2K Flash with NVDS	109
Figure 16.	4K Flash with NVDS	109
Figure 17.	8K Flash with NVDS	110
Figure 18.	12K Flash without NVDS	111
Figure 19.	Flash Controller Operation Flow Chart	113
Figure 20.	On-Chip Debugger Block Diagram	139
Figure 21.	Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #1 of 2	140
Figure 22.	Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #2 of 2	141
Figure 23.	OCD Data Format	142
Figure 24.	Oscillator Control Clock Switching Flow Chart	156
Figure 25.	Recommended 20MHz Crystal Oscillator Configuration	158
Figure 26.	Connecting the On-Chip Oscillator to an External RC Network	159

Table 119. Flash Memory Electrical Characteristics and Timing	192
Table 120. Watchdog Timer Electrical Characteristics and Timing	192
Table 121. Nonvolatile Data Storage	193
Table 122. Analog-to-Digital Converter Electrical Characteristics and Timing	193
Table 123. Comparator Electrical Characteristics	194
Table 124. GPIO Port Input Timing	195
Table 125. GPIO Port Output Timing	196
Table 126. On-Chip Debugger Timing	197
Table 127. Power Consumption Reference Table	198
Table 128. Z8 Encore! XP F0830 Series Ordering Matrix	200
Table 129. Package and Pin Count Description	207
Table 130. Timer 0 High Byte Register (T0H)	208
Table 131. Timer 0 Low Byte Register (T0L)	209
Table 132. Timer 0 Reload High Byte Register (T0RH)	209
Table 133. Timer 0 Reload Low Byte Register (T0RL)	209
Table 134. Timer 0 PWM High Byte Register (T0PWMH)	209
Table 135. Timer 0 PWM Low Byte Register (T0PWML)	210
Table 136. Timer 0 Control Register 0 (T0CTL0)	210
Table 137. Timer 0 Control Register 1 (T0CTL1)	210
Table 138. Timer 1 High Byte Register (T1H)	210
Table 139. Timer 1 Low Byte Register (T1L)	211
Table 140. Timer 1 Reload High Byte Register (T1RH)	211
Table 141. Timer 1 Reload Low Byte Register (T1RL)	211
Table 142. Timer 1 PWM High Byte Register (T1PWMH)	211
Table 143. Timer 1 PWM Low Byte Register (T1PWML)	212
Table 144. Timer 1 Control Register 0 (T1CTL0)	212
Table 145. Timer 1 Control Register 1 (T1CTL1)	212
Table 146. ADC Control Register 0 (ADCCTL0)	213
Table 147. ADC Data High Byte Register (ADCD_H)	214
Table 148. ADC Data Low Bits Register (ADCD_L)	214

Table 149. ADC Sample Settling Time (ADCSST)	215
Table 150. ADC Sample Time (ADCST)	215
Table 151. Power Control Register 0 (PWRCTL0)	216
Table 152. LED Drive Enable (LEDEN)	216
Table 153. LED Drive Level High Register (LEDLVLH)	217
Table 154. LED Drive Level Low Register (LEDLVLL)	217
Table 155. Oscillator Control Register (OSCCTL)	217
Table 156. Comparator Control Register (CMP0)	218
Table 157. Interrupt Request 0 Register (IRQ0)	218
Table 158. IRQ0 Enable High Bit Register (IRQ0ENH)	219
Table 159. IRQ0 Enable Low Bit Register (IRQ0ENL)	219
Table 160. Interrupt Request 1 Register (IRQ1)	219
Table 161. IRQ1 Enable High Bit Register (IRQ1ENH)	219
Table 162. IRQ1 Enable Low Bit Register (IRQ1ENL)	220
Table 163. Interrupt Request 2 Register (IRQ2)	220
Table 164. IRQ2 Enable High Bit Register (IRQ2ENH)	220
Table 165. IRQ2 Enable Low Bit Register (IRQ2ENL)	220
Table 166. Interrupt Edge Select Register (IRQES)	221
Table 167. Shared Interrupt Select Register (IRQSS)	221
Table 168. Interrupt Control Register (IRQCTL)	221
Table 169. Port A GPIO Address Register (PAADDR)	222
Table 170. Port A Control Registers (PACTL)	222
Table 171. Port A Input Data Registers (PAIN)	222
Table 172. Port A Output Data Register (PAOUT)	223
Table 173. Port B GPIO Address Register (PBADDR)	223
Table 174. Port B Control Registers (PBCTL)	223
Table 175. Port B Input Data Registers (PBIN)	223
Table 176. Port B Output Data Register (PBOUT)	224
Table 177. Port C GPIO Address Register (PCADDR)	224
Table 178. Port C Control Registers (PCCTL)	224

Table 179. Port C Input Data Registers (PCIN)	224
Table 180. Port C Output Data Register (PCOUT)	225
Table 181. Port D GPIO Address Register (PDADDR)	225
Table 182. Port D Control Registers (PDCTL)	225
Table 183. Port D Output Data Register (PDOUT)	226
Table 184. Watchdog Timer Control Register (WDTCTL)	226
Table 185. Reset Status Register (RSTSTAT)	226
Table 186. Watchdog Timer Reload Upper Byte Register (WDTU)	227
Table 187. Watchdog Timer Reload High Byte Register (WDTH)	227
Table 188. Watchdog Timer Reload Low Byte Register (WDTL)	227
Table 189. Trim Bit Address Register (TRMADR)	228
Table 190. Trim Bit Data Register (TRMDR)	228
Table 191. Flash Control Register (FCTL)	228
Table 192. Flash Status Register (FSTAT)	229
Table 193. Flash Page Select Register (FPS)	229
Table 194. Flash Sector Protect Register (FPROT)	229
Table 195. Flash Frequency High Byte Register (FFREQH)	229
Table 196. Flash Frequency Low Byte Register (FFREQL)	230

Block Diagram

Figure 1 displays a block diagram of the Z8 Encore! F0830 Series architecture.

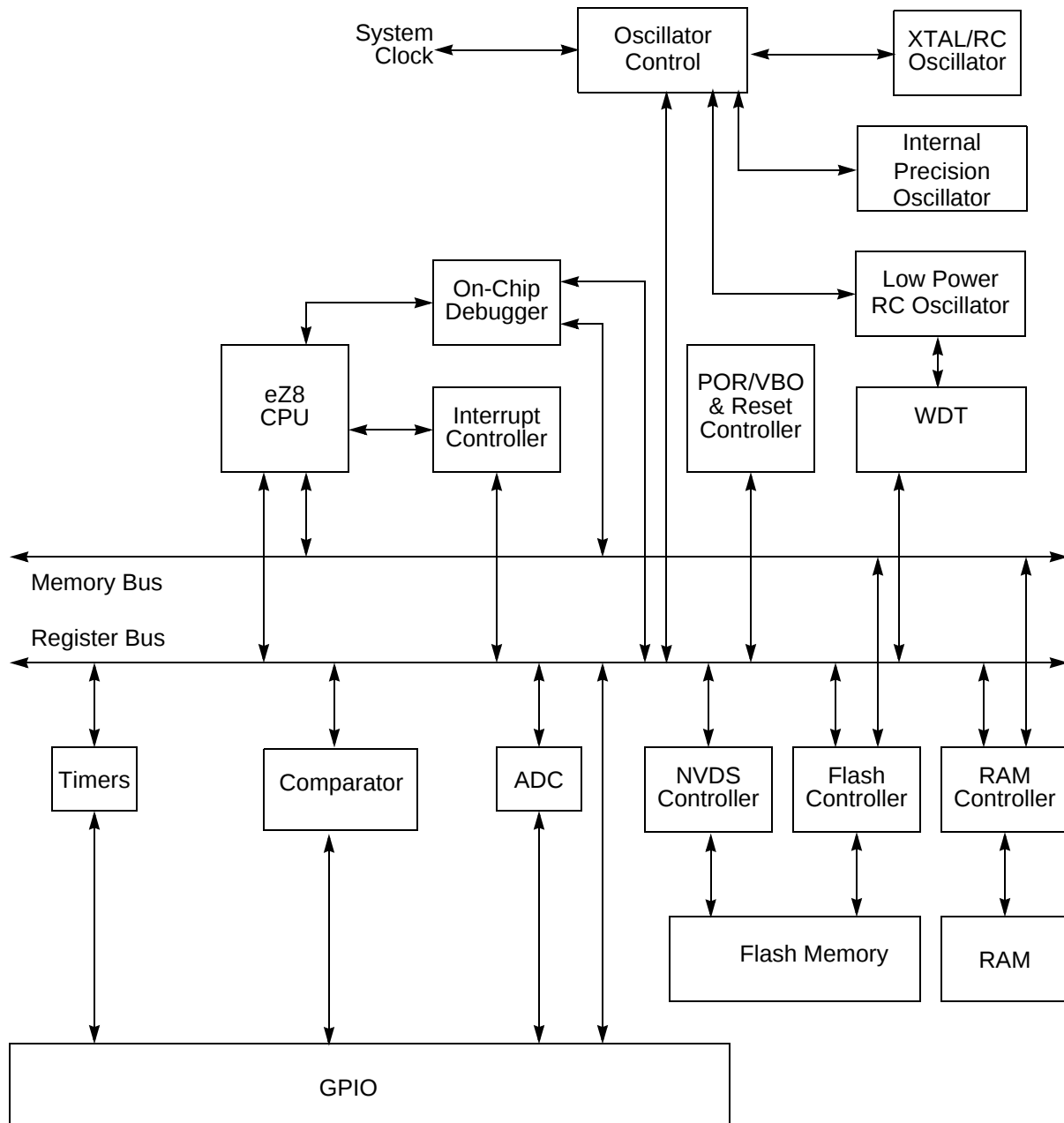


Figure 1. Z8 Encore! F0830 Series Block Diagram

Reset Sources

Table 10 lists the possible sources of a system reset.

Table 10. Reset Sources and Resulting Reset Type

Operating Mode	Reset Source	Special Conditions
NORMAL or HALT modes	Power-On Reset/Voltage Brown-Out	Reset delay begins after supply voltage exceeds POR level.
	Watchdog Timer time-out when configured for reset	None.
	RESET pin assertion	All reset pulses less than four system clocks in width are ignored.
	On-Chip Debugger initiated reset (OCDCTL[0] set to 1)	System, except the On-Chip Debugger is unaffected by the reset.
STOP Mode	Power-On Reset/Voltage Brown-Out	Reset delay begins after supply voltage exceeds POR level.
	RESET pin assertion	All reset pulses less than 12 ns are ignored.
	DBG pin driven Low	None.

Power-On Reset

Each device in the Z8 Encore! F0830 Series contains an internal Power-On Reset circuit. The POR circuit monitors the digital supply voltage and holds the device in the Reset state until the digital supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (V_{POR}), the device is held in the Reset state until the POR counter has timed out. If the crystal oscillator is enabled by the option bits, the time-out is longer.

After the Z8 Encore! F0830 Series device exits the Power-On Reset state, the eZ8 CPU fetches the reset vector. Following the Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1.

Figure 6 displays the Power-On Reset operation. See the [Electrical Characteristics](#) chapter on page 184 for the POR threshold voltage (V_{POR}).

Stop Mode Recovery Using the External $\overline{\text{RESET}}$ Pin

When the Z8 Encore! F0830 Series device is in STOP Mode and the external $\overline{\text{RESET}}$ pin is driven low, a system reset occurs. Because of a glitch filter operating on the $\overline{\text{RESET}}$ pin, the low pulse must be greater than the minimum width specified about 12 ns or it is ignored. The EXT bit in the Reset Status (RSTSTAT) Register is set.

Debug Pin Driven Low

Debug reset is initiated when the On-Chip Debugger detects any of the following error conditions on the DBG pin:

- Serial break (a minimum of nine continuous bits Low)
- Framing error (received STOP bit is Low)
- Transmit collision (simultaneous OCD and host transmission detected by the OCD)

When the Z8F0830 Series device is operating in STOP Mode, the debug reset will cause a system reset. The On-Chip Debugger block is not reset, but the remainder of the chip's operations go through a normal system reset. The POR bit in the Reset Status (RSTSTAT) Register is set to 1.

Reset Register Definitions

The following sections define the Reset registers.

Reset Status Register

The Reset Status (RSTSTAT) Register, shown in Table 12, is a read-only register that indicates the source of the most recent Reset event, Stop Mode Recovery event or Watchdog Timer time-out event. Reading this register resets the upper four bits to 0.

This register shares its address with the Watchdog Timer Control Register, which is write-only.

Table 16. Port Alternate Function Mapping (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C³	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or comparator input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or comparator input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6	ADC analog input	AFS1[2]: 1
	PC3	COUT	Comparator output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1
Port D¹	PD0	RESET	Default to be Reset function	N/A

Notes:

1. Because there is only a single alternate function for each Port A and Port D (PD0) pin, the Alternate Function Set registers are not implemented for Port A and Port D (PD0). Enabling alternate function selections (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) automatically enables the associated alternate function.
2. Because there are at most two choices of alternate functions for any Port B pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) must also be enabled.
3. Because there are at most two choices of alternate functions for any Port C pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) must also be enabled.

Port A–D Alternate Function Set 1 Subregisters

The Port A–D Alternate Function Set 1 Subregister, shown in Table 27, is accessed through the Port A–D Control Register by writing 07H to the Port A–D Address Register. The Alternate Function Set 1 subregisters select the alternate function available at a port pin. Alternate functions selected by setting or clearing bits in this register are defined in the [GPIO Alternate Functions](#) section on page 34.

► **Note:** Alternate function selection on the port pins must also be enabled, as described in the [Port A–D Alternate Function Subregisters](#) section on page 42.

Table 27. Port A–D Alternate Function Set 1 Subregisters (PxAFS1)

Bit	7	6	5	4	3	2	1	0
Field	PAFS17	PAFS16	PAFS15	PAFS14	PAFS13	PAFS12	PAFS11	PAFS10
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 07H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0]	Port Alternate Function Set 1
PAFS1x	0 = Port Alternate function selected as defined in Table 16 in GPIO Alternate Functions section. 1 = Port Alternate function selected as defined in Table 16 in GPIO Alternate Functions section.

Note: x indicates the specific GPIO port pin number (7–0).

Watchdog Timer Control Register Definitions

This section defines the features of the following Watchdog Timer Control registers.

Watchdog Timer Control Register (WDTCTL): see page 95

Watchdog Timer Reload Low Byte Register (WDTL): see page 97

Watchdog Timer Reload Upper Byte Register (WDTU): see page 96

Watchdog Timer Reload High Byte Register (WDTH): see page 96

Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) Register is a write-only control register. Writing the unlock sequence: 55H, AAH to the WDTCTL Register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address have no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the reload registers.

This register address is shared with the read-only Reset Status Register.

Table 59. Watchdog Timer Control Register (WDTCTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTUNLK							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
Address	FF0H							

Bit	Description
[7:0]	Watchdog Timer Unlock
WDTUNLK	The user software must write the correct unlocking sequence to this register before it is allowed to modify the contents of the Watchdog Timer Reload registers.

Flash Frequency High and Low Byte Registers

The Flash Frequency High and Low Byte registers, shown in Tables 76 and 77, combine to form a 16-bit value, FFREQ, to control timing for Flash program and erase operations. The 16-bit binary Flash frequency value must contain the system clock frequency (in kHz) and is calculated using the following equation:

$$\text{FFREQ}[15:0] = \{ \text{FFREQH}[7:0], \text{FFREQL}[7:0] \} = \frac{\text{System Clock Frequency}}{1000}$$

! **Caution:** Flash programming and erasure is not supported for system clock frequencies below 10kHz or above 20MHz. The Flash Frequency High and Low Byte registers must be loaded with the correct value to ensure proper operation of the device.

Table 76. Flash Frequency High Byte Register (FFREQH)

Bit	7	6	5	4	3	2	1	0
Field	FFREQH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FFAH							

Bit	Description
[7:0]	Flash Frequency High Byte
FFREQH	High byte of the 16-bit Flash frequency value.

Table 77. Flash Frequency Low Byte Register (FFREQL)

Bit	7	6	5	4	3	2	1	0
Field	FFREQL							
RESET	0							
R/W	R/W							
Address	FFBH							

Bit	Description
[7:0]	Flash Frequency High Byte
FFREQL	Low byte of the 16-bit Flash frequency value.

Option Bit Types

This section describes the two types of Flash option bits offered in the F0830 Series.

User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits is provided because these locations contain application specific device configurations. The information contained here is lost when page 0 of program memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered by the user. Program memory can be erased without endangering these values. It is possible to alter working values of these bits by accessing the trim bit address and data registers, but these working values are lost after a power loss.

There are 32 bytes of trim data. To modify one of these values, the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data Register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data Register returns the working value of the target trim data byte.

► **Note:** The trim address range is from information address 20–3F only. The remaining information page is not accessible via the Trim Bit Address and Data registers.

During reset, the first 43 system clock cycles perform 43 Flash accesses. The six bits of the counter provide the lower six bits of the Flash memory address. All other address bits are set to 0. The option bit registers use the 6-bit address from the counter as an address and latch the data from the Flash on the positive edge of the IPO clock, allowing for a maximum of 344-bits (43 bytes) of option information to be read from Flash.

Because option information is stored in both the first two bytes of program memory and in the information area of Flash memory, the data must be placed in specific locations to be read correctly. In this case, the first two bytes at addresses 0 and 1 in program memory are read out and the remainder of the bytes are read out of the Flash information area.

Bit	Description (Continued)
[1:0]	Filter Select
FilterSely	2-bit selection for the clock filter mode. 00 = No filter. 01 = Filter low level noise on high level signal. 10 = Filter high level noise on low level signal. 11 = Filter both.
Notes: x indicates bit values 3–1; y indicates bit values 1–0.	

► **Note:** The bit values used in Table 89 are set at factory and no calibration is required.

Table 90. ClkFlt Delay Control Definition

DlyCtl3, DlyCtl2, DlyCtl1	Low Noise Pulse on High Signal (ns)	High Noise Pulse on Low Signal (ns)
000	5	5
001	7	7
010	9	9
011	11	11
100	13	13
101	17	17
110	20	20
111	25	25
Note: The variation is about 30%.		

OCD Status Register

The OCD Status Register reports status information about the current state of the debugger and the system.

Table 97. OCD Status Register (OCDSTAT)

Bit	7	6	5	4	3	2	1	0
Field	DBG	HALT	FRPENB	Reserved				
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R

Bit	Description
[7] DBG	Debug Status 0 = NORMAL Mode. 1 = DEBUG Mode.
[6] HALT	HALT Mode 0 = Not in HALT Mode. 1 = In HALT Mode.
[5] FRPENB	Flash Read Protect Option Bit Enable 0 = FRP bit enabled, that allows disabling of many OCD commands. 1 = FRP bit has no effect.
[4:0]	Reserved These bits are reserved and must be programmed to 00000.

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
AND dst, src	$\text{dst} \leftarrow \text{dst AND src}$	r	r	52	–	*	*	0	–	–	2	3
		r	lr	53							2	4
		R	R	54							3	3
		R	IR	55							3	4
		R	IM	56							3	3
		IR	IM	57							3	4
ANDX dst, src	$\text{dst} \leftarrow \text{dst AND src}$	ER	ER	58	–	*	*	0	–	–	4	3
		ER	IM	59							4	3
ATM	Block all interrupt and DMA requests during execution of the next 3 instructions			2F	–	–	–	–	–	–	1	2
BCLR bit, dst	$\text{dst}[\text{bit}] \leftarrow 0$	r		E2	–	*	*	0	–	–	2	2
BIT p, bit, dst	$\text{dst}[\text{bit}] \leftarrow \text{p}$	r		E2	–	*	*	0	–	–	2	2
BRK	Debugger Break			00	–	–	–	–	–	–	1	1
BSET bit, dst	$\text{dst}[\text{bit}] \leftarrow 1$	r		E2	–	*	*	0	–	–	2	2
BSWAP dst	$\text{dst}[7:0] \leftarrow \text{dst}[0:7]$	R		D5	X	*	*	0	–	–	2	2
BTJ p, bit, src, dst	if $\text{src}[\text{bit}] = \text{p}$ $\text{PC} \leftarrow \text{PC} + \text{X}$		r	F6	–	–	–	–	–	–	3	3
			lr	F7							3	4
BTJNZ bit, src, dst	if $\text{src}[\text{bit}] = 1$ $\text{PC} \leftarrow \text{PC} + \text{X}$		r	F6	–	–	–	–	–	–	3	3
			lr	F7							3	4
BTJZ bit, src, dst	if $\text{src}[\text{bit}] = 0$ $\text{PC} \leftarrow \text{PC} + \text{X}$		r	F6	–	–	–	–	–	–	3	3
			lr	F7							3	4
CALL dst	SP $\leftarrow$ SP – 2 @SP $\leftarrow$ PC PC $\leftarrow$ dst	IRR		D4	–	–	–	–	–	–	2	6
		DA		D6							3	3
CCF	$\text{C} \leftarrow \sim \text{C}$			EF	*	–	–	–	–	–	1	2

Note: Flags Notation:

* = Value is a function of the result of the operation.

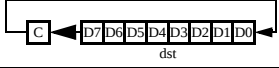
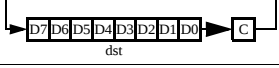
– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
POPX dst	dst ← @SP SP ← SP + 1	ER		D8	–	–	–	–	–	–	3	2
PUSH src	SP ← SP – 1 @SP ← src	R		70	–	–	–	–	–	–	2	2
		IR		71							2	3
		IM		IF70							3	2
PUSHX src	SP ← SP – 1 @SP ← src	ER		C8	–	–	–	–	–	–	3	2
RCF	C ← 0			CF	0	–	–	–	–	–	1	2
RET	PC ← @SP SP ← SP + 2			AF	–	–	–	–	–	–	1	4
RL dst		R		90	*	*	*	*	–	–	2	2
		IR		91							2	3
RLC dst		R		10	*	*	*	*	–	–	2	2
		IR		11							2	3
RR dst		R		E0	*	*	*	*	–	–	2	2
		IR		E1							2	3
RRC dst		R		C0	*	*	*	*	–	–	2	2
		IR		C1							2	3
SBC dst, src	dst ← dst – src – C	r	r	32	*	*	*	*	1	*	2	3
		r	lr	33							2	4
		R	R	34							3	3
		R	IR	35							3	4
		R	IM	36							3	3
		IR	IM	37							3	4
SBCX dst, src	dst ← dst – src – C	ER	ER	38	*	*	*	*	1	*	4	3
		ER	IM	39							4	3
SCF	C ← 1			DF	1	–	–	–	–	–	1	2

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

DC Characteristics

Table 116 lists the DC characteristics of the Z8 Encore! F0830 Series products. All voltages are referenced to V_{SS} , the primary system ground.

Table 116. DC Characteristics

Symbol	Parameter	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
V_{DD}	Supply Voltage				2.7	–	3.6	V	Power supply noise not to exceed 100mV peak to peak
V_{IL1}	Low Level Input Voltage				–0.3	–	$0.3 \cdot V_{DD}$	V	For all input pins except RESET.
V_{IL2}	Low Level Input Voltage				–0.3	–	0.8	V	For RESET.
V_{IH1}	High Level Input Voltage				2.0	–	5.5	V	For all input pins without analog or oscillator function.
V_{IH2}	High Level Input Voltage				2.0	–	$V_{DD} + 0.3$	V	For those pins with analog or oscillator function.
V_{OL1}	Low Level Output Voltage				–	–	0.4	V	$I_{OL} = 2\text{mA}$; $V_{DD} = 3.0\text{V}$ High Output Drive disabled.
V_{OH1}	High Level Output Voltage				2.4	–	–	V	$I_{OH} = -2\text{mA}$; $V_{DD} = 3.0\text{V}$ High Output Drive disabled.
V_{OL2}	Low Level Output Voltage				–	–	0.6	V	$I_{OL} = 20\text{mA}$; $V_{DD} = 3.3\text{V}$ High Output Drive enabled.
V_{OH2}	High Level Output Voltage				2.4	–	–	V	$I_{OH} = -20\text{mA}$; $V_{DD} = 3.3\text{V}$ High Output Drive enabled.
I_{IL}	Input Leakage Current				–5	–	+5	μA	$V_{DD} = 3.6\text{V}$; $V_{IN} = V_{DD}$ or V_{SS} ¹
I_{TL}	Tristate Leakage Current				–5	–	+5	μA	$V_{DD} = 3.6\text{V}$

Notes:

1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.
3. See Figure 31 for HALT Mode current.

Hex Address: F05

Table 135. Timer 0 PWM Low Byte Register (T0PWML)

Bit	7	6	5	4	3	2	1	0
Field	PWML							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F05H							

Hex Address: F06

Table 136. Timer 0 Control Register 0 (T0CTL0)

Bit	7	6	5	4	3	2	1	0
Field	TMODEHI	TICONFIG		Reserved	PWMD			INPCAP
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F06H							

Hex Address: F07

Table 137. Timer 0 Control Register 1 (T0CTL1)

Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F07H							

Hex Address: F08

Table 138. Timer 1 High Byte Register (T1H)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F08H							

Hex Address: F74**Table 149. ADC Sample Settling Time (ADCSST)**

Bit	7	6	5	4	3	2	1	0
Field	Reserved				SST			
RESET	0				1	1	1	1
R/W	R				R/W			
Address	F74H							

Bit	Description
[7:4]	Reserved These bits are reserved and must be programmed to 0000.
[3:0] SST	Sample Settling Time 0h–Fh = Number of system clock periods to meet 0.5 μ s minimum.

Hex Address: F75**Table 150. ADC Sample Time (ADCST)**

Bit	7	6	5	4	3	2	1	0
Field	Reserved		ST					
RESET	0		1	1	1	1	1	1
R/W	R/W		R/W					
Address	F75H							

Bit	Description
[7:6]	Reserved This register is reserved and must be programmed to 0.
[5:0] ST	Sample/Hold Time 0h–Fh = Number of system clock periods to meet 1 μ s minimum.

Hex Addresses: F77–F7F

This address range is reserved.

page select register 121, 122
 FPS register 121, 122
 FSTAT register 120

G

gated mode 89
 general-purpose I/O 33
 GPIO 4, 33
 alternate functions 34
 architecture 34
 control register definitions 39
 input data sample timing 195
 interrupts 39
 port A-C pull-up enable sub-registers 46, 47, 48
 port A-H address registers 40
 port A-H alternate function sub-registers 42
 port A-H control registers 41
 port A-H data direction sub-registers 41
 port A-H high drive enable sub-registers 44
 port A-H input data registers 49
 port A-H output control sub-registers 43
 port A-H output data registers 50, 51
 port A-H stop mode recovery sub-registers 45
 port availability by device 33
 port input timing 195
 port output timing 196

H

H 165
 HALT 168
 halt mode 31, 168
 hexadecimal number prefix/suffix 165

I

IM 164
 immediate data 164
 immediate operand prefix 165
 INC 166
 increment 166
 increment word 167
 INCW 167

indexed 165
 indirect address prefix 165
 indirect register 164
 indirect register pair 164
 indirect working register 164
 indirect working register pair 164
 instruction set, ez8 CPU 162
 instructions
 ADC 166
 ADCX 166
 ADD 166
 ADDX 166
 AND 169
 ANDX 169
 arithmetic 166
 BCLR 167
 BIT 167
 bit manipulation 167
 block transfer 167
 BRK 169
 BSET 167
 BSWAP 167, 169
 BTJ 169
 BTJNZ 166, 169
 BTJZ 169
 CALL 169
 CCF 167, 168
 CLR 168
 COM 169
 CP 166
 CPC 166
 CPCX 166
 CPU control 168
 CPX 166
 DA 166
 DEC 166
 DECW 166
 DI 168
 DJNZ 169
 EI 168
 HALT 168
 INC 166
 INCW 167
 IRET 169