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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0231sh020eg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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General Purpose Input/Output

The Z8 Encore! F0830 Series products support a maximum of 25 port pins (Ports A–D) for General Purpose Input/Output (GPIO) operations. Each port contains control and data registers. The GPIO control registers determine data direction, open-drain, output drive current, programmable pull-ups, Stop Mode Recovery functionality and alternate pin functions. Each port pin is individually programmable. In addition, the Port C pins are capable of direct LED drive at programmable drive strengths.

GPIO Port Availability by Device

Table 15 lists the port pins available with each device and package type.

Devices	Package	10-Bit ADC	Port A	Port B	Port C	Port D	Total I/O
Z8F1232, Z8F0830, Z8F0430, Z8F0230, Z8F0130	20-pin	Yes	[7:0]	[3:0]	[3:0]	[0]	17
Z8F1233, Z8F0831 Z8F0431, Z8F0231 Z8F0131	20-pin	No	[7:0]	[3:0]	[3:0]	[0]	17
Z8F1232, Z8F0830, Z8F0430, Z8F0230, Z8F0130	28-pin	Yes	[7:0]	[5:0]	[7:0]	[0]	23
Z8F1233, Z8F0831 Z8F0431, Z8F0231 Z8F0131	28-pin	No	[7:0]	[7:0]	[7:0]	[0]	25
Note: 20-pin and 28-pin	and 10-bit ADC	Enabled or	r Disabled ca	n be selected	via the optio	n bits.	

Table 15. Port Availability by Device and Package Type

Port A–D Pull-up Enable Subregisters

The Port A–D Pull-Up Enable Subregister is accessed through the Port A–D Control Register by writing 06H to the Port A–D Address Register. See Table 26. Setting the bits in the Port A–D Pull-Up Enable subregisters enables a weak internal resistive pull-up on the specified port pins.

	1	6	5	4	3	2	1	0
Field	PPUE7	PPUE6	PPUE5	PPUE4	PPUE3	PPUE2	PPUE1	PPUE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 06H in Port A–D Address Register, accessible through the Port A–D Control Register							

Table 26. Port A–D Pull-Up Enable Subregisters (PxPUE)

Bit	Description
[7:0]	Port Pull-Up Enable
P <i>x</i> PUE	0 = The weak pull-up on the port pin is disabled.
	1 = The weak pull-up on the port pin is enabled.
Note: x ii	ndicates the specific GPIO port pin number (7–0).

• Writing 1 to the IRQE bit in the Interrupt Control Register

Interrupts are globally disabled by any of the following actions:

- Execution of a DI (disable interrupt) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the Interrupt Controller
- Writing a 0 to the IRQE bit in the Interrupt Control Register
- Reset
- Execution of a trap instruction
- Illegal instruction Trap
- Primary oscillator fail trap
- Watchdog Oscillator fail trap

Interrupt Vectors and Priority

The Interrupt Controller supports three levels of interrupt priority. Level 3 is the highest priority, level 2 is the second highest priority and level 1 is the lowest priority. If all of the interrupts are enabled with identical interrupt priority (all as level 2 interrupts, for example), the interrupt priority is assigned from highest to lowest as specified in <u>Table 34</u> on page 54. Level 3 interrupts are always assigned higher priority than level 2 interrupts and level 2 interrupts are assigned higher priority than level 1 interrupts. Within each interrupt priority level (level 1, level 2 or level 3), priority is assigned as specified in Table 34, above. Reset, Watchdog Timer interrupt (if enabled), primary oscillator fail trap, Watchdog Oscillator fail trap and illegal instruction trap always have highest (level 3) priority.

Interrupt Assertion

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the interrupt request register is cleared. Writing 0 to the corresponding bit in the interrupt request register clears the interrupt request.

Caution: Zilog recommends not using a coding style that clears bits in the Interrupt Request registers. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost. See Example 1, which follows.

Example 1. A poor coding style that can result in lost interrupt requests:

Bit	Description (Continued)
[6] TPOL (cont'd)	 PWM DUAL OUTPUT Mode 0 = Timer output is forced Low (0) and timer output complement is forced High (1), when the timer is disabled. When enabled and the PWM count matches, the timer output is forced High (1) and forced Low (0) when enabled and reloaded. When enabled and the PWM count matches, the timer output complement is forced Low (0) and forced High (1) when enabled and reloaded. 1 = Timer output is forced High (1) and timer output complement is forced Low (0) when the timer is disabled. When enabled and the PWM count matches, the timer output is forced Low (0) when the timer is disabled. When enabled and the PWM count matches, the timer output is forced Low (0) and forced High (1) when enabled and reloaded. When enabled and the PWM count matches, the timer output is forced Low (0) and forced High (1) when enabled and reloaded. When enabled and the PWM count matches, the timer output complement is forced High (1) and forced Low (0) when enabled and reloaded. The PWMD field in the TxCTL0 register determines an optional added delay on the assertion (Low to High) transition of both timer output and timer output complement for deadband generation.
	 CAPTURE RESTART Mode 0 = Count is captured on the rising edge of the timer input signal. 1 = Count is captured on the falling edge of the timer input signal. COMPARATOR COUNTER Mode When the timer is disabled, the timer output signal is set to the value of this bit. When the timer is enabled, the timer output signal is complemented on timer reload.
	Caution: When the timer output alternate function TxOUT on a GPIO port pin is enabled, TxOUT will change to whatever state the TPOL bit is in. The timer does not need to be enabled for that to happen. Additionally, the port data direction sub register is not needed to be set to output on TxOUT. Changing the TPOL bit when the timer is enabled and running does not immediately change the polarity TxOUT.
[5:3] PRES	Prescale Value The timer input clock is divided by 2 ^{PRES} , where PRES can be set from 0 to 7. The prescaler is reset each time the timer is disabled. This reset ensures proper clock division each time the timer is restarted. 000 = Divide by 1. 001 = Divide by 2. 010 = Divide by 4. 011 = Divide by 8. 100 = Divide by 16. 101 = Divide by 32. 110 = Divide by 64. 111 = Divide by 128.

Bit	Description (Continued)
[2:0]	Timer Mode
TMODE	This field along with the TMODEHI bit in TxCTL0 register determines the operating mode of
	the timer. TMODEHI is the most significant bit of the timer mode selection value.
	0000 = ONE-SHOT Mode.
	0001 = CONTINUOUS Mode.
	0010 = COUNTER Mode.
	0011 = PWM SINGLE OUTPUT Mode.
	0100 = CAPTURE Mode.
	0101 = COMPARE Mode.
	0110 = GATED Mode.
	0111 = CAPTURE/COMPARE Mode.
	1000 = PWM DUAL OUTPUT Mode.
	1001 = CAPTURE RESTART Mode.
	1010 = COMPARATOR COUNTER Mode.

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Table 62. Watchdog Timer Reload Low Byte Register (WDTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTL							
RESET	0	0	0	0	0	0	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF3H							
Note: *A r	ead returns th	he current WI	DT count valu	ie; a write set	s the appropr	iate reload va	lue.	
Bit	Descriptio	on						

BR	beenpach
[7:0]	WDT Reload Low
WDTL	Least significant byte (LSB), bits[7:0] of the 24-bit WDT reload value.

Sample Time Register

The Sample Time Register, shown in Table 67, is used to program the length of active time for a sample after a conversion has begun by setting the START bit in the ADC Control Register. The number of system clock cycles required for the sample time varies from system to system, depending on the clock period used. The system designer should program this register to contain the number of system clocks required to meet a $1 \,\mu s$ minimum sample time.

Bit	7	6	5	4	3	2	1	0
Field	Rese	erved	ST					
RESET	()	1	1	1	1	1	1
R/W	R/	W	R/W					
Address			F75H					

Table 67.	Sample	Time	(ADCST)
-----------	--------	------	---------

Bit	Description
[7:6]	Reserved These bits are reserved and must be programmed to 00.
[5:0] ST	0h–Fh = Sample-hold time in number of system clock periods to meet 1 μ s minimum.

bits can only be set to 1. Thus, sectors can be protected, but not unprotected, via register write operations. Writing a value other than 5EH to the Flash Control Register deselects the Flash Sector Protect Register and reenables access to the Page Select Register. Observe the following procedure to setup the Flash Sector Protect Register from user code:

- 1. Write 00H to the Flash Control Register to reset the Flash Controller.
- 2. Write 5EH to the Flash Control Register to select the Flash Sector Protect Register.
- 3. Read and/or write the Flash Sector Protect Register which is now at Register File address FF9H.
- 4. Write 00H to the Flash Control Register to return the Flash Controller to its reset state.

The Sector Protect Register is initialized to 0 on reset, putting each sector into an unprotected state. When a bit in the Sector Protect Register is written to 1, the corresponding sector can no longer be written or erased. After setting a bit in the Sector Protect Register, the bit cannot be cleared by the user.

Byte Programming

Flash memory is enabled for byte programming after unlocking the Flash Controller and successfully enabling either mass erase or page erase. When the Flash Controller is unlocked and mass erase is successfully enabled, all of the program memory locations are available for byte programming. In contrast, when the Flash Controller is unlocked and page erase is successfully enabled, only the locations of the selected page are available for byte programming. An erased Flash byte contains all 1's (FFH). The programming operation can only be used to change bits from 1 to 0. To change a Flash bit (or multiple bits) from 0 to 1 requires execution of either the page erase or mass erase commands.

Byte programming can be accomplished using the On-Chip Debugger's write memory command or eZ8 CPU execution of the LDC or LDCI instructions. Refer to the <u>eZ8 CPU</u> <u>Core User Manual (UM0128)</u>, which is available for download on <u>www.zilog.com</u>, for the description of the LDC and LDCI instructions. While the Flash Controller programs the Flash memory, the eZ8 CPU idles, but the system clock and on-chip peripherals continue to operate. To exit programming mode and lock the Flash, write any value to the Flash Control Register, except the mass erase or page erase commands.

Caution: The byte at each address within Flash memory cannot be programmed (any bits written to 0) more than twice before an erase cycle occurs.

Option Bit Types

This section describes the two types of Flash option bits offered in the F0830 Series.

User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits is provided because these locations contain application specific device configurations. The information contained here is lost when page 0 of program memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered by the user. Program memory can be erased without endangering these values. It is possible to alter working values of these bits by accessing the trim bit address and data registers, but these working values are lost after a power loss.

There are 32 bytes of trim data. To modify one of these values, the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data Register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data Register returns the working value of the target trim data byte.

Note: The trim address range is from information address 20–3F only. The remaining information page is not accessible via the Trim Bit Address and Data registers.

During reset, the first 43 system clock cycles perform 43 Flash accesses. The six bits of the counter provide the lower six bits of the Flash memory address. All other address bits are set to 0. The option bit registers use the 6-bit address from the counter as an address and latch the data from the Flash on the positive edge of the IPO clock, allowing for a maximum of 344-bits (43 bytes) of option information to be read from Flash.

Because option information is stored in both the first two bytes of program memory and in the information area of Flash memory, the data must be placed in specific locations to be read correctly. In this case, the first two bytes at addresses 0 and 1 in program memory are read out and the remainder of the bytes are read out of the Flash information area.

Bit	7	6	5	4	3	2	1	0				
Field	TRMDR: Trim Bit Data											
RESET	0	0	0	0	0	0	0	0				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address	FF7H											

Table 80. Trim Bit Data Register (TRMDR)

Flash Option Bit Address Space

The first two bytes of Flash program memory at addresses 0000H and 0001H are reserved for the user-programmable Flash option bits. See Tables 81 and 82.

Bit	7	6	5	4	3	2	1	0					
Field	WDT_RES	WDT_AO	OSC_S	EL[1:0]	VBO_AO	FRP	Reserved	FWP					
RESET	U	U	U	U	U	U	U	U					
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W					
Address			Р	rogram Mer	nory 0000H								
Note: U =	Note: U = Unchanged by Reset. R/W = Read/Write.												
Bit	Descriptio	on											
[7] WDT_RES	 Watchdog Timer Reset S 0 = Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request. 1 = Watchdog Timer time-out causes a system reset. This is the default setting for unprogrammed (erased) Flash. 												
[6] WDT_AO	 Watchdog Timer Always On 0 = On application of system power, Watchdog Timer is automatically enabled. Watchdog Timer cannot be disabled. 1 = Watchdog Timer is enabled on execution of the WDT instruction. Once enabled, the Watchdog Timer can only be disabled by a reset. This is the default setting for unprogrammed (erased) Elash 												
[5:4] OSC_SEL	 OSCILLATOR Mode Selection 00 = On-chip oscillator configured for use with external RC networks (<4MHz). 01 = Minimum power for use with very low frequency crystals (32 kHz to 1.0MHz). 10 = Medium power for use with medium frequency crystals or ceramic resonators (0.5MHz to 5.0MHz). 11 = Maximum power for use with high frequency crystals (5.0MHz to 20.0MHz). This is the default setting for unprogrammed (erased) Flash. 												

Table 81. Flash Option Bits at Program Memory Address 0000H

Runtime Counter

The OCD contains a 16-bit runtime counter. It counts system clock cycles between breakpoints. The counter starts counting when the OCD leaves DEBUG Mode and stops counting when it enters DEBUG Mode again or when it reaches the maximum count of FFFFH.

On-Chip Debugger Commands

The host communicates to the On-Chip Debugger by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG Mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash read protect option bit (FRP). The FRP prevents the code in memory from being read out of the Z8 Encore! F0830 Series products. When this option is enabled, several of the OCD commands are disabled.

Table 95 summarizes the On-Chip Debugger commands. This table indicates the commands that operate when the device is not in DEBUG Mode (normal operation) and the commands that are disabled by programming the FRP.

Debug Command	Command Byte	Enabled when not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	_
Reserved	01H	_	_
Read OCD Status Register	02H	Yes	_
Read Runtime Counter	03H	_	_
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit
Read OCD Control Register	05H	Yes	_
Write Program Counter	06H	_	Disabled
Read Program Counter	07H	_	Disabled
Write Register	08H	_	Only writes of the Flash Memory Con- trol registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Con- trol register.
Read Register	09H	_	Disabled
Write Program Memory	0AH	_	Disabled
Read Program Memory	0BH	_	Disabled
Write Data Memory	0CH	_	Yes
Read Data Memory	0DH	_	-

Table 95. On-Chip Debugger Command Summary

OCD Status Register

The OCD Status Register reports status information about the current state of the debugger and the system.

Bit	7	6	5	4	3	2	1	0		
Field	DBG	HALT	FRPENB	Reserved						
RESET	0	0	0	0	0	0	0	0		
R/W	R	R	R	R	R	R	R	R		
Bit	Descriptio	n								

Bit	Description
[7] DBG	Debug Status 0 = NORMAL Mode. 1 = DEBUG Mode.
[6] HALT	HALT Mode 0 = Not in HALT Mode. 1 = In HALT Mode.
[5] FRPENB	Flash Read Protect Option Bit Enable 0 = FRP bit enabled, that allows disabling of many OCD commands. 1 = FRP bit has no effect.
[4:0]	Reserved These bits are reserved and must be programmed to 00000.

When selecting a new clock source, the primary oscillator failure detection circuitry and the Watchdog Timer Oscillator failure circuitry must be disabled. If POFEN and WOFEN are not disabled prior to a clock switch-over, it is possible to generate an interrupt for a failure of either oscillator. The failure detection circuitry can be enabled anytime after a successful write of OSCSEL in the Oscillator Control Register.

The Internal Precision Oscillator is enabled by default. If the user code changes to a different oscillator, it may be appropriate to disable the IPO for power savings. Disabling the IPO does not occur automatically.

Clock Failure Detection and Recovery

Primary Oscillator Failure

The Z8F04xA family devices can generate nonmaskable interrupt-like events when the primary oscillator fails. To maintain system function in this situation, the clock failure recovery circuitry automatically forces the Watchdog Timer Oscillator to drive the system clock. The Watchdog Timer Oscillator must be enabled to allow the recovery. Although this oscillator runs at a much slower speed than the original system clock, the CPU continues to operate, allowing execution of a clock failure vector and software routines that either remedy the oscillator failure or issue a failure alert. This automatic switch-over is not available if the Watchdog Timer is the primary oscillator. It is also unavailable if the Watchdog Timer reset function outlined in the Watchdog Timer chapter of this document.

The primary oscillator failure detection circuitry asserts if the system clock frequency drops below 1 KHz \pm 50%. If an external signal is selected as the system oscillator, it is possible that a very slow but nonfailing clock can generate a failure condition. Under these conditions, do not enable the clock failure circuitry (POFEN must be deasserted in the OSCCTL Register).

Watchdog Timer Failure

In the event of failure of a Watchdog Timer Oscillator, a similar nonmaskable interruptlike event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a primary oscillator failure. The failure detection circuitry does not function if the Watchdog Timer is used as the primary oscillator or if the Watchdog Timer Oscillator has been disabled. For either of these cases, it is necessary to disable the detection circuitry by deasserting the WDFEN bit of the OSCCTL Register.

The Watchdog Timer Oscillator failure detection circuit counts system clocks while looking for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which the Watchdog Timer failure is detected. A very slow system clock results in very slow detection times.

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Figure 27. Typical RC Oscillator Frequency as a Function of External Capacitance with a 45 k Ω Resistor

Caution: When using the external RC OSCILLATOR Mode, the oscillator can stop oscillating if the power supply drops below 2.7V but before it drops to the Voltage Brown-Out threshold. The oscillator resumes oscillation when the supply voltage exceeds 2.7V.

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eZ8 CPU Instruction Summary

Table 113 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect upon the Flags register, the number of CPU clock cycles required for the instruction fetch and the number of CPU clock cycles required for the instruction.

Assembly		Address Mode		Op Code(s)	Flags					Fetch	Instr.	
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	Cycles	Cycles
ADC dst, src	$dst \gets dst + src + C$	r	r	12	*	*	*	*	0	*	2	3
		r	lr	13							2	4
		R	R	14	_						3	3
		R	IR	15	_						3	4
		R	IM	16	_						3	3
		IR	IM	17	_						3	4
ADCX dst, src	$dst \gets dst + src + C$	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19	_						4	3
ADD dst, src	$dst \gets dst + src$	r	r	02	*	*	*	*	0	*	2	3
		r	lr	03	_						2	4
		R	R	04	_						3	3
		R	IR	05	_						3	4
		R	IM	06	_						3	3
		IR	IM	07	_						3	4
ADDX dst, src	$dst \gets dst + src$	ER	ER	08	*	*	*	*	0	*	4	3
		ER	IM	09	_						4	3

Table 113. eZ8 CPU Instruction Summary

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

	V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C			V _{DD} T _A = -4	= 2.7 to 40°C to -	3.6V +105°C			
Parameter	Min	Тур	Max	Min	Тур	Max	Units	Notes	
Flash Byte Read Time				50	-	-	ns		
Flash Byte Program Time				20	-	_	μs		
Flash Page Erase Time				50	-	-	ms		
Flash Mass Erase Time				50	-	-	ms		
Writes to Single Address Before Next Erase				-	-	2			
Flash Row Program Time				_	_	8	ms	Cumulative pro- gram time for single row cannot exceed limit before next erase. This parame- ter is only an issue when bypassing the Flash Controller.	
Data Retention				10	_	_	years	25°C	
Endurance				10,000	-	-	cycles	Program/erase cycles	

Table 119. Flash Memory Electrical Characteristics and Timing

Table 120. Watchdog Timer Electrical Characteristics and Timing

		V _{DD} : T _A = 0	= 2.7 to 0°C to -	3.6∨ ⊧70°C	V _{DD} T _A	= 2.7 - = -40°C +105°C	3.6V C to			
Symbol	Parameter	Min	Тур	Max	Min	Тур	Max	Units	Conditions	
	Active power consumption					2	3	μA		
F _{WDT}	WDT oscillator frequency				2.5	5	7.5	kHz		

		V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C		3.6 V ⊦70°C	V _{DD} T _A = -4	= 2.7 to 40°C to	o 3.6V +105°C		
Symbol	Parameter	Min	Тур	Max	Min	Тур	Max	Units	Conditions
Z _{IN}	Input Impedance				10			MΩ	
V _{IN}	Input Voltage Range				0		2.0	V	Internal refer- ence
					0		0.9*VD D		External refer- ence
	Conversion Time				11.9			μs	20MHz (ADC Clock)
	Input Bandwidth					500		KHz	
	Wake Up Time					0.02		ms	Internal refer- ence
						10			External refer- ence
	Input Clock Duty				45	50	55		
	Maximum Input Clock Frequency						20	MHz	
Note: ¹ W	hen the input voltage is	lower that	an 20mV.	the conv	/ersion er	ror is out	t of spec.		

Table 122. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

		V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C			V _{DD} = 2.7 to 3.6V T _A = -40°C to +105°C					
Symbol	Parameter	Min	Тур	Мах	Min	Тур	Мах	Units	Conditions	
V _{OS}	Input DC Offset					5		mV		
V _{CREF}	Programmable Internal Reference Voltage Range				0		1.8	V	User-program- mable in 200 mV step	
V _{CREF}	Programmable internal reference voltage				0.92	1.0	1.08	V	Default (CMP0[REFLVL] =5H)	
T _{PROP}	Propagation delay					100		ns		
V _{HYS}	Input hysteresis					8		mV		

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Analog-to-Digital Converter

For more information about these ADC registers, see the <u>ADC Control Register Defini-</u> tions section on page 101.

Hex Address: F70

Bit	7	6	5	4	3	2	1	0
Field	START	Reserved	REFEN	ADCEN	Reserved	ANAIN[2:0]		
RESET	0	0	0	0	0	0	0	0
R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F70h							

Table 146. ADC Control Register 0 (ADCCTL0)

Bit	Description
[7] START	 ADC Start/Busy 0 = Writing to 0 has no effect; reading a 0 indicates that the ADC is available to begin a conversion. 1 = Writing to 1 starts a conversion; reading a 1 indicates that a conversion is currently in progress.
[6]	This bit is reserved and must be programmed to 0.
[5] REFEN	 Reference Enable 0 = Internal reference voltage is disabled allowing an external reference voltage to be used by the ADC. 1 = Internal reference voltage for the ADC is enabled. The internal reference voltage can be measured on the V_{REF} pin.
[4] ADCEN	ADC Enable 0 = ADC is disabled for low power operation. 1 = ADC is enabled for normal use.
[3]	This bit is reserved and must be programmed to 0.
[2:0] ANAIN	 Analog Input Select 000 = ANA0 input is selected for analog to digital conversion. 001 = ANA1 input is selected for analog to digital conversion. 010 = ANA2 input is selected for analog to digital conversion. 011 = ANA3 input is selected for analog to digital conversion. 100 = ANA4 input is selected for analog to digital conversion. 101 = ANA5 input is selected for analog to digital conversion. 101 = ANA6 input is selected for analog to digital conversion. 111 = ANA7 input is selected for analog to digital conversion.

Hex Addresses: F87–F8F

This address range is reserved.

Comparator 0

For more information about the Comparator Register, see the <u>Comparator Control Register Definitions</u> section on page 107.

Hex Address: F90

Bit	7	6	5	4	3	2	1	0
Field	Reserved	INNSEL	REFLVL				Reserved	
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F90H							

Table 156. Comparator Control Register (CMP0)

Hex Addresses: F91–FBF

This address range is reserved.

Interrupt Controller

For more information about the Interrupt Control registers, see the <u>Interrupt Control Reg-</u> <u>ister Definitions</u> section on page 57.

Hex Address: FC0

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1I	TOI	Reserved	Reserved	Reserved	Reserved	ADCI
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC0H							

Table 157. Interrupt Request 0 Register (IRQ0)