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Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	25
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0231sj020eg

Email: info@E-XFL.COM

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Z8 Encore![®] F0830 Series Product Specification



Figure 4. Z8F0830 Series in 20-Pin QFN Package

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Program Memory

The eZ8 CPU supports 64KB of program memory address space. The Z8 Encore! F0830 Series devices contain 1KB to 12KB of on-chip Flash memory in the program memory address space, depending on the device. Reading from program memory addresses outside the available Flash memory address range returns FFH. Writing to these unimplemented program memory addresses produces no effect. Table 6 shows a program memory map for the Z8 Encore! F0830 Series products.

Program Memory Address (He	ex) Function
Z8F0830 and Z8F0831 Produc	sts
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–003D	Interrupt Vectors*
003E-1FFF	Program Memory
Z8F0430 and Z8F0431 Produc	cts
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–003D	Interrupt Vectors*
003E-0FFF	Program Memory
Z8F0130 and Z8F0131 Produc	cts
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–003D	Interrupt Vectors*
003E-03FF	Program Memory
Z8F0230 and Z8F0231 Produc	cts
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–003D	Interrupt Vectors*
003E-07FF	Program Memory
Note: *See Table 34 on page 54 for	or a list of interrupt vectors.

Table 6. Z8	Encore!	F0830	Series	Program	Memory	Maps
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	Reset Characteristics and Latency					
Reset Type	Control Registers	eZ8 CPU	Reset Latency (Delay)			
System Reset	Reset (as applicable)	Reset	About 66 Internal Precision Oscillator Cycles			
System Reset with Crystal Oscillator Enabled	Reset (as applicable)	Reset	About 5000 Internal Precision Oscillator Cycles			
Stop Mode Recovery	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	About 66 Internal Precision Oscillator cycles			
Stop Mode Recovery with crystal oscillator enabled	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	About 5000 Internal Precision Oscillator cycles			

Table 9. Reset and Stop Mode Recovery Characteristics and Latency

During a system RESET or Stop Mode Recovery, the Z8 Encore! F0830 Series device is held in reset for about 66 cycles of the Internal Precision Oscillator. If the crystal oscillator is enabled in the Flash option bits, the reset period is increased to about 5000 IPO cycles. When a reset occurs because of a low voltage condition or Power-On Reset, the reset delay is measured from the time that the supply voltage first exceeds the POR level (discussed later in this chapter). If the external pin reset remains asserted at the end of the reset period, the device remains in reset until the pin is deasserted.

At the beginning of reset, all GPIO pins are configured as inputs with pull-up resistor disabled, except PD0 which is shared with the reset pin. On reset, the Port D0 pin is configured as a bidirectional open-drain reset. This pin is internally driven low during port reset, after which the user code may reconfigure this pin as a general purpose output.

During reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watchdog Timer Oscillator continues to run.

On reset, control registers within the register file that have a defined reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer and Flags) and general purpose RAM are undefined following the reset. The eZ8 CPU fetches the reset vector at program memory addresses 0002H and 0003H and loads that value into the program counter. Program execution begins at the reset vector address.

Because the control registers are reinitialized by a system reset, the system clock after reset is always the IPO. User software must reconfigure the oscillator control block, to enable and select the correct system clock source.

Port A–D Pull-up Enable Subregisters

The Port A–D Pull-Up Enable Subregister is accessed through the Port A–D Control Register by writing 06H to the Port A–D Address Register. See Table 26. Setting the bits in the Port A–D Pull-Up Enable subregisters enables a weak internal resistive pull-up on the specified port pins.

	1	6	5	4	3	2	1	0
Field	PPUE7	PPUE6	PPUE5	PPUE4	PPUE3	PPUE2	PPUE1	PPUE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 06H in Port A–D Address Register, accessible through the Port A–D Control Register							

Table 26. Port A–D Pull-Up Enable Subregisters (PxPUE)

Bit	Description
[7:0]	Port Pull-Up Enable
P <i>x</i> PUE	0 = The weak pull-up on the port pin is disabled.
	1 = The weak pull-up on the port pin is enabled.
Note: x ii	ndicates the specific GPIO port pin number (7–0).

LED Drive Enable Register

The LED Drive Enable Register, shown in Table 31, activates the controlled current drive. The Alternate Function Register has no control over the LED function; therefore, setting the Alternate Function Register to select the LED function is not required. LEDEN bits [7:0] correspond to Port C bits [7:0], respectively.

Bit	7	6	5	4	3	2	1	0
Field	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F82H							

Table 31	I FD	Drive	Fnable	(I EDEN)
Table JT.		DIIVE		

Bit	Description
[7:0]	LED Drive Enable
LEDEN	These bits determine which Port C pins are connected to an internal current sink. 0 = Tristate the Port C pin.
	1= Connect controlled current sink to the Port C pin.

LED Drive Level High Register

The LED Drive Level High Register, shown in Table 32, contains two control bits for each Port C pin. These two bits select one of four programmable current drive levels for each Port C pin. Each pin is individually programmable.

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address		F83H						

Bit Description

[7:0] LED Level High Bits

LEDLVLH {LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin. 00 = 3mA.

01= 7 mA.

10= 13mA.

11= 20mA.

Watchdog Timer

The Watchdog Timer (WDT) protects from corrupted or unreliable software, power faults and other system-level problems which can place the Z8 Encore! F0830 Series devices into unsuitable operating states. The features of the Watchdog Timer include:

- On-chip RC oscillator
- A selectable time-out response: reset or interrupt
- 24-bit programmable time-out value

Operation

The Watchdog Timer is a retriggerable one-shot timer that resets or interrupts the Z8 Encore! F0830 Series devices when the WDT reaches its terminal count. The WDT uses a dedicated on-chip RC oscillator as its clock source. The WDT operates only in two modes: ON and OFF. Once enabled, it always counts and must be refreshed to prevent a time-out. Perform an enable by executing the WDT instruction or by setting the WDT_AO Flash option bit. The WDT_AO bit forces the WDT to operate immediately on reset, even if a WDT instruction has not been executed.

The Watchdog Timer is a 24-bit reloadable downcounter that uses three 8-bit registers in the eZ8 CPU register space to set the reload value. The nominal WDT time-out period is calculated using the following equation:

WDT Time-out Period (ms) = $\frac{\text{WDT Reload Value}}{10}$

where the WDT reload value is the 24-bit decimal value provided by {WDTU[7:0], WDTH[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10KHz. The Watchdog Timer cannot be refreshed after it reaches 000002H. The WDT reload value must not be set to values below 000004H. Table 58 provides information about approximate time-out delays for the minimum and maximum WDT reload values.

WDT Reload Value	WDT Reload Value	Approxima (with 10KHz Typica	ate Time-Out Delay I WDT Oscillator Frequency)
(Hex)	(Decimal)	Typical	Description
000004	4	400µs	Minimum time-out delay
000400	1024	102ms	Default time-out delay
FFFFF	16,777,215	28 minutes	Maximum time-out delay

Table 58. Watchdog Timer Approximate Time-Out Delays

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Watchdog Timer Control Register Definitions

This section defines the features of the following Watchdog Timer Control registers. Watchdog Timer Control Register (WDTCTL): see page 95

Watchdog Timer Reload Low Byte Register (WDTL): see page 97

Watchdog Timer Reload Upper Byte Register (WDTU): see page 96

Watchdog Timer Reload High Byte Register (WDTH): see page 96

Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) Register is a write-only control register. Writing the unlock sequence: 55H, AAH to the WDTCTL Register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address have no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the reload registers.

This register address is shared with the read-only Reset Status Register.

Bit	7	6	5	4	3	2	1	0	
Field	WDTUNLK								
RESET	Х	Х	Х	Х	Х	Х	Х	Х	
R/W	W	W	W	W	W	W	W	W	
Address	FF0H								
<u> </u>	Derector	· · · ·							

Bit	Description
[7:0]	Watchdog Timer Unlock
WDTUNLK	The user software must write the correct unlocking sequence to this register before it is
	allowed to modify the contents of the Watchdog Timer Reload registers.

Comparator

The Z8 Encore! F0830 Series devices feature a general purpose comparator that compares two analog input signals. A GPIO (CINP) pin provides the positive comparator input. The negative input (CINN) can be taken from either an external GPIO pin or from an internal reference. The output is available as an interrupt source or can be routed to an external pin using the GPIO multiplex. The comparator includes the following features:

- Positive input is connected to a GPIO pin
- Negative input can be connected to either a GPIO pin or a programmable internal reference
- Output can be either an interrupt source or an output to an external pin

Operation

One of the comparator inputs can be connected to an internal reference that is a user-selectable reference and is user-programmable with 200 mV resolution.

The comparator can be powered down to save supply current. For details, see the <u>Power</u> <u>Control Register 0</u> section on page 31.

Caution: As a result of the propagation delay of the comparator, Zilog does not recommend enabling the comparator without first disabling interrupts and waiting for the comparator output to settle. This delay prevents spurious interrupts after comparator enabling.

The following example shows how to safely enable the comparator:

```
di
ld cmp0,r0; load some new configuration
nop
nop ; wait for output to settle
clr irq0; clear any spurious interrupts pending
ei
```

bits can only be set to 1. Thus, sectors can be protected, but not unprotected, via register write operations. Writing a value other than 5EH to the Flash Control Register deselects the Flash Sector Protect Register and reenables access to the Page Select Register. Observe the following procedure to setup the Flash Sector Protect Register from user code:

- 1. Write 00H to the Flash Control Register to reset the Flash Controller.
- 2. Write 5EH to the Flash Control Register to select the Flash Sector Protect Register.
- 3. Read and/or write the Flash Sector Protect Register which is now at Register File address FF9H.
- 4. Write 00H to the Flash Control Register to return the Flash Controller to its reset state.

The Sector Protect Register is initialized to 0 on reset, putting each sector into an unprotected state. When a bit in the Sector Protect Register is written to 1, the corresponding sector can no longer be written or erased. After setting a bit in the Sector Protect Register, the bit cannot be cleared by the user.

Byte Programming

Flash memory is enabled for byte programming after unlocking the Flash Controller and successfully enabling either mass erase or page erase. When the Flash Controller is unlocked and mass erase is successfully enabled, all of the program memory locations are available for byte programming. In contrast, when the Flash Controller is unlocked and page erase is successfully enabled, only the locations of the selected page are available for byte programming. An erased Flash byte contains all 1's (FFH). The programming operation can only be used to change bits from 1 to 0. To change a Flash bit (or multiple bits) from 0 to 1 requires execution of either the page erase or mass erase commands.

Byte programming can be accomplished using the On-Chip Debugger's write memory command or eZ8 CPU execution of the LDC or LDCI instructions. Refer to the <u>eZ8 CPU</u> <u>Core User Manual (UM0128)</u>, which is available for download on <u>www.zilog.com</u>, for the description of the LDC and LDCI instructions. While the Flash Controller programs the Flash memory, the eZ8 CPU idles, but the system clock and on-chip peripherals continue to operate. To exit programming mode and lock the Flash, write any value to the Flash Control Register, except the mass erase or page erase commands.

Caution: The byte at each address within Flash memory cannot be programmed (any bits written to 0) more than twice before an erase cycle occurs.

Flash Option Bits

Programmable Flash option bits allow user configuration of certain aspects of Z8 Encore! F0830 Series operation. The feature configuration data is stored in the Flash program memory and read during reset. The features available for control through the Flash option bits are:

- Watchdog Timer time-out response selection-interrupt or system reset
- Watchdog Timer enabled at reset
- The ability to prevent unwanted read access to user code in program memory
- The ability to prevent accidental programming and erasure of all or a portion of the user code in program memory
- Voltage Brown-Out configuration always enabled or disabled during STOP Mode to reduce STOP Mode power consumption
- OSCILLATOR Mode selection for high, medium and low power crystal oscillators or external RC oscillator
- Factory trimming information for the Internal Precision Oscillator and VBO voltage

Operation

This section describes the type and configuration of the programmable Flash option bits.

Option Bit Configuration by Reset

Each time the Flash option bits are programmed or erased, the device must be reset for the change to be effective. During any Reset operation (system reset or Stop Mode Recovery), the Flash option bits are automatically read from Flash program memory and written to the Option Configuration registers, which control Z8 Encore! F0830 Series device operation. Option bit control is established before the device exits reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the register file and are not accessible for read or write access.

Bit	Description (Continued)					
[1:0]	Filter Select					
FilterSely	2-bit selection for the clock filter mode.					
	00 = No filter.					
	01 = Filter low level noise on high level signal.					
	10 = Filter high level noise on low level signal.					
	11 = Filter both.					
Notes: x ir	Notes: x indicates bit values 3–1; y indicates bit values 1–0.					

Note: The bit values used in Table 89 are set at factory and no calibration is required.

DlyCtl3, DlyCtl2, DlyCtl1	Low Noise Pulse on High Signal (ns)	High Noise Pulse on Low Signal (ns)
000	5	5
001	7	7
010	9	9
011	11	11
100	13	13
101	17	17
110	20	20
111	25	25
Note: The variation is	about 30%.	

Table 90. ClkFlt Delay Control Definition

Byte Read

To read a byte from the NVDS array, user code must first push the address onto the stack. User code issues a CALL instruction to the address of the byte-read routine (0×2000). At the return from the subroutine, the read byte resides in working register R0 and the read status byte resides in working register R1. The bit fields of this status byte are defined in Table 92. Additionally, the user code should pop the address byte off the stack.

The read routine uses 16 bytes of stack space in addition to the one byte of address pushed by the user code. Sufficient memory must be available for this stack usage.

Due to the Flash memory architecture, NVDS reads exhibit a nonuniform execution time. A read operation takes between $71 \mu s$ and $258 \mu s$ (assuming a 20MHz system clock). Slower system clock speeds result in proportionally higher execution times.

NVDS byte reads from invalid addresses (those exceeding the NVDS array size) return $0 \times ff$. Illegal read operations have a $6 \mu s$ execution time.

The status byte returned by the NVDS read routine is zero for a successful read. If the status byte is nonzero, there is a corrupted value in the NVDS array at the location being read. In this case, the value returned in R0 is the byte most recently written to the array that does not have an error.

Bit	7	6	5	4	3	2	1	0			
Field		Reserved		DE	Reserved	FE	IGADDR	Reserved			
Default Value	0	0	0	0	0	0	0	0			
Bit	Description										
[7:5]	Reserved These bits are reserved and must be programmed to 000.										
[4] DE	Data Error When reading an NVDS address, if an error is found in the latest data corresponding to this NVDS address, this bit is set to 1. NVDS source code steps forward until it finds valid data at this address.										
[3]	Reserved This bit is re	eserved and	must be pro	ogrammed t	o 0.						
[2] FE	Flash Erro If a Flash e	r rror is detec	ted, this bit i	s set to 1.							
[1] IGADDR	Illegal Address When NVDS byte reads from invalid addresses (those exceeding the NVDS array size) occur, this bit is set to 1.										
[0]	Reserved This bit is re	eserved and	must be pro	ogrammed t	o 0.						

Table 92. Read Status Byte

Operation

The following section describes the operation of the On-Chip Debugging function.

OCD Interface

The On-Chip Debugger uses the DBG pin for communication with an external host. This one-pin interface is a bidirectional open-drain interface that transmits and receives data. Data transmission is half-duplex, which means that transmission and data retrieval cannot occur simultaneously. The serial data on the DBG pin is sent using the standard asynchronous data format defined in RS-232. This pin creates an interface between the Z8 Encore! F0830 Series products and the serial port of a host PC using minimal external hardware. Two different methods for connecting the DBG pin to an RS-232 interface are displayed in Figures 21 and 22. The recommended method is the buffered implementation depicted in Figure 22. The DBG pin must always be connected to V_{DD} through an external pull-up resistor.

Caution: For proper operation of the On-Chip Debugger, all power pins (V_{DD} and AV_{DD}) must be supplied with power and all ground pins (V_{SS} and AV_{SS}) must be properly grounded. The DBG pin is open-drain and must always be connected to V_{DD} through an external pull-up resistor to ensure proper operation.



Figure 21. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #1 of 2

Caution: It is possible to disable the clock failure detection circuitry as well as all functioning clock sources. In this case, the Z8 Encore! F0830 Series device ceases functioning and can only be recovered by power-on-reset.

Oscillator Control Register Definitions

The following section provides the bit definitions for the Oscillator Control Register.

Oscillator Control Register

The Oscillator Control Register (OSCCTL) enables/disables the various oscillator circuits, enables/disables the failure detection/recovery circuitry and selects the primary oscillator, which becomes the system clock.

The Oscillator Control Register must be unlocked before writing. Writing the two step sequence E7H followed by 18H to the Oscillator Control Register unlocks it. The register is locked at successful completion of a register write to the OSCCTL.

Figure 24 displays the oscillator control clock switching flow. See <u>Table 117</u> on page 189 to review the waiting times of various oscillator circuits.

Bit	7	6	5	4	3	2	1	0	
Field	INTEN	XTLEN	WDTEN	POFEN	WDFEN	SCKSEL			
RESET	1	0	1	0	0	0	0	0	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	F86H								

Table 99.	. Oscillator	Control	Register	(OSCCTL)
-----------	--------------	---------	----------	----------

Bit	Description
[7]	Internal Precision Oscillator Enable
INTEN	1 = Internal Precision Oscillator is enabled.
	0 = Internal Precision Oscillator is disabled.
[6]	Crystal Oscillator Enable
XTLEN	This setting overrides the GPIO register control for PA0 and PA1.
	1 = Crystal oscillator is enabled.
	0 = Crystal oscillator is disabled.
[5]	Watchdog Timer Oscillator Enable
WDTEN	1 = Watchdog Timer Oscillator is enabled.
	0 = Watchdog Timer Oscillator is disabled.

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Figure 27. Typical RC Oscillator Frequency as a Function of External Capacitance with a 45 k Ω Resistor

Caution: When using the external RC OSCILLATOR Mode, the oscillator can stop oscillating if the power supply drops below 2.7V but before it drops to the Voltage Brown-Out threshold. The oscillator resumes oscillation when the supply voltage exceeds 2.7V.

160

4000

170

Table 112. Rotate and Shift Instructions (Continued)

Mnemonic	Operands	Instruction
RR	dst	Rotate Right
RRC	dst	Rotate Right through Carry
SRA	dst	Shift Right Arithmetic
SRL	dst	Shift Right Logical
SWAP	dst	Swap Nibbles

	V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C			V _{DD} = 2.7 to 3.6V T _A = -40°C to +105°C					
Parameter	Min	Тур	Max	Min	Тур	Max	Units	Notes	
Flash Byte Read Time				50	-	-	ns		
Flash Byte Program Time				20	-	_	μs		
Flash Page Erase Time				50	-	-	ms		
Flash Mass Erase Time				50	-	-	ms		
Writes to Single Address Before Next Erase				-	-	2			
Flash Row Program Time				_	_	8	ms	Cumulative pro- gram time for single row cannot exceed limit before next erase. This parame- ter is only an issue when bypassing the Flash Controller.	
Data Retention				10	_	_	years	25°C	
Endurance				10,000	-	-	cycles	Program/erase cycles	

Table 119. Flash Memory Electrical Characteristics and Timing

Table 120. Watchdog Timer Electrical Characteristics and Timing

		$V_{DD} = 2.7 \text{ to } 3.6 \text{V}$ $V_{DD} = 2.7 \text{ to } 3.6 \text{V}$ $T_{A} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $+105^{\circ}\text{C}$								
Symbol	Parameter	Min	Тур	Max	Min	Тур	Max	Units	Conditions	
	Active power consumption					2	3	μA		
F _{WDT}	WDT oscillator frequency				2.5	5	7.5	kHz		

Hex Address: FDB

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDBH							

Hex Address: FDC

Table 181. Port D GPIO Address Register (PDADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDCH							

Hex Address: FDD

Table 182. Port D Control Registers (PDCTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDDH							

Hex Address: FDE

This address range is reserved.

Hex Address: FFB

Table 196. Flash Frequency Low Byte Register (FFREQL)

Bit	7	6	5	4	3	2	1	0
Field	FFREQL							
RESET	0							
R/W	R/W							
Address	FFBH							

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