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Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0430hh020eg

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Block Diagram

Figure 1 displays a block diagram of the Z8 Encore! F0830 Series architecture.

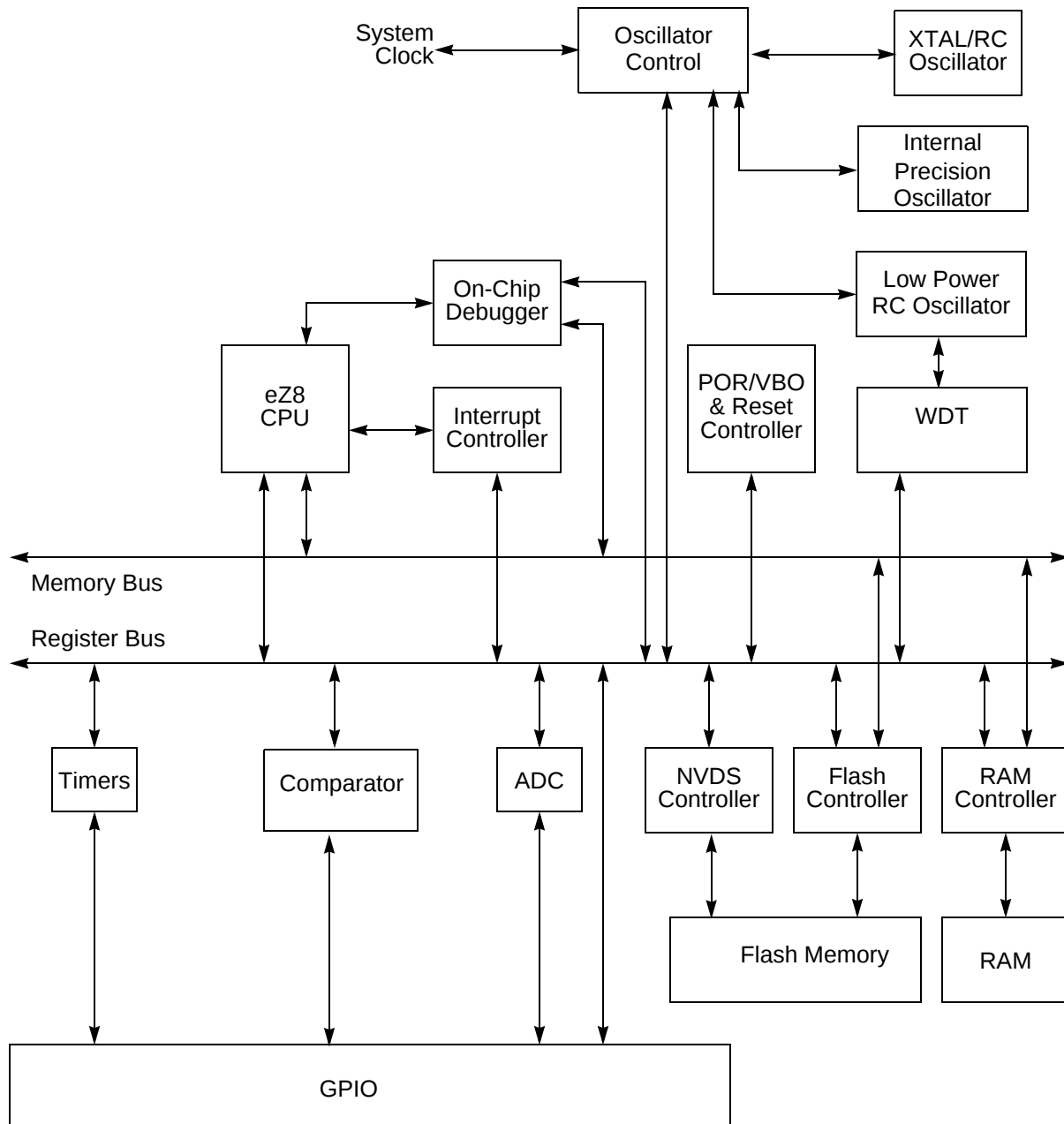


Figure 1. Z8 Encore! F0830 Series Block Diagram

Reset Controller

The Z8 Encore! F0830 Series products are reset using any one of the following: the RESET pin, Power-On Reset, Watchdog Timer (WDT) time-out, STOP Mode exit or Voltage Brown-Out (VBO) warning signal. The RESET pin is bidirectional; i.e., it functions as a reset source as well as a reset indicator.

On-Chip Debugger

The Z8 Encore! F0830 Series products feature an integrated On-Chip Debugger (OCD). The OCD provides a rich set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code. The OCD uses one single-pin interface for communication with an external host.

Acronyms and Expansions

This document references a number of acronyms; each is expanded in Table 2 for the reader's understanding.

Table 2. Acronyms and Expansions

Acronyms	Expansions
ADC	Analog-to-Digital Converter
NVDS	Nonvolatile Data Storage
WDT	Watchdog Timer
GPIO	General-Purpose Input/Output
OCD	On-Chip Debugger
POR	Power-On Reset
VBO	Voltage Brown-Out
IPO	Internal Precision Oscillator
PDIP	Plastic Dual Inline Package
SOIC	Small Outline Integrated Circuit
SSOP	Small Shrink Outline Package
QFN	Quad Flat No Lead
IRQ	Interrupt request
ISR	Interrupt service routine
MSB	Most significant byte
LSB	Least significant byte
PWM	Pulse Width Modulation
SAR	Successive Approximation Regis-

Program Memory

The eZ8 CPU supports 64KB of program memory address space. The Z8 Encore! F0830 Series devices contain 1KB to 12KB of on-chip Flash memory in the program memory address space, depending on the device. Reading from program memory addresses outside the available Flash memory address range returns FFH. Writing to these unimplemented program memory addresses produces no effect. Table 6 shows a program memory map for the Z8 Encore! F0830 Series products.

Table 6. Z8 Encore! F0830 Series Program Memory Maps

Program Memory Address (Hex) Function	
Z8F0830 and Z8F0831 Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–003D	Interrupt Vectors*
003E–1FFF	Program Memory
Z8F0430 and Z8F0431 Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–003D	Interrupt Vectors*
003E–0FFF	Program Memory
Z8F0130 and Z8F0131 Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–003D	Interrupt Vectors*
003E–03FF	Program Memory
Z8F0230 and Z8F0231 Products	
0000–0001	Flash Option Bits
0002–0003	Reset Vector
0004–003D	Interrupt Vectors*
003E–07FF	Program Memory

Note: *See [Table 34](#) on page 54 for a list of interrupt vectors.

Table 43. IRQ1 Enable Low Bit Register (IRQ1ENL)

Bit	7	6	5	4	3	2	1	0
Field	PA7ENL	PA6CENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC5H							

Bit	Description
[7] PA7ENL	Port A Bit[7] Interrupt Request Enable Low Bit
[6] PA6CENL	Port A Bit[7] or Comparator Interrupt Request Enable Low Bit
[5:0] PAxENL	Port A Bit[x] Interrupt Request Enable Low Bit See the interrupt port select register for selection of either Port A or Port D as the interrupt source.

Note: x indicates register bits in the address range 5–0.

IRQ2 Enable High and Low Bit Registers

Table 44 describes the priority control for IRQ2. The IRQ2 Enable High and Low Bit registers, shown in Tables 45 and 46, form a priority-encoded enabling service for interrupts in the Interrupt Request 2 Register. Priority is generated by setting the bits in each register.

Table 44. IRQ2 Enable and Priority Encoding

IRQ2ENH[x]	IRQ2ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

Note: x indicates register bits in the address range 7–0.

Watchdog Timer Control Register Definitions

This section defines the features of the following Watchdog Timer Control registers.

Watchdog Timer Control Register (WDTCTL): see page 95

Watchdog Timer Reload Low Byte Register (WDTL): see page 97

Watchdog Timer Reload Upper Byte Register (WDTU): see page 96

Watchdog Timer Reload High Byte Register (WDTH): see page 96

Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) Register is a write-only control register. Writing the unlock sequence: 55H, AAH to the WDTCTL Register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address have no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the reload registers.

This register address is shared with the read-only Reset Status Register.

Table 59. Watchdog Timer Control Register (WDTCTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTUNLK							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
Address	FF0H							

Bit	Description
[7:0] WDTUNLK	Watchdog Timer Unlock The user software must write the correct unlocking sequence to this register before it is allowed to modify the contents of the Watchdog Timer Reload registers.

Flash Memory

The products in the Z8 Encore! F0830 Series features either 1KB (1024 bytes with NVDS), 2KB (2048 bytes with NVDS), 4KB (4096 bytes with NVDS), 8KB (8192 bytes with NVDS) or 12KB (12288 bytes with no NVDS) of nonvolatile Flash memory with read/write/erase capability. Flash memory can be programmed and erased in-circuit by either user code or through the On-Chip Debugger.

The Flash memory array is arranged in pages with 512 bytes per page. The 512-byte page is the minimum Flash block size that can be erased. Each page is divided into eight rows of 64 bytes.

For program/data protection, Flash memory is also divided into sectors. In the Z8 Encore! F0830 Series, each sector maps to one page (for 1KB, 2KB and 4KB devices), two pages (8KB device) or three pages (12KB device).

The first two bytes of Flash program memory is used as Flash option bits. For more information, see the [Flash Option Bits](#) chapter on page 124.

Table 69 lists the Flash memory configuration for each device in the Z8 Encore! F0830 Series. Figures 14 through 18 display the memory arrangements for each Flash memory size.

Table 69. Z8 Encore! F0830 Series Flash Memory Configuration

Part Number	Flash Size KB (Bytes)	Flash Pages	Program Memory Addresses	Flash Sector Size (bytes)
Z8F123x	12 (12,288)	24	0000H–2FFFH	1536
Z8F083x	8 (8196)	16	0000H–1FFFH	1024
Z8F043x	4 (4096)	8	0000H–0FFFH	512
Z8F023x	2 (2048)	4	0000H–07FFH	512
Z8F013x	1 (1024)	2	0000H–03FFH	512

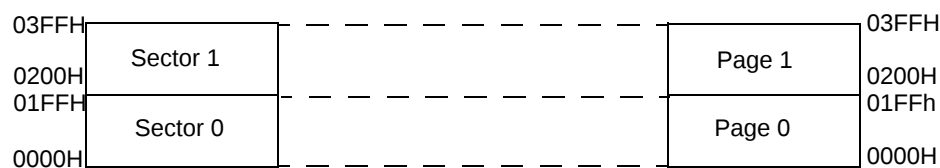


Figure 14. 1K Flash with NVDS

Flash information area is mapped into program memory and overlays the 128 bytes in the address range FE00H to FE7FH. When the information area access is enabled, all reads from these program memory addresses return the information area data rather than the program memory data. Access to the Flash information area is read-only.

The trim bits are handled differently than the other Zilog Flash option bits. The trim bits are the hybrid of the user option bits and the standard Zilog option bits. These trim bits must be user-accessible for reading at all times using external registers regardless of the state of bit 7 in the Flash Page Select Register. Writes to the trim space change the value of the Option Bit Holding Register but do not affect the Flash bits, which remain as read-only.

Table 70. Z8F083 Flash Memory Area Map

Program Memory Address (Hex)	Function
FE00–FE3F	Zilog option bits
FE40–FE53	Part number 20-character ASCII alphanumeric code Left justified and filled with FH
FE54–FE5F	Reserved
FE60–FE7F	Reserved

Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for byte programming, page erase and mass erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

The flowchart in Figure 19 display basic Flash Controller operation. The following subsections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select Page Erase and Mass Erase) displayed in Figure 19.

Bit	Description (Continued)
[4] XTLDIS	State of the Crystal Oscillator at Reset This bit enables only the crystal oscillator. Selecting the crystal oscillator as the system clock must be performed manually. 0 = The crystal oscillator is enabled during reset, resulting in longer reset timing. 1 = The crystal oscillator is disabled during reset, resulting in shorter reset timing.
[3:0]	Reserved These bits are reserved and must be programmed to 1111.

Trim Bit Address Space

All available trim bit addresses and their functions are listed in Tables 83 through 90.

Operation

The following section describes the operation of the On-Chip Debugging function.

OCD Interface

The On-Chip Debugger uses the DBG pin for communication with an external host. This one-pin interface is a bidirectional open-drain interface that transmits and receives data. Data transmission is half-duplex, which means that transmission and data retrieval cannot occur simultaneously. The serial data on the DBG pin is sent using the standard asynchronous data format defined in RS-232. This pin creates an interface between the Z8 Encore! F0830 Series products and the serial port of a host PC using minimal external hardware. Two different methods for connecting the DBG pin to an RS-232 interface are displayed in Figures 21 and 22. The recommended method is the buffered implementation depicted in Figure 22. The DBG pin must always be connected to V_{DD} through an external pull-up resistor.

! Caution: For proper operation of the On-Chip Debugger, all power pins (V_{DD} and AV_{DD}) must be supplied with power and all ground pins (V_{SS} and AV_{SS}) must be properly grounded. The DBG pin is open-drain and must always be connected to V_{DD} through an external pull-up resistor to ensure proper operation.

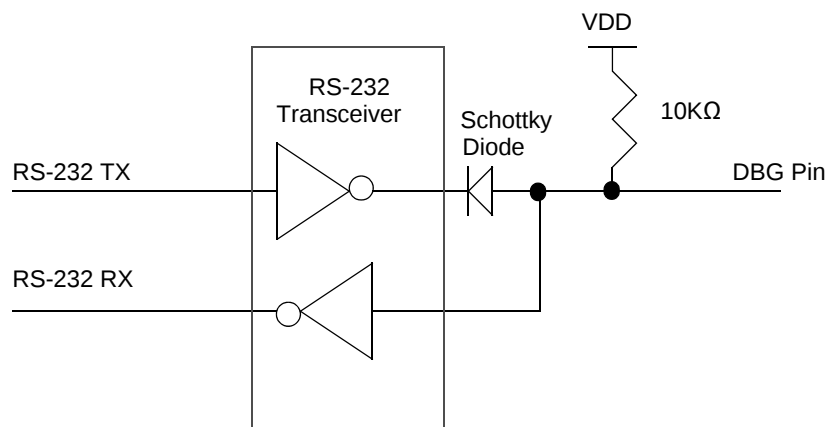


Figure 21. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #1 of 2

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
LDX dst, src	$\text{dst} \leftarrow \text{src}$	r	ER	84	–	–	–	–	–	–	3	2
		lr	ER	85							3	3
		R	IRR	86							3	4
		IR	IRR	87							3	5
		r	X(rr)	88							3	4
		X(rr)	r	89							3	4
		ER	r	94							3	2
		ER	lr	95							3	3
		IRR	R	96							3	4
		IRR	IR	97							3	5
		ER	ER	E8							4	2
		ER	IM	E9							4	2
LEA dst, X(src)	$\text{dst} \leftarrow \text{src} + \text{X}$	r	X(r)	98	–	–	–	–	–	–	3	3
		rr	X(rr)	99							3	5
MULT dst	$\text{dst}[15:0] \leftarrow \text{dst}[15:8] * \text{dst}[7:0]$	RR		F4	–	–	–	–	–	–	2	8
NOP	No operation			0F	–	–	–	–	–	–	1	2
OR dst, src	$\text{dst} \leftarrow \text{dst OR src}$	r	r	42	–	*	*	0	–	–	2	3
		r	lr	43							2	4
		R	R	44							3	3
		R	IR	45							3	4
		R	IM	46							3	3
		IR	IM	47							3	4
ORX dst, src	$\text{dst} \leftarrow \text{dst OR src}$	ER	ER	48	–	*	*	0	–	–	4	3
		ER	IM	49							4	3
POP dst	$\text{dst} \leftarrow @\text{SP}$ $\text{SP} \leftarrow \text{SP} + 1$	R		50	–	–	–	–	–	–	2	2
		IR		51							2	3

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Electrical Characteristics

The data in this chapter represents all known data prior to qualification and characterization of the F0830 Series of products, and is therefore subject to change. Additional electrical characteristics may be found in the individual chapters of this document.

Absolute Maximum Ratings

Stresses greater than those listed in Table 115 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, tie unused inputs to one of the supply voltages (V_{DD} or V_{SS}).

Table 115. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	0	+105	°C	
Storage temperature	−65	+150	°C	
Voltage on any pin with respect to V_{SS}	−0.3	+5.5	V	
Voltage on V_{DD} pin with respect to V_{SS}	−0.3	+3.6	V	
Maximum current on input and/or inactive output pin	−5	+5	μA	
Maximum output current from active output pin	−25	+25	mA	
20-pin Packages Maximum Ratings at 0°C to 70°C				
Total power dissipation		430	mW	
Maximum current into V_{DD} or out of V_{SS}		120	mA	
28-pin Packages Maximum Ratings at 0°C to 70°C				
Total power dissipation		450	mW	
Maximum current into V_{DD} or out of V_{SS}		125	mA	

Table 119. Flash Memory Electrical Characteristics and Timing

Parameter	V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C			V _{DD} = 2.7 to 3.6V T _A = -40°C to +105°C			Units	Notes
	Min	Typ	Max	Min	Typ	Max		
Flash Byte Read Time				50	–	–	ns	
Flash Byte Program Time				20	–	–	µs	
Flash Page Erase Time				50	–	–	ms	
Flash Mass Erase Time				50	–	–	ms	
Writes to Single Address Before Next Erase				–	–	2		
Flash Row Program Time				–	–	8	ms	Cumulative program time for single row cannot exceed limit before next erase. This parameter is only an issue when bypassing the Flash Controller.
Data Retention				10	–	–	years	25°C
Endurance				10,000	–	–	cycles	Program/erase cycles

Table 120. Watchdog Timer Electrical Characteristics and Timing

Symbol	Parameter	V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C			V _{DD} = 2.7 - 3.6V T _A = -40°C to +105°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
	Active power consumption					2	3	µA	
F _{WDT}	WDT oscillator frequency				2.5	5	7.5	kHz	

Table 122. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

Symbol	Parameter	$V_{DD} = 2.7 \text{ to } 3.6\text{V}$ $T_A = 0^\circ\text{C to } +70^\circ\text{C}$			$V_{DD} = 2.7 \text{ to } 3.6\text{V}$ $T_A = -40^\circ\text{C to } +105^\circ\text{C}$			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Z_{IN}	Input Impedance				10			MΩ	
V_{IN}	Input Voltage Range				0		2.0	V	Internal reference
					0		0.9* V_{DD}		External reference
	Conversion Time				11.9			μs	20MHz (ADC Clock)
	Input Bandwidth					500		KHz	
	Wake Up Time					0.02		ms	Internal reference
						10			External reference
	Input Clock Duty				45	50	55		
	Maximum Input Clock Frequency						20	MHz	

Note: ¹When the input voltage is lower than 20mV, the conversion error is out of spec.

Table 123. Comparator Electrical Characteristics

Symbol	Parameter	$V_{DD} = 2.7 \text{ to } 3.6\text{V}$ $T_A = 0^\circ\text{C to } +70^\circ\text{C}$			$V_{DD} = 2.7 \text{ to } 3.6\text{V}$ $T_A = -40^\circ\text{C to } +105^\circ\text{C}$			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
V_{OS}	Input DC Offset					5		mV	
V_{CREF}	Programmable Internal Reference Voltage Range				0		1.8	V	User-programmable in 200 mV step
V_{CREF}	Programmable internal reference voltage				0.92	1.0	1.08	V	Default (CMP0[REFLVL] =5H)
T_{PROP}	Propagation delay					100		ns	
V_{HYS}	Input hysteresis					8		mV	

Table 128. Z8 Encore! XP F0830 Series Ordering Matrix

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8F1233QH020EG	12KB	256	No	0	QFN 20-pin
Z8F1232SJ020EG	12KB	256	No	8	SOIC 28-pin
Z8F1232HJ020EG	12KB	256	No	8	SSOP 28-pin
Z8F1232PJ020EG	12KB	256	No	8	PDIP 28-pin
Z8F1232QJ020EG	12KB	256	No	8	QFN 28-pin
Z8F1233SJ020EG	12KB	256	No	0	SOIC 28-pin
Z8F1233HJ020EG	12KB	256	No	0	SSOP 28-pin
Z8F1233PJ020EG	12KB	256	No	0	PDIP 28-pin
Z8F1233QJ020EG	12KB	256	No	0	QFN 28-pin
Z8 Encore! F0830 with 8KB Flash					
Standard Temperature: 0°C to 70°C					
Z8F0830SH020SG	8KB	256	Yes	7	SOIC 20-pin
Z8F0830HH020SG	8KB	256	Yes	7	SSOP 20-pin
Z8F0830PH020SG	8KB	256	Yes	7	PDIP 20-pin
Z8F0830QH020SG	8KB	256	Yes	7	QFN 20-pin
Z8F0831SH020SG	8KB	256	Yes	0	SOIC 20-pin
Z8F0831HH020SG	8KB	256	Yes	0	SSOP 20-pin
Z8F0831PH020SG	8KB	256	Yes	0	PDIP 20-pin
Z8F0831QH020SG	8KB	256	Yes	0	QFN 20-pin
Z8F0830SJ020SG	8KB	256	Yes	8	SOIC 28-pin
Z8F0830HJ020SG	8KB	256	Yes	8	SSOP 28-pin
Z8F0830PJ020SG	8KB	256	Yes	8	PDIP 28-pin
Z8F0830QJ020SG	8KB	256	Yes	8	QFN 28-pin
Z8F0831SJ020SG	8KB	256	Yes	0	SOIC 28-pin
Z8F0831HJ020SG	8KB	256	Yes	0	SSOP 28-pin
Z8F0831PJ020SG	8KB	256	Yes	0	PDIP 28-pin
Z8F0831QJ020SG	8KB	256	Yes	0	QFN 28-pin
Extended Temperature: -40°C to 105°C					
Z8F0830SH020EG	8KB	256	Yes	7	SOIC 20-pin
Z8F0830HH020EG	8KB	256	Yes	7	SSOP 20-pin
Z8F0830PH020EG	8KB	256	Yes	7	PDIP 20-pin
Z8F0830QH020EG	8KB	256	Yes	7	QFN 20-pin
Z8F0831SH020EG	8KB	256	Yes	0	SOIC 20-pin

Hex Address: FC1

Table 158. IRQ0 Enable High Bit Register (IRQ0ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1ENH	T0ENH	Reserved	Reserved	Reserved	Reserved	ADCENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC1H							

Hex Address: FC2

Table 159. IRQ0 Enable Low Bit Register (IRQ0ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1ENL	T0ENL	Reserved	Reserved	Reserved	Reserved	ADCENL
RESET	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R	R	R/W
Address	FC2H							

Hex Address: FC3

Table 160. Interrupt Request 1 Register (IRQ1)

Bit	7	6	5	4	3	2	1	0
Field	PA7I	PA6CI	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC3H							

Hex Address: FC4

Table 161. IRQ1 Enable High Bit Register (IRQ1ENH)

Bit	7	6	5	4	3	2	1	0
Field	PA7ENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC4H							

Hex Addresses: FC9–FCC

This address range is reserved.

Hex Address: FCD

Table 166. Interrupt Edge Select Register (IRQES)

Bit	7	6	5	4	3	2	1	0
Field	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCDH							

Hex Address: FCE

Table 167. Shared Interrupt Select Register (IRQSS)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	PA6CS	Reserved					
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCEH							

Hex Address: FCF

Table 168. Interrupt Control Register (IRQCTL)

Bit	7	6	5	4	3	2	1	0
Field	IRQE	Reserved						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R	R	R	R	R	R	R
Address	FCFH							

Hex Address: FDF**Table 183. Port D Output Data Register (PDOUT)**

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDFH							

Hex Addresses: FE0–FEF

This address range is reserved.

Watchdog Timer

For more information about the Watchdog Timer registers, see the [Watchdog Timer Control Register Definitions](#) section on page 95.

Hex Address: FF0

The Watchdog Timer Control Register address is shared with the read-only Reset Status Register.

Table 184. Watchdog Timer Control Register (WDTCTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTUNLK							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
Address	FF0H							

Table 185. Reset Status Register (RSTSTAT)

Bit	7	6	5	4	3	2	1	0
Field	POR	STOP	WDT	EXT	Reserved			
RESET	See Table 12 on page 29			0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	FF0H							