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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0430hj020sg |

## Nonvolatile Data Storage

The Nonvolatile Data Storage (NVDS) function uses a hybrid hardware/software scheme to implement a byte-programmable data memory and is capable of storing about 100,000 write cycles.

## Internal Precision Oscillator

The Internal Precision Oscillator (IPO) function, with an accuracy of ±4% full voltage/temperature range, is a trimmable clock source that requires no external components.

## External Crystal Oscillator

The crystal oscillator circuit provides highly accurate clock frequencies using an external crystal, ceramic resonator or RC network.

## 10-Bit Analog-to-Digital Converter

The optional Analog-to-Digital Converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from eight different analog input pins.

## Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable reference voltage or with a signal at the second input pin. The comparator output is used either to drive a logic output pin or to generate an interrupt.

## Timers

Two enhanced 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in ONE-SHOT, CONTINUOUS, GATED, CAPTURE, CAPTURE RESTART, COMPARE, CAPTURE and COMPARE, PWM SINGLE OUTPUT and PWM DUAL OUTPUT Modes.

## Interrupt Controller

The Z8 Encore! F0830 Series products support seventeen interrupt sources with sixteen interrupt vectors: up to five internal peripheral interrupts and up to twelve GPIO interrupts. These interrupts have three levels of programmable interrupt priority.

The analog supply pins ($AV_{DD}$ and $AV_{SS}$) are also not available on these parts and are replaced by PB6 and PB7.

At reset, by default, all pins of Port A, B and C are in Input state. The alternate functionality is also disabled, so the pins function as general purpose input ports until programmed otherwise. At power-up, the Port D0 pin defaults to the $\overline{\text{RESET}}$ Alternate function.

The pin configurations listed are preliminary and subject to change based on manufacturing limitations.

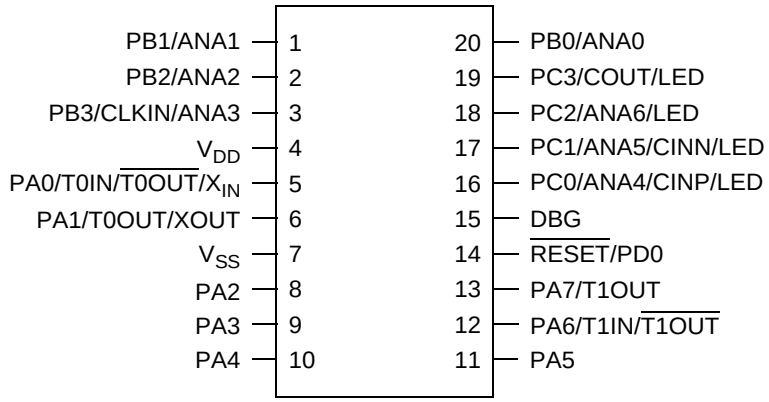


**Figure 2. Z8F0830 Series in 20-Pin SOIC, SSOP, PDIP Package**

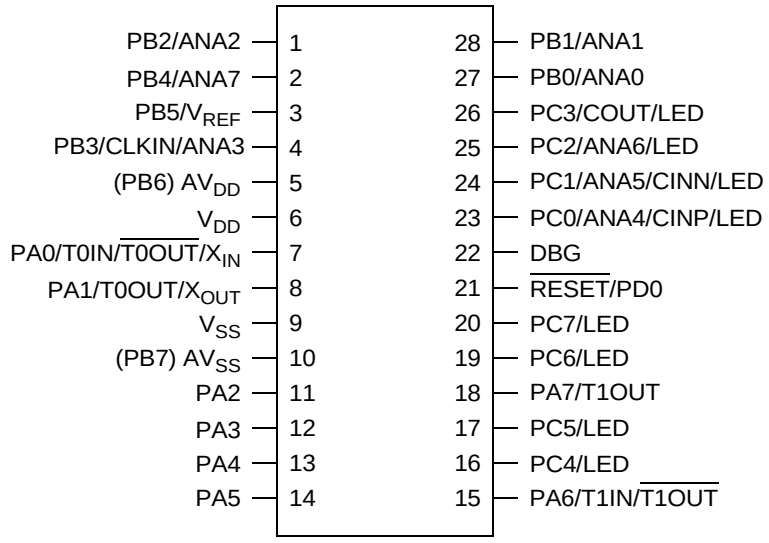


**Figure 3. Z8F0830 Series in 28-Pin SOIC, SSOP, PDIP Package**

# Interrupt Controller

The Interrupt Controller on the Z8 Encore!® F0830 Series products prioritize the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of the Interrupt Controller include:

- Seventeen interrupt sources using sixteen unique interrupt vectors:
  - Twelve GPIO port pin interrupt sources
  - Five on-chip peripheral interrupt sources (Comparator Output interrupt shares one interrupt vector with PA6)
- Flexible GPIO interrupts
  - Eight selectable rising and falling edge GPIO interrupts
  - Four dual-edge interrupts
- Three levels of individually programmable interrupt priority
- Watchdog Timer can be configured to generate an interrupt
  m

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the Interrupt Controller has no effect on operation. For more information about interrupt servicing by the eZ8 CPU, refer to the eZ8 CPU User Manual (UM0128), which is available for download at www.zilog.com.

## Interrupt Vector Listing

Table 34 lists the interrupts available in order of priority. The interrupt vector is stored with the most significant byte (MSB) at the even program memory address and the least significant byte (LSB) at the odd program memory address.

**Note:** Some port interrupts are not available on the 20-pin and 28-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.

## IRQ1 Enable High and Low Bit Registers

Table 41 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit registers, shown in Tables 42 and 43, form a priority-encoded enabling service for interrupts in the Interrupt Request 1 Register. Priority is generated by setting the bits in each register.

**Table 41. IRQ1 Enable and Priority Encoding**

| IRQ1ENH[*x*] | IRQ1ENL[*x*] | Priority | Description |
|---|---|---|---|
| 0 | 0 | Disabled | Disabled |
| 0 | 1 | Level 1 | Low |
| 1 | 0 | Level 2 | Nominal |
| 1 | 1 | Level 3 | High |

Note: *x* indicates register bits in the address range 7–0.

**Table 42. IRQ1 Enable High Bit Register (IRQ1ENH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PA7ENH | PA6CENH | PA5ENH | PA4ENH | PA3ENH | PA2ENH | PA1ENH | PA0ENH |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FC4H | | | | | | | |

| Bit | Description |
|---|---|
| [7] PA7ENH | **Port A Bit[7] Interrupt Request Enable High Bit** |
| [6] PA6CENH | **Port A Bit[7] or Comparator Interrupt Request Enable High Bit** |
| [5:0] PA*x*ENH | **Port A Bit[*x*] Interrupt Request Enable High Bit**<br>See the interrupt port select register for selection of either Port A or Port D as the interrupt source. |

Note: *x* indicates register bits in the address range 5–0.

| Bit | Description (Continued) |
|---|---|
| [0]<br>INPCAP | **Input Capture Event**<br>This bit indicates whether the most recent timer interrupt is caused by a timer input capture event.<br>0 = Previous timer interrupt is not caused by timer input capture event.<br>1 = Previous timer interrupt is caused by timer input capture event. |

## Timer 0–1 Control Register 1

The Timer 0–1 Control (TxCTL1) registers enable/disable the timers, set the prescaler value, and determine the timer operating mode.

**Table 57. Timer 0–1 Control Register 1 (TxCTL1)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TEN | TPOL | PRES | | | TMODE | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F07H, F0FH | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>TEN | **Timer Enable**<br>0 = Timer is disabled.<br>1 = Timer enabled to count. |

## Flash Page Select Register

The Flash Page Select Register shares address space with the Flash Sector Protect Register. Unless the Flash Controller is locked and written with 5EH, any writes to this address will target the Flash Page Select Register.

The register selects one of the eight available Flash memory pages to be programmed or erased. Each Flash page contains 512-bytes of Flash memory. During a page erase operation, all Flash memory containing addresses with the most significant 7-bits within FPS[6:0] are chosen for program/erase operations.

**Table 74. Flash Page Select Register (FPS)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | INFO_EN | PAGE | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF9H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>INFO_EN | **Information Area Enable**<br>0 = Information area is not selected.<br>1 = Information area is selected. The information area is mapped into the program memory address space at addresses FE00H through FFFFH. |
| [6:0]<br>PAGE | **Page Select**<br>This 7-bit field identifies the Flash memory page for page erase and page unlocking. Program memory address[15:9] = PAGE[6:0]. For Z8F04xx and Z8F02xx devices, the upper four bits must always be 0. For Z8F01xx devices, the upper five bits must always be 0. |

## Flash Sector Protect Register

The Flash Sector Protect Register is shared with the Flash Page Select Register. When the Flash Control Register is locked and written with 5EH, the next write to this address targets the Flash Sector Protect Register. In all other cases, it targets the Flash Page Select Register.

This register selects one of the eight available Flash memory sectors to be protected. The Reset state of each sector protect bit is the zero (unprotected) state. After a sector is protected by setting its corresponding register bit, the register bit cannot be cleared by the user.

To determine the appropriate Flash memory sector address range and sector number for your F0830 Series product, please refer to Table 70 on page 112.

**Table 75. Flash Sector Protect Register (FPROT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SPROT7 | SPROT6 | SPROT5 | SPROT4 | SPROT3 | SPROT2 | SPROT1 | SPROT0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF9H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0]<br>SPROT*x* | **Sector Protection**<br>For Z8F12xx, Z8F08xx and Z8F04xx devices, all bits are used. For Z8F02xx devices, the upper four bits remain unused. For Z8F01xx devices, the upper six bits remain unused. To determine the appropriate Flash memory sector address range and sector number for your F0830 Series product, please refer to Table 69 and to Figures 14 through 18. |

Note: *x* indicates bits in the range 7–0.

| Bit | Description (Continued) |
|---|---|
| [4]<br>XTLDIS | **State of the Crystal Oscillator at Reset**<br>This bit enables only the crystal oscillator. Selecting the crystal oscillator as the system clock must be performed manually.<br>0 = The crystal oscillator is enabled during reset, resulting in longer reset timing.<br>1 = The crystal oscillator is disabled during reset, resulting in shorter reset timing. |
| [3:0] | **Reserved**<br>These bits are reserved and must be programmed to 1111. |

# Trim Bit Address Space

All available trim bit addresses and their functions are listed in Tables 83 through 90.

| Bit | Description (Continued) |
|---|---|
| [4]<br>POFEN | **Primary Oscillator Failure Detection Enable**<br>1 = Failure detection and recovery of primary oscillator is enabled.<br>0 = Failure detection and recovery of primary oscillator is disabled. |
| [3]<br>WDFEN | **Watchdog Timer Oscillator Failure Detection Enable**<br>1 = Failure detection of Watchdog Timer Oscillator is enabled.<br>0 = Failure detection of Watchdog Timer Oscillator is disabled. |
| [2:0]<br>SCKSEL | **System Clock Oscillator Select**<br>000 = Internal Precision Oscillator functions as system clock at 5.53 MHz.<br>001 = Internal Precision Oscillator functions as system clock at 32 kHz.<br>010 = Crystal oscillator or external RC oscillator functions as system clock.<br>011 = Watchdog Timer Oscillator functions as system clock.<br>100 = External clock signal on PB3 functions as system clock.<br>101 = Reserved.<br>110 = Reserved.<br>111 = Reserved. |

# Crystal Oscillator

The products in the Z8 Encore! F0830 Series contain an on-chip crystal oscillator for use with external crystals with 32kHz to 20MHz frequencies. In addition, the oscillator supports external RC networks with oscillation frequencies up to 4MHz or ceramic resonators with frequencies up to 8MHz. The on-chip crystal oscillator can be used to generate the primary system clock for the internal eZ8 CPU and the majority of its on-chip peripherals. Alternatively, the $X_{IN}$ input pin can also accept a CMOS-level clock input signal (32kHz–20MHz). If an external clock generator is used, the $X_{OUT}$ pin must remain unconnected. The on-chip crystal oscillator also contains a clock filter function. To see the settings for this clock filter, see Table 90 on page 133. By default, however, this clock filter is disabled; therefore, no divide to the input clock (namely, the frequency of the signal on the $X_{IN}$ input pin) can determine the frequency of the system clock when using the default settings.

**Note:** Although the $X_{IN}$ pin can be used as an input for an external clock generator, the CLKIN pin is better suited for such use. See *the* System Clock Selection *section on page 151* for more information.

## Operating Modes

The Z8 Encore! F0830 Series products support the following four OSCILLATOR Modes:

- Minimum power for use with very low frequency crystals (32kHz to 1MHz)
- Medium power for use with medium frequency crystals or ceramic resonators (0.5MHz to 8MHz)
- Maximum power for use with high frequency crystals (8MHz to 20MHz)
- On-chip oscillator configured for use with external RC networks (<4MHz)

The OSCILLATOR Mode is selected using user-programmable Flash option bits. See the Flash Option Bits chapter on page 124 for more information.

## Crystal Oscillator Operation

The XTLDIS Flash option bit controls whether the crystal oscillator is enabled during reset. The crystal may later be disabled after reset if a new oscillator has been selected as the system clock. If the crystal is manually enabled after reset through the OSCCTL Reg-

**Table 113. eZ8 CPU Instruction Summary (Continued)**

| Assembly Mnemonic | Symbolic Operation | Address Mode dst | Address Mode src | Op Code(s) (Hex) | Flags C | Z | S | V | D | H | Fetch Cycles | Instr. Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DJNZ dst, RA | dst ← dst – 1<br>if dst ≠ 0<br>PC ← PC + X | r | | 0A–FA | – | – | – | – | – | – | 2 | 3 |
| EI | IRQCTL[7] ← 1 | | | 9F | – | – | – | – | – | – | 1 | 2 |
| HALT | HALT Mode | | | 7F | – | – | – | – | – | – | 1 | 2 |
| INC dst | dst ← dst + 1 | R | | 20 | – | * | * | – | – | – | 2 | 2 |
| | | IR | | 21 | | | | | | | 2 | 3 |
| | | r | | 0E–FE | | | | | | | 1 | 2 |
| INCW dst | dst ← dst + 1 | RR | | A0 | – | * | * | * | – | – | 2 | 5 |
| | | IRR | | A1 | | | | | | | 2 | 6 |
| IRET | FLAGS ← @SP<br>SP ← SP + 1<br>PC ← @SP<br>SP ← SP + 2<br>IRQCTL[7] ← 1 | | | BF | * | * | * | * | * | * | 1 | 5 |
| JP dst | PC ← dst | DA | | 8D | – | – | – | – | – | – | 3 | 2 |
| | | IRR | | C4 | | | | | | | 2 | 3 |
| JP cc, dst | if cc is true<br>PC ← dst | DA | | 0D–FD | – | – | – | – | – | – | 3 | 2 |
| JR dst | PC ← PC + X | DA | | 8B | – | – | – | – | – | – | 2 | 2 |
| JR cc, dst | if cc is true<br>PC ← PC + X | DA | | 0B–FB | – | – | – | – | – | – | 2 | 2 |

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

**Table 113. eZ8 CPU Instruction Summary (Continued)**

| Assembly Mnemonic | Symbolic Operation | Address Mode dst | Address Mode src | Op Code(s) (Hex) | Flags C | Z | S | V | D | H | Fetch Cycles | Instr. Cycles |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TM dst, src | dst AND src | r | r | 72 | – | * | * | 0 | – | – | 2 | 3 |
| | | r | Ir | 73 | | | | | | | 2 | 4 |
| | | R | R | 74 | | | | | | | 3 | 3 |
| | | R | IR | 75 | | | | | | | 3 | 4 |
| | | R | IM | 76 | | | | | | | 3 | 3 |
| | | IR | IM | 77 | | | | | | | 3 | 4 |
| TMX dst, src | dst AND src | ER | ER | 78 | – | * | * | 0 | – | – | 4 | 3 |
| | | ER | IM | 79 | | | | | | | 4 | 3 |
| TRAP Vector | SP ← SP – 2<br>@SP ← PC<br>SP ← SP – 1<br>@SP ← FLAGS<br>PC ← @Vector | | Vec-tor | F2 | – | – | – | – | – | – | 2 | 6 |
| WDT | | | | 5F | – | – | – | – | – | – | 1 | 2 |
| XOR dst, src | dst ← dst XOR src | r | r | B2 | – | * | * | 0 | – | – | 2 | 3 |
| | | r | Ir | B3 | | | | | | | 2 | 4 |
| | | R | R | B4 | | | | | | | 3 | 3 |
| | | R | IR | B5 | | | | | | | 3 | 4 |
| | | R | IM | B6 | | | | | | | 3 | 3 |
| | | IR | IM | B7 | | | | | | | 3 | 4 |
| XORX dst, src | dst ← dst XOR src | ER | ER | B8 | – | * | * | 0 | – | – | 4 | 3 |
| | | ER | IM | B9 | | | | | | | 4 | 3 |

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

**Table 114. Op Code Map Abbreviations**

| Abbreviation | Description | Abbreviation | Description |
|---|---|---|---|
| b | Bit position | IRR | Indirect Register Pair |
| cc | Condition code | p | Polarity (0 or 1) |
| X | 8-bit signed index or displacement | r | 4-bit Working Register |
| DA | Destination address | R | 8-bit register |
| ER | Extended Addressing Register | r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1 | Destination address |
| IM | Immediate data value | r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2 | Source address |
| Ir | Indirect Working Register | RA | Relative |
| IR | Indirect Register | rr | Working Register Pair |
| Irr | Indirect Working Register Pair | RR | Register Pair |

| Upper Nibble (Hex) \ Lower Nibble (Hex) | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | | | | | | |
| 1 | | | | | | | | | | | | | | | | |
| 2 | | | | | | | | | | | | | | | | |
| 3 | | | | | | | | | | | | | | | | |
| 4 | | | | | | | | | | | | | | | | |
| 5 | | | | | | | | | | | | | | | | |
| 6 | | | | | | | | | | | | | | | | |
| 7 | 3.2 PUS | | | | | | | | | | | | | | | |
| 8 | | | | | | | | | | | | | | | | |
| 9 | | | | | | | | | | | | | | | | |
| A | | | 3.3 **CPC** r1,r2 | 3.4 **CPC** r1,Ir2 | 4.3 **CPC** R2,R1 | 4.4 **CPC** IR2,R1 | 4.3 **CPC** R1,IM | 4.4 **CPC** IR1,IM | 5.3 **CPCX** ER2,ER1 | 5.3 **CPCX** IM,ER1 | | | | | | |
| B | | | | | | | | | | | | | | | | |
| C | 3.2 **SRL** R1 | 3.3 **SRL** IR1 | | | | | | | | | | | | | | |
| D | | | | | | | | | | | | | | | | |
| E | | | | | | | | | 5, 4 **LDWX** ER2,ER1 | | | | | | | |
| F | | | | | | | | | | | | | | | | |

**Figure 30. Second Op Code Map after 1FH**

# AC Characteristics

The section provides information about the AC characteristics and timing. All AC timing information assumes a standard load of 50pF on all outputs.

**Table 117. AC Characteristics**

| | | $V_{DD}$ = 2.7 to 3.6V $T_A$ = 0°C to +70°C | | $V_{DD}$ = 2.7 to 3.6V $T_A$ = –40°C to +105°C | | | |
|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Units** | **Conditions** |
| $F_{SYSCLK}$ | System Clock Frequency | | | – | 20.0 | MHz | Read-only from Flash memory |
| | | | | 0.032768 | 20.0 | MHz | Program or erasure of the Flash memory |
| $F_{XTAL}$ | Crystal Oscillator Frequency | | | 1.0 | 20.0 | MHz | System clock frequencies below the crystal oscillator minimum require an external |
| $F_{IPO}$ | Internal Precision Oscillator Frequency | | | 0.032768 | 5.5296 | MHz | Oscillator is **not** adjustable over the entire range. User may select Min or Max value only. |
| $F_{IPO}$ | Internal Precision Oscillator Frequency | | | 5.31 | 5.75 | MHz | High speed with trimming |
| $F_{IPO}$ | Internal Precision Oscillator Frequency | | | 4.15 | 6.91 | MHz | High speed without trimming |
| $F_{IPO}$ | Internal Precision Oscillator Frequency | | | 30.7 | 33.3 | KHz | Low speed with trimming |
| $F_{IPO}$ | Internal Precision Oscillator Frequency | | | 24 | 40 | KHz | Low speed without trimming |
| $T_{XIN}$ | System Clock Period | | | 50 | – | ns | $T_{CLK} = 1/F_{sysclk}$ |
| $T_{XINH}$ | System Clock High Time | | | 20 | 30 | ns | $T_{CLK}$ = 50 ns |
| $T_{XINL}$ | System Clock Low Time | | | 20 | 30 | ns | $T_{CLK}$ = 50 ns |

## General Purpose I/O Port Output Timing

Figure 34 and Table 125 provide timing information for the GPIO port pins.

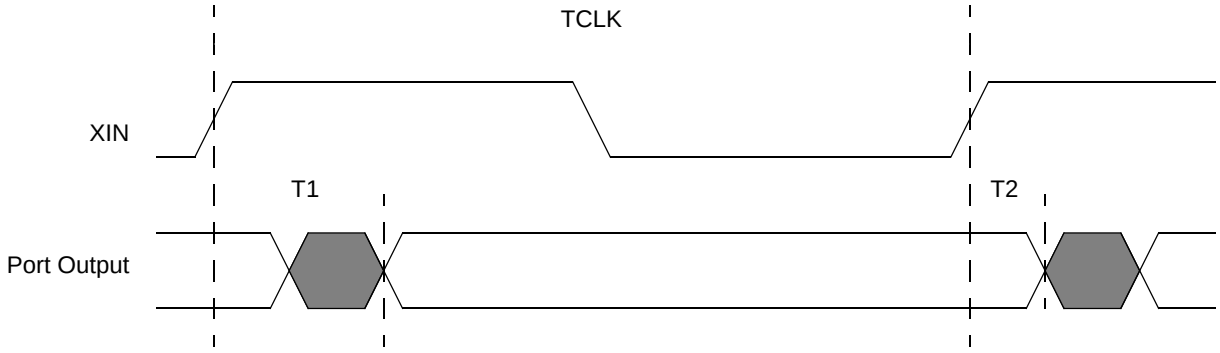


**Figure 34. GPIO Port Output Timing**

**Table 125. GPIO Port Output Timing**

| | | Delay (ns) | |
|---|---|---|---|
| **Parameter** | **Abbreviation** | **Minimum** | **Maximum** |
| **GPIO Port Pins** | | | |
| $T_1$ | XIN Rise to Port Output Valid Delay | – | 15 |
| $T_2$ | XIN Rise to Port Output Hold Time | 2 | – |

### Hex Address: F01

**Table 131. Timer 0 Low Byte Register (T0L)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TL | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F01H | | | | | | | |

### Hex Address: F02

**Table 132. Timer 0 Reload High Byte Register (T0RH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TRH | | | | | | | |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F02H | | | | | | | |

### Hex Address: F03

**Table 133. Timer 0 Reload Low Byte Register (T0RL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TRL | | | | | | | |
| RESET | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F03H | | | | | | | |

### Hex Address: F04

**Table 134. Timer 0 PWM High Byte Register (T0PWMH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | PWMH | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F04H | | | | | | | |

### Hex Address: FDF

**Table 183. Port D Output Data Register (PDOUT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | POUT7 | POUT6 | POUT5 | POUT4 | POUT3 | POUT2 | POUT1 | POUT0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FDFH | | | | | | | |

### Hex Addresses: FE0–FEF

This address range is reserved.

## Watchdog Timer

For more information about the Watchdog Timer registers, see the Watchdog Timer Control Register Definitions section on page 95.

### Hex Address: FF0

The Watchdog Timer Control Register address is shared with the read-only Reset Status Register.

**Table 184. Watchdog Timer Control Register (WDTCTL)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | WDTUNLK | | | | | | | |
| RESET | X | X | X | X | X | X | X | X |
| R/W | W | W | W | W | W | W | W | W |
| Address | FF0H | | | | | | | |

**Table 185. Reset Status Register (RSTSTAT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | POR | STOP | WDT | EXT | Reserved | | | |
| RESET | See Table 12 on page 29 | | | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R |
| Address | FF0H | | | | | | | |

### Hex Address: FF8

**Table 192. Flash Status Register (FSTAT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | FSTAT | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R |
| Address | FF8H | | | | | | | |

### Hex Address: FF9

The Flash Page Select Register is shared with the Flash Sector Protect Register.

**Table 193. Flash Page Select Register (FPS)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | INFO_EN | PAGE | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF9H | | | | | | | |

**Table 194. Flash Sector Protect Register (FPROT)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | SPROT7 | SPROT6 | SPROT5 | SPROT4 | SPROT3 | SPROT2 | SPROT1 | SPROT0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FF9H | | | | | | | |

### Hex Address: FFA

**Table 195. Flash Frequency High Byte Register (FFREQH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | FFREQH | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | FFAH | | | | | | | |

## D



## E



## F