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#### Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0430ph020eg">https://www.e-xfl.com/product-detail/zilog/z8f0430ph020eg</a>

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## Data Memory

The Z8 Encore! F0830 Series does not use the eZ8 CPU's 64KB data memory address space.

## Flash Information Area

Table 7 maps the Z8 Encore! F0830 Series Flash information area. The 128-byte information area is accessed, by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash information area is mapped into program memory and overlays these 128 bytes at addresses FE00H to FE7FH. When information area access is enabled, all reads from these program memory addresses return information area data rather than program memory data. Access to the Flash information area is read-only.

**Table 7. Z8 Encore! F0830 Series Flash Memory Information Area Map**

<b>Program Memory Address (Hex)</b>	<b>Function</b>
FE00–FE3F	Zilog option bits
FE40–FE53	Part Number 20-character ASCII alphanumeric code Left-justified and filled with FH
FE54–FE5F	Reserved
FE60–FE7F	Reserved
FE80–FFFF	Reserved

## GPIO Interrupts

Many of the GPIO port pins can be used as interrupt sources. Some port pins can be configured to generate an interrupt request on either the rising edge or falling edge of the input pin signal. Other port pin interrupt sources, generate an interrupt when any edge occurs (both rising and falling). See the [Interrupt Controller](#) chapter on page 53 for more information about interrupts using the GPIO pins.

## GPIO Control Register Definitions

Four registers for each port provide access to GPIO control, input data and output data; Table 17 lists these port registers. Use the Port A–D Address and Control registers together to provide access to subregisters for port configuration and control.

**Table 17. GPIO Port Registers and Subregisters**

Port Register Mnemonic	Port Register Name
PxADDR	Port A–D Address Register (selects subregisters)
PxCTL	Port A–D Control Register (provides access to subregisters)
PxIN	Port A–D Input Data Register
PxOUT	Port A–D Output Data Register
Port Subregister Mnemonic	Port Register Name
PxDD	Data Direction
PxAF	Alternate Function
PxOC	Output Control (open-drain)
PxHDE	High Drive Enable
PxSMRE	Stop Mode Recovery Source Enable
PxPUE	Pull-Up Enable
PxAFS1	Alternate Function Set 1
PxAFS2	Alternate Function Set 2

## Port A–D Control Registers

The Port A–D Control registers, shown in Table 20, set the GPIO port operation. The value in the corresponding Port A–D Address Register determines which subregister is read from or written to by a Port A–D Control Register transaction.

**Table 20. Port A–D Control Registers (PxCTL)**

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD1H, FD5H, FD9H, FDDH							

Bit	Description
[7:0] PCTL	<b>Port Control</b> The Port Control Register provides access to all subregisters that configure the GPIO port operation.

## Port A–D Data Direction Subregisters

The Port A–D Data Direction Subregister, shown in Table 21, is accessed through the Port A–D Control Register by writing 01H to the Port A–D Address Register.

**Table 21. Port A–D Data Direction Subregisters (PxDD)**

Bit	7	6	5	4	3	2	1	0
Field	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 01H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0] DDx	<b>Data Direction</b> These bits control the direction of the associated port pin. Port Alternate Function operation overrides the Data Direction Register setting. 0 = Output. Data in the Port A–D Output Data Register is driven onto the port pin. 1 = Input. The port pin is sampled and the value written into the Port A–D Input Data Register. The output driver is tristated.

Note: x indicates the specific GPIO port pin number (7–0).

reload. For the timer output to make a state change at a ONE-SHOT time-out (rather than a single cycle pulse), first set the TPOL bit in the Timer Control Register to the start value before enabling ONE-SHOT Mode. After starting the timer, set TPOL to the opposite bit value.

Observe the following steps for configuring a timer for ONE-SHOT Mode and for initiating the count:

1. Write to the Timer Control Register to:
  - Disable the timer
  - Configure the timer for ONE-SHOT Mode
  - Set the prescale value
  - Set the initial output level (High or Low) if using the timer output Alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. If using the timer output function, configure the associated GPIO port pin for the timer output alternate function.
6. Write to the Timer Control Register to enable the timer and initiate counting.

In ONE-SHOT Mode, the system clock always provides the timer input. The timer period is calculated with the following equation:

$$\text{One-Shot Mode Time-Out Period (s)} = \frac{(\text{Reload Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

## **CONTINUOUS Mode**

In CONTINUOUS Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and the counting resumes. Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps for configuring a timer for CONTINUOUS Mode and for initiating the count:

1. Write to the Timer Control Register to:

6. Write to the Timer Control Register to enable the timer.
7. Counting begins on the first appropriate transition of the timer input signal. No interrupt is generated by the first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

## Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on Timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the timer low byte register are placed in a holding register. A subsequent read from the timer low byte register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value when enabled. When the timers are not enabled, a read from the timer low byte register returns the actual value in the counter.

## Timer Pin Signal Operation

Timer output is a GPIO port pin alternate function. The timer output is toggled every time the counter is reloaded.

The timer input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO alternate function registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT Mode. For this mode, no timer input is available.



### WDT Reset in Normal Operation

If configured to generate a reset when a time-out occurs, the Watchdog Timer forces the device into the System Reset state. The WDT status bit in the Watchdog Timer Control Register is set to 1. See *the Reset and Stop Mode Recovery chapter on page 21* for more information about system reset operations.

### WDT Reset in STOP Mode

If configured to generate a reset when a time-out occurs and the device is in STOP Mode, the Watchdog Timer initiates a Stop Mode Recovery. Both the WDT status bit and the STOP bit in the Watchdog Timer Control Register are set to 1 following WDT time-out in STOP Mode. See *the Reset and Stop Mode Recovery chapter on page 21* for more information about Stop Mode Recovery operations.

## Watchdog Timer Reload Unlock Sequence

Writing the unlock sequence to the Watchdog Timer (WDTCTL) Control Register address, unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTL and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address produce no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the reload registers.

The following sequence is required to unlock the Watchdog Timer Reload Byte registers (WDTU, WDTL and WDTL) for write access:

1. Write 55H to the Watchdog Timer Control Register (WDTCTL).
2. Write AAH to the Watchdog Timer Control Register (WDTCTL).
3. Write the Watchdog Timer Reload Upper Byte Register (WDTU).
4. Write the Watchdog Timer Reload High Byte Register (WDTL).
5. Write the Watchdog Timer Reload Low Byte Register (WDTL).

All three Watchdog Timer Reload registers must be written in the order listed above. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

## ADC Control Register 0

The ADC Control 0 Register, shown in Table 63, initiates an A/D conversion and provides ADC status information.

**Table 63. ADC Control Register 0 (ADCCTL0)**

Bit	7	6	5	4	3	2	1	0
Field	START	Reserved	REFEN	ADCEN	Reserved	ANAIN[2:0]		
RESET	0	0	0	0	0	0	0	0
R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F70h							

Bit	Description
[7] START	<b>ADC Start/Busy</b> 0 = Writing to 0 has no effect; reading a 0 indicates that the ADC is available to begin a conversion. 1 = Writing to 1 starts a conversion; reading a 1 indicates that a conversion is currently in progress.
[6]	<b>Reserved</b> This bit is reserved and must be programmed to 0.
[5] REFEN	<b>Reference Enable</b> 0 = Internal reference voltage is disabled allowing an external reference voltage to be used by the ADC. 1 = Internal reference voltage for the ADC is enabled. The internal reference voltage can be measured on the $V_{REF}$ pin.
[4] ADCEN	<b>ADC Enable</b> 0 = ADC is disabled for low power operation. 1 = ADC is enabled for normal use.
[3]	<b>Reserved</b> This bit is reserved and must be programmed to 0.
[2:0] ANAIN	<b>Analog Input Select</b> 000 = ANA0 input is selected for analog to digital conversion. 001 = ANA1 input is selected for analog to digital conversion. 010 = ANA2 input is selected for analog to digital conversion. 011 = ANA3 input is selected for analog to digital conversion. 100 = ANA4 input is selected for analog to digital conversion. 101 = ANA5 input is selected for analog to digital conversion. 110 = ANA6 input is selected for analog to digital conversion. 111 = ANA7 input is selected for analog to digital conversion.

- The Flash Sector Protect Register is ignored for programming and Erase operations.
- Programming operations are not limited to the page selected in the page select register.
- Bits in the Flash Sector Protect Register can be written to one or zero.
- The second write of the page select register to unlock the Flash Controller is not necessary.
- The page select register can be written when the Flash Controller is unlocked.
- The mass erase command is enabled through the Flash Control Register

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**!** **Caution:** For security reasons, Flash Controller allows only a single page to be opened for write/erase. When writing multiple Flash pages, the Flash Controller must go through the unlock sequence again to select another page.

---

## NVDS Operational Requirements

The device uses a 12KB Flash memory space, despite the maximum specified Flash size of 8KB (with the exception of 12KB mode with non-NVDS). User code accesses the lower 8KB of Flash, leaving the upper 4KB for proprietary (for Zilog-only) memory. The NVDS is implemented by using this proprietary memory space for special-purpose routines and for the data required by these routines, which are factory-programmed and cannot be altered by the user. The NVDS operation is described in detail in *the [Nonvolatile Data Storage](#) chapter on page 134*.

The NVDS routines are triggered by a user code: CALL into proprietary memory. Code executing from this proprietary memory must be able to read and write other locations within proprietary memory. User code must not be able to read or write proprietary memory.

## Flash Control Register Definitions

This section defines the features of the following Flash Control registers.

Flash Control Register: see page 119

Flash Status Register: see page 120

Flash Page Select Register: see page 121

Flash Sector Protect Register: see page 122

Flash Frequency High and Low Byte Registers: see page 123

## Flash Control Register

The Flash Controller must be unlocked using the Flash Control Register before programming or erasing Flash memory. Writing the sequence 73H 8CH, sequentially, to the Flash Control Register unlocks the Flash Controller. When the Flash Controller is unlocked, Flash memory can be enabled for mass erase or page erase by writing the appropriate enable command to the FCTL. Page erase applies only to the active page selected in Flash Page Select Register. Mass erase is enabled only through the On-Chip Debugger. Writing an invalid value or an invalid sequence returns the Flash Controller to its Locked state. The write-only Flash Control Register shares its register file address with the read-only Flash Status Register.

**Table 72. Flash Control Register (FCTL)**

Bit	7	6	5	4	3	2	1	0
Field	FCMD							
RESET	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
Address	FF8H							

Bit	Description
[7:0]	<b>Flash Command</b>
FCMD	73H = First unlock command. 8CH = Second unlock command. 95H = Page erase command (must be third command in sequence to initiate page erase). 63H = Mass erase command (must be third command in sequence to initiate mass erase). 5EH = Enable Flash Sector Protect Register access.

► **Note:** The bit values used in Table 85 are set at the factory; no calibration is required.

**Table 86. Trim Option Bits at 0002H (TIPO)**

Bit	7	6	5	4	3	2	1	0
Field	IPO_TRIM							
RESET	U							
R/W	R/W							
Address	Information Page Memory 0022H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0]	<b>Internal Precision Oscillator Trim Byte</b>
IPO_TRIM	Contains trimming bits for the Internal Precision Oscillator.

► **Note:** The bit values used in Table 86 are set at the factory; no calibration is required.

**Table 87. Trim Option Bits at 0003H (TVBO)**

Bit	7	6	5	4	3	2	1	0
Field	Reserved				Reserved	VBO_TRIM		
RESET	U				U	1	0	0
R/W	R/W				R/W	R/W		
Address	Information Page Memory 0023H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:3]	<b>Reserved</b> These bits are reserved and must be programmed to 11111.
[2]	<b>VBO Trim Values</b>
VBO_TRIM	Contains factory-trimmed values for the oscillator and the VBO.

## Operation

The following section describes the operation of the On-Chip Debugging function.

### OCD Interface

The On-Chip Debugger uses the DBG pin for communication with an external host. This one-pin interface is a bidirectional open-drain interface that transmits and receives data. Data transmission is half-duplex, which means that transmission and data retrieval cannot occur simultaneously. The serial data on the DBG pin is sent using the standard asynchronous data format defined in RS-232. This pin creates an interface between the Z8 Encore! F0830 Series products and the serial port of a host PC using minimal external hardware. Two different methods for connecting the DBG pin to an RS-232 interface are displayed in Figures 21 and 22. The recommended method is the buffered implementation depicted in Figure 22. The DBG pin must always be connected to  $V_{DD}$  through an external pull-up resistor.

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**! Caution:** For proper operation of the On-Chip Debugger, all power pins ( $V_{DD}$  and  $AV_{DD}$ ) must be supplied with power and all ground pins ( $V_{SS}$  and  $AV_{SS}$ ) must be properly grounded. The DBG pin is open-drain and must always be connected to  $V_{DD}$  through an external pull-up resistor to ensure proper operation.

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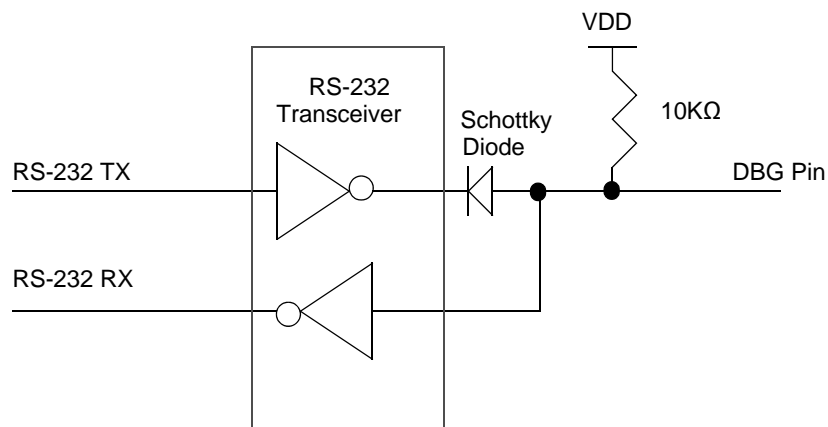


Figure 21. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #1 of 2

When selecting a new clock source, the primary oscillator failure detection circuitry and the Watchdog Timer Oscillator failure circuitry must be disabled. If POFEN and WOFEN are not disabled prior to a clock switch-over, it is possible to generate an interrupt for a failure of either oscillator. The failure detection circuitry can be enabled anytime after a successful write of OSCSEL in the Oscillator Control Register.

The Internal Precision Oscillator is enabled by default. If the user code changes to a different oscillator, it may be appropriate to disable the IPO for power savings. Disabling the IPO does not occur automatically.

## Clock Failure Detection and Recovery

### Primary Oscillator Failure

The Z8F04xA family devices can generate nonmaskable interrupt-like events when the primary oscillator fails. To maintain system function in this situation, the clock failure recovery circuitry automatically forces the Watchdog Timer Oscillator to drive the system clock. The Watchdog Timer Oscillator must be enabled to allow the recovery. Although this oscillator runs at a much slower speed than the original system clock, the CPU continues to operate, allowing execution of a clock failure vector and software routines that either remedy the oscillator failure or issue a failure alert. This automatic switch-over is not available if the Watchdog Timer is the primary oscillator. It is also unavailable if the Watchdog Timer Oscillator is disabled, though it is not necessary to enable the Watchdog Timer reset function outlined in the Watchdog Timer chapter of this document.

The primary oscillator failure detection circuitry asserts if the system clock frequency drops below 1 KHz  $\pm 50\%$ . If an external signal is selected as the system oscillator, it is possible that a very slow but nonfailing clock can generate a failure condition. Under these conditions, do not enable the clock failure circuitry (POFEN must be deasserted in the OSCCTL Register).

### Watchdog Timer Failure

In the event of failure of a Watchdog Timer Oscillator, a similar nonmaskable interrupt-like event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a primary oscillator failure. The failure detection circuitry does not function if the Watchdog Timer is used as the primary oscillator or if the Watchdog Timer Oscillator has been disabled. For either of these cases, it is necessary to disable the detection circuitry by deasserting the WDFEN bit of the OSCCTL Register.

The Watchdog Timer Oscillator failure detection circuit counts system clocks while looking for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which the Watchdog Timer failure is detected. A very slow system clock results in very slow detection times.

Table 128. Z8 Encore! XP F0830 Series Ordering Matrix

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8F0131PJ020SG	1KB	256	Yes	0	PDIP 28-pin
Z8F0131QJ020SG	1KB	256	Yes	0	QFN 28-pin
<b>Extended Temperature: –40°C to 105°C</b>					
Z8F0130SH020EG	1KB	256	Yes	7	SOIC 20-pin
Z8F0130HH020EG	1KB	256	Yes	7	SSOP 20-pin
Z8F0130PH020EG	1KB	256	Yes	7	PDIP 20-pin
Z8F0130QH020EG	1KB	256	Yes	7	QFN 20-pin
Z8F0131SH020EG	1KB	256	Yes	0	SOIC 20-pin
Z8F0131HH020EG	1KB	256	Yes	0	SSOP 20-pin
Z8F0131PH020EG	1KB	256	Yes	0	PDIP 20-pin
Z8F0131QH020EG	1KB	256	Yes	0	QFN 20-pin
Z8F0130SJ020EG	1KB	256	Yes	8	SOIC 28-pin
Z8F0130HJ020EG	1KB	256	Yes	8	SSOP 28-pin
Z8F0130PJ020EG	1KB	256	Yes	8	PDIP 28-pin
Z8F0130QJ020EG	1KB	256	Yes	8	QFN 28-pin
Z8F0131SJ020EG	1KB	256	Yes	0	SOIC 28-pin
Z8F0131HJ020EG	1KB	256	Yes	0	SSOP 28-pin
Z8F0131PJ020EG	1KB	256	Yes	0	PDIP 28-pin
Z8F0131QJ020EG	1KB	256	Yes	0	QFN 28-pin
ZUSBSC00100ZACG					USB Smart Cable Accessory Kit
ZUSBOPTSC01ZACG					Opto-Isolated USB Smart Cable Accessory Kit

## Part Number Suffix Designations

Zilog part numbers consist of a number of components, as indicated in the following example.

**Example.** Part number Z8F0830SH020SG is an 8-bit 20MHz Flash MCU with 8KB Program Memory and equipped with ADC and NVDS in a 20-pin SOIC package, operating within a 0°C to +70°C temperature range and built using lead-free solder.



## Appendix A. Register Tables

For the reader's convenience, this appendix lists all F0830 Series registers numerically by hexadecimal address.

### General Purpose RAM

In the F0830 Series, the 000–EFF hexadecimal address range is partitioned for general-purpose random access memory, as follows.

#### Hex Addresses: 000–0FF

This address range is reserved for general-purpose register file RAM. For more details, see the [Register File](#) section on page 14.

#### Hex Addresses: 100–EFF

This address range is reserved.

### Timer 0

For more information about these Timer Control registers, see the [Timer Control Register Definitions](#) section on page 83.

#### Hex Address: F00

Table 130. Timer 0 High Byte Register (T0H)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H							

**Hex Address: F01**

**Table 131. Timer 0 Low Byte Register (T0L)**

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H							

**Hex Address: F02**

**Table 132. Timer 0 Reload High Byte Register (T0RH)**

Bit	7	6	5	4	3	2	1	0
Field	TRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F02H							

**Hex Address: F03**

**Table 133. Timer 0 Reload Low Byte Register (T0RL)**

Bit	7	6	5	4	3	2	1	0
Field	TRL							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F03H							

**Hex Address: F04**

**Table 134. Timer 0 PWM High Byte Register (T0PWMH)**

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F04H							

**Hex Address: F05**

**Table 135. Timer 0 PWM Low Byte Register (T0PWML)**

Bit	7	6	5	4	3	2	1	0
Field	PWML							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F05H							

**Hex Address: F06**

**Table 136. Timer 0 Control Register 0 (T0CTL0)**

Bit	7	6	5	4	3	2	1	0
Field	TMODEHI	TICONFIG		Reserved	PWMD			INPCAP
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F06H							

**Hex Address: F07**

**Table 137. Timer 0 Control Register 1 (T0CTL1)**

Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F07H							

**Hex Address: F08**

**Table 138. Timer 1 High Byte Register (T1H)**

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F08H							

**Hex Address: F09**

**Table 139. Timer 1 Low Byte Register (T1L)**

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F09H							

**Hex Address: F0A**

**Table 140. Timer 1 Reload High Byte Register (T1RH)**

Bit	7	6	5	4	3	2	1	0
Field	TRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F0AH							

**Hex Address: F0B**

**Table 141. Timer 1 Reload Low Byte Register (T1RL)**

Bit	7	6	5	4	3	2	1	0
Field	TRL							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F0BH							

**Hex Address: F0C**

**Table 142. Timer 1 PWM High Byte Register (T1PWMH)**

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F0CH							

## Low Power Control

For more information about the Power Control Register, see the [Power Control Register Definitions](#) section on page 31.

### Hex Address: F80

Table 151. Power Control Register 0 (PWRCTL0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved			VBO	Reserved	Reserved	COMP	Reserved
RESET	1	0	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F80H							

### Hex Address: F81

This address range is reserved.

## LED Controller

For more information about the LED Drive registers, see the [GPIO Control Register Definitions](#) section on page 39.

### Hex Address: F82

Table 152. LED Drive Enable (LEDEN)

Bit	7	6	5	4	3	2	1	0
Field	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F82H							