

Welcome to **E-XFL.COM**

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

| Details | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 23 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.600", 15.24mm) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0430pj020sg |

Table of Contents

| List of Tables xi Overview xi Features Part Selection Guide Block Diagram 20 CPU and Peripheral Overview 30 General Purpose Input/Output 40 Flash Controller 41 Nonvolatile Data Storage 11 Internal Precision Oscillator 10 External Crystal Oscillator 10 External Crystal Oscillator 10 Internal Precision Oscillator 10 Internal Precision Oscillator 10 External Crystal Oscillator 10 External Crystal Oscillator 10 External Crystal Oscillator 10 External Crystal Oscillator 10 Bit Analog-to-Digital Converter 4 Analog Comparator 4 Timers 1 Interrupt Controller 1 Reset Controller 1 On-Chip Debugger 4 Acronyms and Expansions 1 Pin Description 4 Available Packages 1 Pin Configurations 1 Signal De | Revision Historyii |
|--|-------------------------------|
| Overview Features Part Selection Guide Block Diagram CPU and Peripheral Overview General Purpose Input/Output Flash Controller Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Address Space Register File Program Memory 1 Data Memory Flash Information Area Register Map Reset Types Reset Types 2 Reset Types 2 Reset Types 2 Reset Types 2 Reset Sources 2 | List of Figures |
| Features Part Selection Guide Block Diagram CPU and Peripheral Overview General Purpose Input/Output Flash Controller Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Address Space Register File Program Memory 1 Data Memory Flash Information Area Reset and Stop Mode Recovery Reset Types Reset Types Reset Types Reset Sources 2 Reset Types Reset Sources 2 Reset Sourc | List of Tables |
| Part Selection Guide Block Diagram CPU and Peripheral Overview General Purpose Input/Output Flash Controller 4 Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 5 10-Bit Analog-to-Digital Converter 4 Analog Comparator 7 Timers 1 Interrupt Controller 6 Reset Controller 6 On-Chip Debugger 6 Acronyms and Expansions 6 Pin Description 7 Available Packages 7 Pin Configurations 7 Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File 14 Program Memory 15 Data Memory 16 Flash Information Area 16 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | Overview |
| Block Diagram CPU and Peripheral Overview General Purpose Input/Output Flash Controller Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Register File Program Memory 1 Data Memory 1 Flash Information Area 1 Register Map Reset Types 2 Reset Types 2 Reset Types 2 Reset Types 2 Reset Sources 2 2 | Features |
| CPU and Peripheral Overview General Purpose Input/Output Flash Controller Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File Program Memory Data Memory Flash Information Area Register Map 1 Reset and Stop Mode Recovery Reset Types Reset Types Reset Sources 2 Reset Sources | Part Selection Guide |
| General Purpose Input/Output 4 Flash Controller 4 Nonvolatile Data Storage 5 Internal Precision Oscillator 5 External Crystal Oscillator 6 10-Bit Analog-to-Digital Converter 6 Analog Comparator 7 Timers 7 Interrupt Controller 6 On-Chip Debugger 6 Acronyms and Expansions 6 Pin Description 7 Available Packages 7 Pin Configurations 7 Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File 1 Program Memory 1 Data Memory 1 Flash Information Area 1 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | Block Diagram |
| Flash Controller 4 Nonvolatile Data Storage 1 Internal Precision Oscillator 2 External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator 2 Timers 3 Interrupt Controller 4 Reset Controller 6 On-Chip Debugger 6 Acronyms and Expansions 6 Pin Description 7 Available Packages 7 Pin Configurations 1 Signal Descriptions 1 Pin Characteristics 1 Address Space 14 Register File 14 Program Memory 15 Data Memory 10 Flash Information Area 16 Register Map 17 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | CPU and Peripheral Overview |
| Nonvolatile Data Storage Internal Precision Oscillator External Crystal Oscillator 20-Bit Analog-to-Digital Converter Analog Comparator 3-Bit Analog-to-Digital Converter Analog Comparator 3-Bit Analog-to-Digital Converter Analog Comparator 3-Bit Analog-to-Digital Converter Timers 3-Bit Analog-to-Digital Converter Interrupt Controller 3-Bit Analog-to-Digital Converter On-Chip Debugger 3-Bit Acronyms and Expansions Pin Description 3-Bit Analog-to-Digital Converter Available Packages 3-Bit Analog-to-Digital Converter Pin Description 3-Bit Analog-to-Digital Converter Available Packages 3-Bit Analog-to-Digital Converter Pin Description 3-Bit Analog-to-Digital Converter Available Packages 3-Bit Analog-to-Digital Converter Pin Description 3-Bit Analog-to-Digital Converter Available Packages 3-Bit Analog-to-Digital Converter Pin Description 3-Bit Analog-to-Digital Converter Acronyms and Expansions 4-Bit Analog-to-Digital Converter Acronyms and Expansions 4-Bit Analog-to-Digital Converter Pin Description 4-Bit Analog-to-Digital Converter | General Purpose Input/Output |
| Internal Precision Oscillator External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions On-Chip Debugger Acronyms and Expansions On-Chip Debugger Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File 14 Program Memory 15 Data Memory 16 Flash Information Area 16 Register Map 17 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 25 | Flash Controller |
| External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 11 Pin Characteristics 12 Address Space Register File Program Memory Data Memory Flash Information Area Register Map Reset and Stop Mode Recovery Reset Types Reset Types Reset Sources 22 Reset Sources 23 | Nonvolatile Data Storage |
| External Crystal Oscillator 10-Bit Analog-to-Digital Converter Analog Comparator Timers Interrupt Controller Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 11 Pin Characteristics 12 Address Space Register File Program Memory Data Memory Flash Information Area Register Map Reset and Stop Mode Recovery Reset Types Reset Types Reset Sources 22 Reset Sources 23 | Internal Precision Oscillator |
| 10-Bit Analog-to-Digital Converter Analog Comparator Timers State of Controller Reset Controller On-Chip Debugger Acronyms and Expansions On-Chip Debugger Pin Description Available Packages Pin Configurations 1 Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File 1 Program Memory 1 Data Memory 1 Flash Information Area 1 Register Map 1 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | |
| Analog Comparator 1 Timers 2 Interrupt Controller 3 Reset Controller 4 On-Chip Debugger 5 Acronyms and Expansions 6 Pin Description 7 Available Packages 7 Pin Configurations 1 Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File 1 Program Memory 1 Data Memory 1 Flash Information Area 1 Register Map 1 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | |
| Timers Interrupt Controller Reset Controller 6 On-Chip Debugger 6 Acronyms and Expansions 6 Pin Description 7 Available Packages 7 Pin Configurations 1 Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File 14 Program Memory 12 Data Memory 16 Flash Information Area 16 Register Map 1 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | |
| Interrupt Controller Reset Controller On-Chip Debugger On-Chip Debugger Acronyms and Expansions On-Chip Debugger Acronyms and Expansions On-Chip Debugger Pin Description Available Packages Pin Configurations 1 Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File 1 Program Memory 1 Data Memory 1 Flash Information Area 1 Register Map 1 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | |
| Reset Controller On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File Program Memory Data Memory 1 Flash Information Area 1 Register Map 1 Reset and Stop Mode Recovery Reset Types Reset Sources 2 Reset Sources 2 2 Reset Sources 2 2 2 2 2 3 3 4 3 4 4 5 6 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 | |
| On-Chip Debugger Acronyms and Expansions Pin Description Available Packages Pin Configurations Signal Descriptions 1 Pin Characteristics 1 Address Space 14 Register File 14 Program Memory 15 Data Memory 16 Flash Information Area 16 Register Map 17 Reset and Stop Mode Recovery Reset Types 2 Reset Sources 22 | |
| Acronyms and Expansions 6 Pin Description 7 Available Packages 7 Pin Configurations 1 Signal Descriptions 1 Pin Characteristics 1 Address Space 1 Register File 1 Program Memory 1 Data Memory 1 Flash Information Area 1 Register Map 1 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | |
| Pin Description Available Packages Pin Configurations Signal Descriptions Pin Characteristics 12 Address Space Register File Program Memory Data Memory Flash Information Area 16 Register Map 17 Reset and Stop Mode Recovery Reset Types Reset Sources 22 Reset Sources 23 | |
| Available Packages Pin Configurations Signal Descriptions Pin Characteristics 1 Address Space Register File Program Memory Data Memory Flash Information Area 1 Register Map 1 Reset and Stop Mode Recovery Reset Types Reset Sources 2 2 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 | • |
| Pin Configurations7Signal Descriptions1Pin Characteristics1Address Space14Register File12Program Memory15Data Memory16Flash Information Area16Register Map17Reset and Stop Mode Recovery2Reset Types2Reset Sources2 | |
| Signal Descriptions1Pin Characteristics1Address Space14Register File14Program Memory15Data Memory16Flash Information Area16Register Map17Reset and Stop Mode Recovery2Reset Types2Reset Sources2 | <u> </u> |
| Pin Characteristics15Address Space14Register File14Program Memory15Data Memory16Flash Information Area16Register Map17Reset and Stop Mode Recovery2Reset Types2Reset Sources2 | |
| Address Space 12 Register File 12 Program Memory 15 Data Memory 16 Flash Information Area 16 Register Map 17 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | 7 |
| Register File 14 Program Memory 15 Data Memory 16 Flash Information Area 16 Register Map 17 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | Pin Characteristics |
| Register File 14 Program Memory 15 Data Memory 16 Flash Information Area 16 Register Map 17 Reset and Stop Mode Recovery 2 Reset Types 2 Reset Sources 2 | Address Space |
| Data Memory 10 Flash Information Area 110 Register Map 117 Reset and Stop Mode Recovery 21 Reset Types 22 Reset Sources 22 | Register File |
| Flash Information Area | Program Memory |
| Flash Information Area | Data Memory |
| Reset and Stop Mode Recovery | |
| Reset Types | Register Map |
| Reset Types | Reset and Stop Mode Recovery |
| Reset Sources | |
| | ** |
| | |

PS025113-1212 Table of Contents

| Electrical Characteristics | 184 |
|---|-------------|
| Absolute Maximum Ratings | 184 |
| DC Characteristics | 185 |
| AC Characteristics | 189 |
| On-Chip Peripheral AC and DC Electrical Characteristics | 190 |
| General Purpose I/O Port Input Data Sample Timing | 195 |
| General Purpose I/O Port Output Timing | 196 |
| On-Chip Debugger Timing | 197 |
| Packaging | 199 |
| Ordering Information | 200 |
| Part Number Suffix Designations | |
| Appendix A. Register Tables | |
| General Purpose RAM | |
| Timer 0 | 208 |
| Analog-to-Digital Converter | 213 |
| Low Power Control | 216 |
| LED Controller | 216 |
| Oscillator Control | 217 |
| Comparator 0 | 218 |
| Interrupt Controller | 218 |
| GPIO Port A | 222 |
| Watchdog Timer | 22 <i>e</i> |
| Trim Bit Control | 228 |
| Flash Memory Controller | 228 |
| Index | 231 |
| Customer Support | 239 |
| | |

PS025113-1212 Table of Contents

The Voltage Brown-Out circuit can be either enabled or disabled during STOP Mode. Operations during STOP Mode is set by the VBO_AO Flash option bit. See the <u>Flash Option Bits</u> chapter on page 124 for information about configuring VBO_AO.

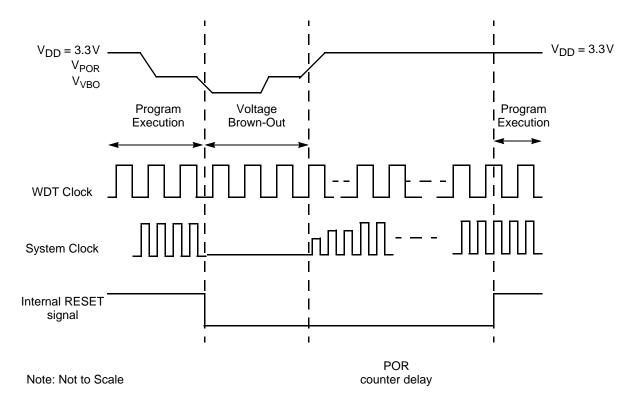


Figure 7. Voltage Brown-Out Reset Operation

Watchdog Timer Reset

If the device is operating in NORMAL or STOP Mode, the Watchdog Timer can initiate a system reset at time-out if the WDT_RES Flash option bit is programmed to 1; this state is the unprogrammed state of the WDT_RES Flash option bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt – not a system reset – at time-out. The WDT status bit in the Reset Status (RSTSTAT) Register is set to 1 to signify that the reset was initiated by the Watchdog Timer.

External Reset Input

The RESET pin has a Schmitt-triggered input and an internal pull-up resistor. After the \overline{RESET} pin is asserted for a minimum of four system clock cycles, the device progresses through the system reset sequence. Because of the possible asynchronicity of the system

PS025113-1212 Reset Sources

LED Drive Enable Register

The LED Drive Enable Register, shown in Table 31, activates the controlled current drive. The Alternate Function Register has no control over the LED function; therefore, setting the Alternate Function Register to select the LED function is not required. LEDEN bits [7:0] correspond to Port C bits [7:0], respectively.

Table 31. LED Drive Enable (LEDEN)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---------|------------|------|-----|-----|-----|-----|-----|-----|--|--|
| Field | LEDEN[7:0] | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |
| Address | | F82H | | | | | | | | |

| Bit | Description |
|-------|--|
| [7:0] | LED Drive Enable |
| LEDEN | These bits determine which Port C pins are connected to an internal current sink. 0 = Tristate the Port C pin. 1= Connect controlled current sink to the Port C pin. |

LED Drive Level High Register

The LED Drive Level High Register, shown in Table 32, contains two control bits for each Port C pin. These two bits select one of four programmable current drive levels for each Port C pin. Each pin is individually programmable.

Table 32. LED Drive Level High Register (LEDLVLH)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------|--------------|------|-----|-----|-----|-----|-----|-----|--|
| Field | LEDLVLH[7:0] | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Address | | F83H | | | | | | | |

| Bit | Description |
|---------|--|
| [7:0] | LED Level High Bits |
| LEDLVLH | I {LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin. |
| | 00 = 3 mA. |
| | 01= 7 mA. |
| | 10= 13mA. |
| | 11= 20 mA. |

Interrupt Edge Select Register

The interrupt edge select (IRQES) register determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A or Port D input pin. See Table 47.

Table 47. Interrupt Edge Select Register (IRQES)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
|---------|------|------|------|------|------|------|------|------|--|--|--|
| Field | IES7 | IES6 | IES5 | IES4 | IES3 | IES2 | IES1 | IES0 | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | | |
| Address | | FCDH | | | | | | | | | |

| Bit | Description |
|--------------|--|
| [7] | Interrupt Edge Select x |
| IES <i>x</i> | 0 = An interrupt request is generated on the falling edge of the PAx input or PDx. |
| | 1 = An interrupt request is generated on the rising edge of the PAx input or PDx . |
| Note: | x indicates register bits in the address range 7–0. |

- Disable the timer
- Configure the timer for CONTINUOUS Mode
- Set the prescale value
- If using the timer output Alternate function, set the initial output level (High or Low)
- 2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H). This action only affects the first pass in CONTINUOUS Mode. After the first timer reload in CONTINUOUS Mode, counting always begins at the reset value of 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. Enable the timer interrupt (if appropriate) and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. Configure the associated GPIO port pin (if using the timer output function) for the timer output alternate function.
- 6. Write to the Timer Control Register to enable the timer and initiate counting.

In CONTINUOUS Mode, the system clock always provides the timer input. The timer period is calculated with the following equation:

Continuous Mode Time-Out Period (s) =
$$\frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first time-out period.

COUNTER Mode

In COUNTER Mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO port pin: timer input alternate function. The TPOL bit in the Timer Control Register determines whether the count occurs on the rising edge or the falling edge of the timer input signal. In COUNTER Mode, the prescaler is disabled.

Caution: The input frequency of the timer input signal must not exceed one-fourth the system clock frequency.

Upon reaching the reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Additionally, if the timer output alternate function

PS025113-1212 Operation

- 4. Enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. If using the timer output function, configure the associated GPIO port pin for the timer output alternate function.
- 6. Write to the Timer Control Register to enable the timer and initiate counting.

In COMPARE Mode, the system clock always provides the timer input. The compare time can be calculated by the following equation:

Compare Mode Time (s) =
$$\frac{(Compare \ Value - Start \ Value) \times Prescale}{System \ Clock \ Frequency \ (Hz)}$$

GATED Mode

In GATED Mode, the timer counts only when the timer input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control Register. When the timer input signal is asserted, counting begins. A timer interrupt is generated when the timer input signal is deasserted or a timer reload occurs. To determine whether the timer input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the timer input signal remains asserted). Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) at timer reset.

Observe the following steps for configuring a timer for GATED Mode and for initiating the count:

- 1. Write to the Timer Control Register to:
 - Disable the timer
 - Configure the timer for GATED Mode
 - Set the prescale value
- 2. Write to the Timer High and Low Byte registers to set the starting count value. Writing these registers only affects the first pass in GATED Mode. After the first timer reset in GATED Mode, counting always begins at the reset value of 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. Enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input deasser-

PS025113-1212 Operation

- 6. Write to the Timer Control Register to enable the timer.
- 7. Counting begins on the first appropriate transition of the timer input signal. No interrupt is generated by the first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to capture event can be calculated using the following equation:

Capture Elapsed Time (s) =
$$\frac{\text{(Capture Value - Start Value)} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on Timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the timer low byte register are placed in a holding register. A subsequent read from the timer low byte register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value when enabled. When the timers are not enabled, a read from the timer low byte register returns the actual value in the counter.

Timer Pin Signal Operation

Timer output is a GPIO port pin alternate function. The timer output is toggled every time the counter is reloaded.

The timer input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO alternate function registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT Mode. For this mode, no timer input is available.

PS025113-1212 Operation

Timer Control Register Definitions

This section defines the features of the following Timer Control registers.

<u>Timer 0–1 High and Low Byte Registers</u>: see page 83

Timer Reload High and Low Byte Registers: see page 85

<u>Timer 0–1 PWM High and Low Byte Registers</u>: see page 86

Timer 0–1 Control Registers: see page 87

Timer 0-1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers, shown in Tables 50 and 51, contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register content when the timer is enabled; however, when the timer is disabled, a read from the TxL reads the TxL Register content directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations; therefore, simultaneous 16-bit writes are not possible. If either the timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low byte) at the next clock edge. The counter continues counting from the new value.

Table 50. Timer 0–1 High Byte Register (TxH)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---------|-----|------------|-----|-----|-----|-----|-----|-----|--|--|
| Field | TH | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | |
| Address | | F00H, F08H | | | | | | | | |

Table 51. Timer 0–1 Low Byte Register (TxL)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|---------|------------|-----|-----|-----|-----|-----|-----|-----|--|
| Field | TL | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | |
| Address | F01H, F09H | | | | | | | | |

Flash Option Bits

Programmable Flash option bits allow user configuration of certain aspects of Z8 Encore! F0830 Series operation. The feature configuration data is stored in the Flash program memory and read during reset. The features available for control through the Flash option bits are:

- Watchdog Timer time-out response selection–interrupt or system reset
- Watchdog Timer enabled at reset
- The ability to prevent unwanted read access to user code in program memory
- The ability to prevent accidental programming and erasure of all or a portion of the user code in program memory
- Voltage Brown-Out configuration always enabled or disabled during STOP Mode to reduce STOP Mode power consumption
- OSCILLATOR Mode selection for high, medium and low power crystal oscillators or external RC oscillator
- Factory trimming information for the Internal Precision Oscillator and VBO voltage

Operation

This section describes the type and configuration of the programmable Flash option bits.

Option Bit Configuration by Reset

Each time the Flash option bits are programmed or erased, the device must be reset for the change to be effective. During any Reset operation (system reset or Stop Mode Recovery), the Flash option bits are automatically read from Flash program memory and written to the Option Configuration registers, which control Z8 Encore! F0830 Series device operation. Option bit control is established before the device exits reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the register file and are not accessible for read or write access.

PS025113-1212 Flash Option Bits

Note: The bit values used in Table 85 are set at the factory; no calibration is required.

Table 86. Trim Option Bits at 0002H (TIPO)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | |
|---|-------------------------------|-----|---|---|---|---|---|---|--|--|
| Field | IPO_TRIM | | | | | | | | | |
| RESET | | U | | | | | | | | |
| R/W | | R/W | | | | | | | | |
| Address | Information Page Memory 0022H | | | | | | | | | |
| Note: U = Unchanged by Reset. R/W = Read/Write. | | | | | | | | | | |

| Bit | Description |
|----------|---|
| [7:0] | Internal Precision Oscillator Trim Byte |
| IPO_TRIM | Contains trimming bits for the Internal Precision Oscillator. |

Note: The bit values used in Table 86 are set at the factory; no calibration is required.

Table 87. Trim Option Bits at 0003H (TVBO)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 0 | | |
|-----------|---|------|-------|---|----------|----------|-----|---|--|
| Field | | Rese | erved | | Reserved | VBO_TRIM | | | |
| RESET | | l | J | | U | 1 | 0 | 0 | |
| R/W | | R | W | | R/W | | R/W | | |
| Address | Information Page Memory 0023H | | | | | | | | |
| Note: U = | Note: U = Unchanged by Reset. R/W = Read/Write. | | | | | | | | |

| Bit | Description |
|----------|---|
| [7:3] | Reserved |
| | These bits are reserved and must be programmed to 11111. |
| [2] | VBO Trim Values |
| VBO_TRIM | Contains factory-trimmed values for the oscillator and the VBO. |

Nonvolatile Data Storage

Z8 Encore! F0830 Series devices contain a Nonvolatile Data Storage (NVDS) element of up to 64 bytes (except when in Flash 12KB mode). This type of memory can perform over 100,000 write cycles.

Operation

NVDS is implemented by special-purpose Zilog software stored in areas of program memory that are not user-accessible. These special-purpose routines use Flash memory to store the data, and incorporate a dynamic addressing scheme to maximize the write/erase endurance of the Flash.

Note:

The products in the Z8 Encore! F0830 Series feature multiple NVDS array sizes. See the Z8 Encore! F0830 Series Family Part Selection Guide section on page 2 for details.

NVDS Code Interface

Two routines are required to access the NVDS: a write routine and a read routine. Both of these routines are accessed with a CALL instruction to a predefined address outside of program memory that is accessible to the user. Both the NVDS address and data are single-byte values. In order to not disturb the user code, these routines save the working register set before using it so that 16 bytes of stack space are required to preserve the site. After finishing the call to these routines, the working register set of the user code is recovered.

During both read and write accesses to the NVDS, interrupt service is not disabled. Any interrupts that occur during NVDS execution must not disturb the working register and existing stack contents; otherwise, the array can become corrupted. Zilog recommends the user disable interrupts before executing NVDS operations.

Use of the NVDS requires 16 bytes of available stack space. The contents of the working register set are saved before calling NVDS read or write routines.

For correct NVDS operation, the Flash Frequency registers must be programmed based on the system clock frequency. See *the* Flash Operation Timing Using the Flash Frequency Registers section on page 114.

This example indicates that the source data is added to the destination data; the result is stored in the destination location.

eZ8 CPU Instruction Classes

eZ8 CPU instructions can be divided functionally into the following groups:

- Arithmetic
- Bit manipulation
- Block transfer
- CPU control
- Load
- Logical
- Program control
- Rotate and shift

Tables 105 through 112 contain the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table as these instructions can be considered as a subset of more than one category. Within these tables, the source operand is identified as *src*, the destination operand is *dst* and a condition code is *cc*.

Table 105. Arithmetic Instructions

| Mnemonic | Operands | Instruction |
|----------|----------|--|
| ADC | dst, src | Add with Carry |
| ADCX | dst, src | Add with Carry using Extended Addressing |
| ADD | dst, src | Add |
| ADDX | dst, src | Add using Extended Addressing |
| СР | dst, src | Compare |
| CPC | dst, src | Compare with Carry |
| CPCX | dst, src | Compare with Carry using Extended Addressing |
| СРХ | dst, src | Compare using Extended Addressing |
| DA | dst | Decimal Adjust |
| DEC | dst | Decrement |
| DECW | dst | Decrement Word |
| INC | dst | Increment |

Table 113. eZ8 CPU Instruction Summary (Continued)

| Assembly | | | ress ode | Op Code(s) | | | Fla | ags | | | _ Fetch | Instr. |
|---------------|-------------------------------------|-----|-------------|---------------|---|---|-----|-----|---|---|---------|--------|
| Mnemonic | Symbolic Operation | dst | src | (Hex) | С | Z | S | ٧ | D | Н | | Cycles |
| SRA dst | | R | | D0 | * | * | * | 0 | _ | _ | 2 | 2 |
| | D7 D6 D5 D4 D3 D2 D1 D0 C | IR | | D1 | _ | | | | | | 2 | 3 |
| SRL dst | 0 - D7 D6 D5 D4 D3 D2 D1 D0 C | R | | 1F C0 | * | * | 0 | * | _ | _ | 3 | 2 |
| | dst | IR | | 1F C1 | _ | | | | | | 3 | 3 |
| SRP src | RP ← src | | IM | 01 | _ | - | - | - | - | - | 2 | 2 |
| STOP | STOP Mode | | | 6F | _ | _ | _ | - | - | _ | 1 | 2 |
| SUB dst, src | dst ← dst – src | r | r | 22 | * | * | * | * | 1 | * | 2 | 3 |
| | - | r | lr | 23 | _ | | | | | | 2 | 4 |
| | - | R | R | 24 | _ | | | | | | 3 | 3 |
| | - - | R | IR | 25 | _ | | | | | | 3 | 4 |
| | - | R | IM | 26 | _ | | | | | | 3 | 3 |
| | - | IR | IM | 27 | _ | | | | | | 3 | 4 |
| SUBX dst, src | dst ← dst – src | ER | ER | 28 | * | * | * | * | 1 | * | 4 | 3 |
| | | ER | IM | 29 | _ | | | | | | 4 | 3 |
| SWAP dst | $dst[7:4] \leftrightarrow dst[3:0]$ | R | | F0 | Χ | * | * | Χ | - | _ | 2 | 2 |
| | - | IR | | F1 | _ | | | | | | 2 | 3 |
| TCM dst, src | (NOT dst) AND src | r | r | 62 | - | * | * | 0 | - | - | 2 | 3 |
| | | r | lr | 63 | _ | | | | | | 2 | 4 |
| | | R | R | 64 | _ | | | | | | 3 | 3 |
| | - | R | IR | 65 | _ | | | | | | 3 | 4 |
| | - | R | IM | 66 | | | | | | | 3 | 3 |
| | | IR | IM | 67 | | | | | | | 3 | 4 |
| TCMX dst, src | (NOT dst) AND src | ER | ER | 68 | _ | * | * | 0 | - | - | 4 | 3 |
| | | ER | IM | 69 | | | | | | | 4 | 3 |

Note: Flags Notation:

^{* =} Value is a function of the result of the operation.

⁻ = Unaffected.

X = Undefined.

^{0 =} Reset to 0.

^{1 =} Set to 1.

DC Characteristics

Table 116 lists the DC characteristics of the Z8 Encore! F0830 Series products. All voltages are referenced to V_{SS} , the primary system ground.

Table 116. DC Characteristics

| | | $T_A = 0$ | °C to - | ⊦70°C | $T_A = -4$ | 0°C to | +105°C | | |
|------------------|------------------------------|-----------|---------|-------|------------|--------|---------------------|-------|--|
| Symbol | Parameter | Min | Тур | Max | Min | Тур | Max | Units | Conditions |
| V _{DD} | Supply Voltage | | | | 2.7 | _ | 3.6 | V | Power supply noise not to exceed 100 mV peak to peak |
| V _{IL1} | Low Level Input Voltage | | | | -0.3 | - | 0.3*V _D | V | For all input pins except RESET. |
| V_{IL2} | Low Level Input Voltage | | | | -0.3 | - | 8.0 | V | For RESET. |
| V _{IH1} | High Level Input Voltage | | | | 2.0 | _ | 5.5 | V | For all input pins without analog or oscillator function. |
| V _{IH2} | High Level Input Voltage | | | | 2.0 | - | V _{DD} +0. | V | For those pins with analog or oscillator function. |
| V _{OL1} | Low Level Output Voltage | | | | - | _ | 0.4 | V | I_{OL} = 2mA; V_{DD} = 3.0V High Output Drive disabled. |
| V _{OH1} | High Level Output Voltage | | | | 2.4 | _ | - | V | $I_{OH} = -2$ mA; $V_{DD} = 3.0$ V High Output Drive disabled. |
| V _{OL2} | Low Level Output Voltage | | | | - | _ | 0.6 | V | I_{OL} = 20 mA; V_{DD} = 3.3 V High Output Drive enabled. |
| V _{OH2} | High Level Output Voltage | | | | 2.4 | - | - | V | $I_{OH} = -20 \text{ mA};$ $V_{DD} = 3.3 \text{ V}$ High Output Drive enabled. |
| I _{IL} | Input Leakage Current | | | | -5 | _ | +5 | μΑ | $V_{DD} = 3.6 \text{ V};$ $V_{IN} = V_{DD} \text{ or } V_{SS}^{1}$ |
| I _{TL} | Tristate Leakage Current | | | | - 5 | - | +5 | μΑ | V _{DD} = 3.6 V |

Notes:

- 1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
- 2. These values are provided for design guidance only and are not tested in production.
- 3. See Figure 31 for HALT Mode current.

PS025113-1212 DC Characteristics

Appendix A. Register Tables

For the reader's convenience, this appendix lists all F0830 Series registers numerically by hexadecimal address.

General Purpose RAM

In the F0830 Series, the 000-EFF hexadecimal address range is partitioned for general-purpose random access memory, as follows.

Hex Addresses: 000-0FF

This address range is reserved for general-purpose register file RAM. For more details, see the <u>Register File</u> section on page 14.

Hex Addresses: 100-EFF

This address range is reserved.

Timer 0

For more information about these Timer Control registers, see the <u>Timer Control Register</u> <u>Definitions</u> section on page 83.

Hex Address: F00

Table 130. Timer 0 High Byte Register (T0H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | |
|---------|-----|-----|-----|-----|-----|-----|-----|-----|--|--|--|
| Field | | TH | | | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | | | |
| Address | | | | F0 | 0H | | | | | | |

Hex Address: F71

This address range is reserved.

Hex Address: F72

Table 147. ADC Data High Byte Register (ADCD_H)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | | | | |
|---------|---|-------|---|----|----|---|---|---|--|--|--|--|
| Field | | ADCDH | | | | | | | | | | |
| RESET | | | |) | < | | | | | | | |
| R/W | | R | | | | | | | | | | |
| Address | | | | F7 | 2H | | | | | | | |

| Bit | Description |
|-------|---|
| [7:0] | ADC High Byte 00h–FFh = The last conversion output is held in the data registers until the next ADC conversion is completed. |

Hex Address: F73

Table 148. ADC Data Low Bits Register (ADCD_L)

| Bit | 7 | 6 | 5 | 5 4 3 2 1 0 | | | | | | |
|---------|-----|-----|----------|-------------|----|---|--|--|--|--|
| Field | ADO | CDL | Reserved | | | | | | | |
| RESET |) | < | | |) | < | | | | |
| R/W | F | ₹ | | R | | | | | | |
| Address | | | | F7 | 3H | | | | | |

| Bit Position | Description |
|-----------------|--|
| [7:6] | ADC Low Bits 00–11b = These bits are the two least significant bits of the 10-bit ADC output. These bits are undefined after a reset. The low bits are latched into this register whenever the ADC Data High Byte Register is read. |
| [5:0] | Reserved These bits are reserved and must be programmed to 000000. |

Hex Address: FDF

Table 183. Port D Output Data Register (PDOUT)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|-------|-------|-------|-------|-------|-------|-------|-------|
| Field | POUT7 | POUT6 | POUT5 | POUT4 | POUT3 | POUT2 | POUT1 | POUT0 |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | | | | FD | FH | | | |

Hex Addresses: FE0-FEF

This address range is reserved.

Watchdog Timer

For more information about the Watchdog Timer registers, see the <u>Watchdog Timer Control Register Definitions</u> section on page 95.

Hex Address: FF0

The Watchdog Timer Control Register address is shared with the read-only Reset Status Register.

Table 184. Watchdog Timer Control Register (WDTCTL)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|---|---|---|---|---|---|---|
| Field | WDTUNLK | | | | | | | |
| RESET | Х | Х | Х | Х | Х | Х | Х | Х |
| R/W | W | W | W | W | W | W | W | W |
| Address | FF0H | | | | | | | |

Table 185. Reset Status Register (RSTSTAT)

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|--------------------------------|------|-----|-----|---|------|-------|---|
| Field | POR | STOP | WDT | EXT | | Rese | erved | |
| RESET | See <u>Table 12</u> on page 29 | | | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R |
| Address | FF0H | | | | | | | |

PS025113-1212 Watchdog Timer

| compare - extended addressing 166 | E |
|--|---|
| compare mode 89 | EI 168 |
| compare with carry 166 | electrical characteristics 184 |
| compare with carry - extended addressing 166 | GPIO input data sample timing 195 |
| complement 169 | watch-dog timer 194 |
| complement carry flag 167, 168 | electrical noise 98 |
| condition code 164 | enable interrupt 168 |
| continuous mode 89 | ER 164 |
| Control Registers 14, 17 | extended addressing register 164 |
| counter modes 89 | external pin reset 25 |
| CP 166 | eZ8 CPU features 4 |
| CPC 166 | eZ8 CPU instruction classes 166 |
| CPCX 166 | eZ8 CPU instruction notation 164 |
| CPU and peripheral overview 4 | eZ8 CPU instruction set 162 |
| CPU control instructions 168 | eZ8 CPU instruction summary 171 |
| CPX 166 | 626 CT C Instruction summary 171 |
| current measurement | |
| architecture 98 | F |
| operation 99 | FCTL register 119, 126, 127, 228 |
| Customer Feedback Form 239 | features, Z8 Encore! 1 |
| Customer Information 239 | first opcode map 182 |
| | FLAGS 165 |
| | flags register 165 |
| D | flash |
| DA 164, 166 | controller 4 |
| data memory 16 | option bit address space 127 |
| DC characteristics 185 | option bit address space 127 option bit configuration - reset 124 |
| debugger, on-chip 139 | program memory address 0000H 127 |
| DEC 166 | program memory address 0001H 128 |
| decimal adjust 166 | flash memory 108 |
| decrement 166 | byte programming 116 |
| decrement and jump non-zero 169 | code protection 114 |
| decrement word 166 | configurations 108 |
| DECW 166 | control register definitions 118, 126 |
| destination operand 165 | controller bypass 117 |
| device, port availability 33 | flash control register 119, 126, 127, 228 |
| DI 168 | flash option bits 115 |
| direct address 164 | flash status register 120 |
| disable interrupts 168 | flow chart 113 |
| DJNZ 169 | frequency high and low byte registers 123 |
| dst 165 | mass erase 117 |
| | operation 112 |
| | operation timing 114 |
| | page erase 117 |
| | page crase 117 |

| JP 169 | interrupt control register 67 |
|----------------------------------|--|
| LD 168 | interrupt controller 53 |
| LDC 168 | architecture 53 |
| LDCI 167, 168 | interrupt assertion types 56 |
| LDE 168 | interrupt vectors and priority 56 |
| LDEI 167 | operation 55 |
| LDX 168 | register definitions 57 |
| LEA 168 | software interrupt assertion 57 |
| load 168 | interrupt edge select register 65 |
| logical 169 | interrupt request 0 register 58 |
| MULT 167 | interrupt request 1 register 59 |
| NOP 168 | interrupt request 2 register 60 |
| OR 169 | interrupt return 169 |
| ORX 169 | interrupt vector listing 53 |
| POP 168 | IR 164 |
| POPX 168 | Ir 164 |
| program control 169 | IRET 169 |
| PUSH 168 | IRQ0 enable high and low bit registers 60 |
| PUSHX 168 | IRQ1 enable high and low bit registers 62 |
| RCF 167, 168 | IRQ2 enable high and low bit registers 63 |
| RET 169 | IRR 164 |
| RL 169 | Irr 164 |
| RLC 169 | |
| rotate and shift 169 | |
| RR 170 | J |
| RRC 170 | JP 169 |
| SBC 167 | jump, conditional, relative, and relative conditional |
| SCF 167, 168 | 169 |
| SRA 170 | 10) |
| SRL 170 | |
| SRP 168 | L |
| STOP 168 | LD 168 |
| SUB 167 | LDC 168 |
| SUBX 167 | LDC 108 LDCI 167, 168 |
| SWAP 170 | LDE 168 |
| TCM 167 | |
| TCMX 167 | LDEI 167, 168 LDX 168 |
| TM 167 | LEA 168 |
| TMX 167 | load 168 |
| TRAP 169 | load constant 167 |
| watch-dog timer refresh 168 | |
| XOR 169 | load constant to/from program memory 168 load constant with auto-increment addresses 168 |
| XORX 169 | load effective address 168 |
| instructions, eZ8 classes of 166 | load external data 168 |
| · | IUAU EXIELIAI UAIA 194 |