Welcome to E-XFL.COM

What is "**Embedded - Microcontrollers**"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0430pj020sg

Table of Contents

The Voltage Brown-Out circuit can be either enabled or disabled during STOP Mode. Operations during STOP Mode is set by the VBO_AO Flash option bit. See the Flash Option Bits chapter on page 124 for information about configuring VBO_AO.
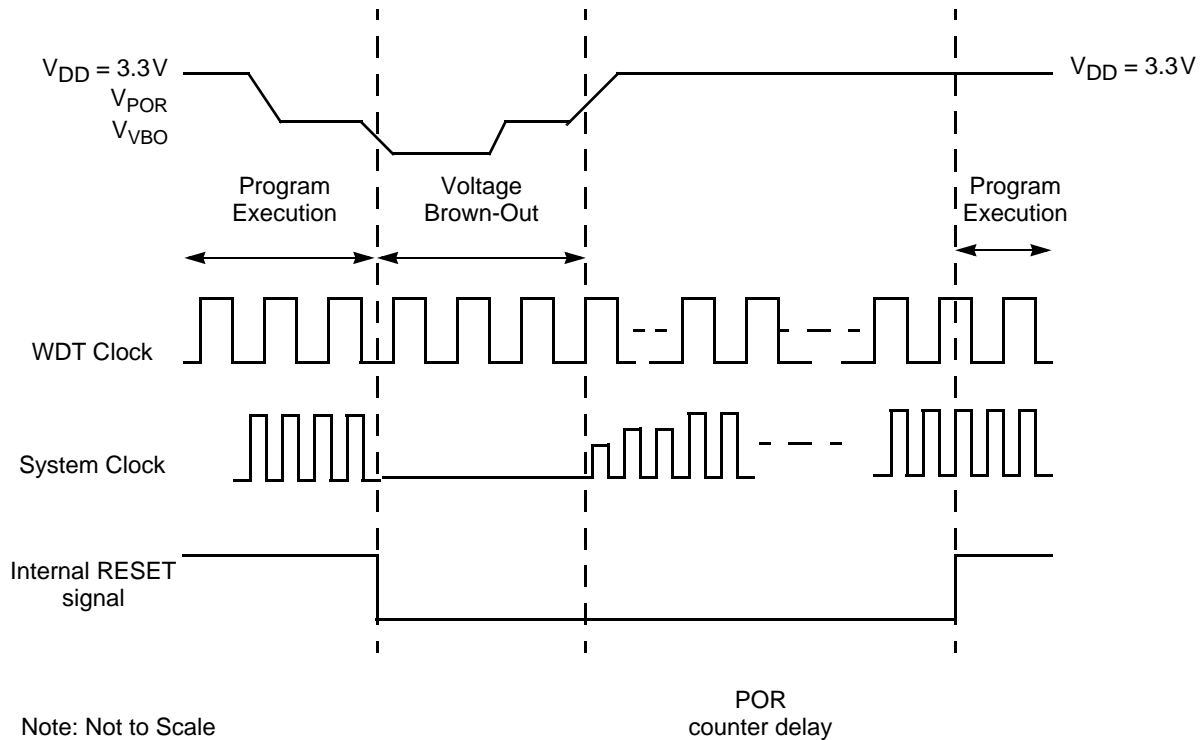
Figure 7. Voltage Brown-Out Reset Operation

Watchdog Timer Reset

If the device is operating in NORMAL or STOP Mode, the Watchdog Timer can initiate a system reset at time-out if the WDT_RES Flash option bit is programmed to 1; this state is the unprogrammed state of the WDT_RES Flash option bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt – not a system reset – at time-out. The WDT status bit in the Reset Status (RSTSTAT) Register is set to 1 to signify that the reset was initiated by the Watchdog Timer.

External Reset Input

The $\overline{\text{RESET}}$ pin has a Schmitt-triggered input and an internal pull-up resistor. After the $\overline{\text{RESET}}$ pin is asserted for a minimum of four system clock cycles, the device progresses through the system reset sequence. Because of the possible asynchronicity of the system

LED Drive Enable Register

The LED Drive Enable Register, shown in Table 31, activates the controlled current drive. The Alternate Function Register has no control over the LED function; therefore, setting the Alternate Function Register to select the LED function is not required. LEDEN bits [7:0] correspond to Port C bits [7:0], respectively.

Table 31. LED Drive Enable (LEDEN)

Bit	7	6	5	4	3	2	1	0
Field	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F82H							

Bit	Description
[7:0] LEDEN	**LED Drive Enable** These bits determine which Port C pins are connected to an internal current sink. 0 = Tristate the Port C pin. 1= Connect controlled current sink to the Port C pin.

LED Drive Level High Register

The LED Drive Level High Register, shown in Table 32, contains two control bits for each Port C pin. These two bits select one of four programmable current drive levels for each Port C pin. Each pin is individually programmable.

Table 32. LED Drive Level High Register (LEDLVLH)

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F83H							

Bit	Description
[7:0] LEDLVLH	**LED Level High Bits** {LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin. 00 = 3mA. 01= 7mA. 10= 13mA. 11= 20mA.

Interrupt Edge Select Register

The interrupt edge select (IRQES) register determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A or Port D input pin. See Table 47.

Table 47. Interrupt Edge Select Register (IRQES)

Bit	7	6	5	4	3	2	1	0
Field	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCDH							

Bit	Description
[7] IESx	**Interrupt Edge Select x** 0 = An interrupt request is generated on the falling edge of the PAx input or PDx. 1 = An interrupt request is generated on the rising edge of the PAx input or PDx.
Note:	x indicates register bits in the address range 7–0.

 – Disable the timer

 – Configure the timer for CONTINUOUS Mode

 – Set the prescale value

 – If using the timer output Alternate function, set the initial output level (High or Low)

2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H). This action only affects the first pass in CONTINUOUS Mode. After the first timer reload in CONTINUOUS Mode, counting always begins at the reset value of 0001H.

3. Write to the Timer Reload High and Low Byte registers to set the reload value.

4. Enable the timer interrupt (if appropriate) and set the timer interrupt priority by writing to the relevant interrupt registers.

5. Configure the associated GPIO port pin (if using the timer output function) for the timer output alternate function.

6. Write to the Timer Control Register to enable the timer and initiate counting.

In CONTINUOUS Mode, the system clock always provides the timer input. The timer period is calculated with the following equation:

$$\text{Continuous Mode Time-Out Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first time-out period.

COUNTER Mode

In COUNTER Mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO port pin: timer input alternate function. The TPOL bit in the Timer Control Register determines whether the count occurs on the rising edge or the falling edge of the timer input signal. In COUNTER Mode, the prescaler is disabled.

! **Caution:** The input frequency of the timer input signal must not exceed one-fourth the system clock frequency.

Upon reaching the reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Additionally, if the timer output alternate function

4.   Enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.

5.   If using the timer output function, configure the associated GPIO port pin for the timer output alternate function.

6.   Write to the Timer Control Register to enable the timer and initiate counting.

In COMPARE Mode, the system clock always provides the timer input. The compare time can be calculated by the following equation:

$$\text{Compare Mode Time (s)} = \frac{(\text{Compare Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

GATED Mode

In GATED Mode, the timer counts only when the timer input signal is in its active state (asserted), as determined by the TPOL bit in the Timer Control Register. When the timer input signal is asserted, counting begins. A timer interrupt is generated when the timer input signal is deasserted or a timer reload occurs. To determine whether the timer input signal deassertion generated the interrupt, read the associated GPIO input value and compare to the value stored in the TPOL bit.

The timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes (assuming the timer input signal remains asserted). Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) at timer reset.

Observe the following steps for configuring a timer for GATED Mode and for initiating the count:

1.   Write to the Timer Control Register to:
     –   Disable the timer
     –   Configure the timer for GATED Mode
     –   Set the prescale value

2.   Write to the Timer High and Low Byte registers to set the starting count value. Writing these registers only affects the first pass in GATED Mode. After the first timer reset in GATED Mode, counting always begins at the reset value of 0001H.

3.   Write to the Timer Reload High and Low Byte registers to set the reload value.

4.   Enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input deasser-

6. Write to the Timer Control Register to enable the timer.

7. Counting begins on the first appropriate transition of the timer input signal. No interrupt is generated by the first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on Timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the timer low byte register are placed in a holding register. A subsequent read from the timer low byte register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value when enabled. When the timers are not enabled, a read from the timer low byte register returns the actual value in the counter.

Timer Pin Signal Operation

Timer output is a GPIO port pin alternate function. The timer output is toggled every time the counter is reloaded.

The timer input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO alternate function registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT Mode. For this mode, no timer input is available.

Timer Control Register Definitions

This section defines the features of the following Timer Control registers.

Timer 0–1 High and Low Byte Registers: see page 83

Timer Reload High and Low Byte Registers: see page 85

Timer 0–1 PWM High and Low Byte Registers: see page 86

Timer 0–1 Control Registers: see page 87

Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers, shown in Tables 50 and 51, contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register content when the timer is enabled; however, when the timer is disabled, a read from the TxL reads the TxL Register content directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations; therefore, simultaneous 16-bit writes are not possible. If either the timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low byte) at the next clock edge. The counter continues counting from the new value.

Table 50. Timer 0–1 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H, F08H							

Table 51. Timer 0–1 Low Byte Register (TxL)

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H, F09H							

Flash Option Bits

Programmable Flash option bits allow user configuration of certain aspects of Z8 Encore! F0830 Series operation. The feature configuration data is stored in the Flash program memory and read during reset. The features available for control through the Flash option bits are:

- Watchdog Timer time-out response selection–interrupt or system reset

- Watchdog Timer enabled at reset

- The ability to prevent unwanted read access to user code in program memory

- The ability to prevent accidental programming and erasure of all or a portion of the user code in program memory

- Voltage Brown-Out configuration always enabled or disabled during STOP Mode to reduce STOP Mode power consumption

- OSCILLATOR Mode selection for high, medium and low power crystal oscillators or external RC oscillator

- Factory trimming information for the Internal Precision Oscillator and VBO voltage

Operation

This section describes the type and configuration of the programmable Flash option bits.

Option Bit Configuration by Reset

Each time the Flash option bits are programmed or erased, the device must be reset for the change to be effective. During any Reset operation (system reset or Stop Mode Recovery), the Flash option bits are automatically read from Flash program memory and written to the Option Configuration registers, which control Z8 Encore! F0830 Series device operation. Option bit control is established before the device exits reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the register file and are not accessible for read or write access.

> **Note:** The bit values used in Table 85 are set at the factory; no calibration is required.

Table 86. Trim Option Bits at 0002H (TIPO)

Bit	7	6	5	4	3	2	1	0
Field	IPO_TRIM							
RESET	U							
R/W	R/W							
Address	Information Page Memory 0022H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:0] IPO_TRIM	**Internal Precision Oscillator Trim Byte** Contains trimming bits for the Internal Precision Oscillator.

> **Note:** The bit values used in Table 86 are set at the factory; no calibration is required.

Table 87. Trim Option Bits at 0003H (TVBO)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				Reserved	VBO_TRIM		
RESET	U				U	1	0	0
R/W	R/W				R/W	R/W		
Address	Information Page Memory 0023H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7:3]	**Reserved** These bits are reserved and must be programmed to 11111.
[2] VBO_TRIM	**VBO Trim Values** Contains factory-trimmed values for the oscillator and the VBO.

Nonvolatile Data Storage

Z8 Encore! F0830 Series devices contain a Nonvolatile Data Storage (NVDS) element of up to 64 bytes (except when in Flash 12 KB mode). This type of memory can perform over 100,000 write cycles.

Operation

NVDS is implemented by special-purpose Zilog software stored in areas of program memory that are not user-accessible. These special-purpose routines use Flash memory to store the data, and incorporate a dynamic addressing scheme to maximize the write/erase endurance of the Flash.

> **Note:** The products in the Z8 Encore! F0830 Series feature multiple NVDS array sizes. See the Z8 Encore! F0830 Series Family Part Selection Guide section on page 2 for details.

NVDS Code Interface

Two routines are required to access the NVDS: a write routine and a read routine. Both of these routines are accessed with a CALL instruction to a predefined address outside of program memory that is accessible to the user. Both the NVDS address and data are single-byte values. In order to not disturb the user code, these routines save the working register set before using it so that 16 bytes of stack space are required to preserve the site. After finishing the call to these routines, the working register set of the user code is recovered.

During both read and write accesses to the NVDS, interrupt service is not disabled. Any interrupts that occur during NVDS execution must not disturb the working register and existing stack contents; otherwise, the array can become corrupted. Zilog recommends the user disable interrupts before executing NVDS operations.

Use of the NVDS requires 16 bytes of available stack space. The contents of the working register set are saved before calling NVDS read or write routines.

For correct NVDS operation, the Flash Frequency registers must be programmed based on the system clock frequency. See *the* Flash Operation Timing Using the Flash Frequency Registers *section on page 114*.

This example indicates that the source data is added to the destination data; the result is stored in the destination location.

eZ8 CPU Instruction Classes

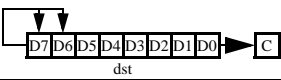eZ8 CPU instructions can be divided functionally into the following groups:

- Arithmetic
- Bit manipulation
- Block transfer
- CPU control
- Load
- Logical
- Program control
- Rotate and shift

Tables 105 through 112 contain the instructions belonging to each group and the number of operands required for each instruction. Some instructions appear in more than one table as these instructions can be considered as a subset of more than one category. Within these tables, the source operand is identified as *src*, the destination operand is *dst* and a condition code is *cc*.

Table 105. Arithmetic Instructions

Mnemonic	Operands	Instruction
ADC	dst, src	Add with Carry
ADCX	dst, src	Add with Carry using Extended Addressing
ADD	dst, src	Add
ADDX	dst, src	Add using Extended Addressing
CP	dst, src	Compare
CPC	dst, src	Compare with Carry
CPCX	dst, src	Compare with Carry using Extended Addressing
CPX	dst, src	Compare using Extended Addressing
DA	dst	Decimal Adjust
DEC	dst	Decrement
DECW	dst	Decrement Word
INC	dst	Increment

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
SRA dst		R		D0	*	*	*	0	–	–	2	2
		IR		D1							2	3
SRL dst		R		1F C0	*	*	0	*	–	–	3	2
		IR		1F C1							3	3
SRP src	RP ← src		IM	01	–	–	–	–	–	–	2	2
STOP	STOP Mode			6F	–	–	–	–	–	–	1	2
SUB dst, src	dst ← dst – src	r	r	22	*	*	*	*	1	*	2	3
		r	Ir	23							2	4
		R	R	24							3	3
		R	IR	25							3	4
		R	IM	26							3	3
		IR	IM	27							3	4
SUBX dst, src	dst ← dst – src	ER	ER	28	*	*	*	*	1	*	4	3
		ER	IM	29							4	3
SWAP dst	dst[7:4] ↔ dst[3:0]	R		F0	X	*	*	X	–	–	2	2
		IR		F1							2	3
TCM dst, src	(NOT dst) AND src	r	r	62	–	*	*	0	–	–	2	3
		r	Ir	63							2	4
		R	R	64							3	3
		R	IR	65							3	4
		R	IM	66							3	3
		IR	IM	67							3	4
TCMX dst, src	(NOT dst) AND src	ER	ER	68	–	*	*	0	–	–	4	3
		ER	IM	69							4	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

DC Characteristics

Table 116 lists the DC characteristics of the Z8 Encore! F0830 Series products. All voltages are referenced to V_{SS}, the primary system ground.

Table 116. DC Characteristics

Symbol	Parameter	T_A = 0°C to +70°C			T_A = −40°C to +105°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
V_{DD}	Supply Voltage				2.7	–	3.6	V	Power supply noise not to exceed 100mV peak to peak
V_{IL1}	Low Level Input Voltage				−0.3	–	$0.3 * V_{DD}$	V	For all input pins except $\overline{RESET}$.
V_{IL2}	Low Level Input Voltage				−0.3	–	0.8	V	For $\overline{RESET}$.
V_{IH1}	High Level Input Voltage				2.0	–	5.5	V	For all input pins without analog or oscillator function.
V_{IH2}	High Level Input Voltage				2.0	–	$V_{DD}+0.3$	V	For those pins with analog or oscillator function.
V_{OL1}	Low Level Output Voltage				–	–	0.4	V	I_{OL} = 2mA; V_{DD} = 3.0V High Output Drive disabled.
V_{OH1}	High Level Output Voltage				2.4	–	–	V	I_{OH} = −2mA; V_{DD} = 3.0V High Output Drive disabled.
V_{OL2}	Low Level Output Voltage				–	–	0.6	V	I_{OL} = 20mA; V_{DD} = 3.3V High Output Drive enabled.
V_{OH2}	High Level Output Voltage				2.4	–	–	V	I_{OH} = −20mA; V_{DD} = 3.3V High Output Drive enabled.
I_{IL}	Input Leakage Current				−5	–	+5	µA	V_{DD} = 3.6V; V_{IN} = V_{DD} or V_{SS}[1]
I_{TL}	Tristate Leakage Current				−5	–	+5	µA	V_{DD} = 3.6V

Notes:
1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.
3. See Figure 31 for HALT Mode current.

Appendix A. Register Tables

For the reader's convenience, this appendix lists all F0830 Series registers numerically by hexadecimal address.

General Purpose RAM

In the F0830 Series, the `000-EFF` hexadecimal address range is partitioned for general-purpose random access memory, as follows.

Hex Addresses: 000–0FF

This address range is reserved for general-purpose register file RAM. For more details, see the Register File section on page 14.

Hex Addresses: 100–EFF

This address range is reserved.

Timer 0

For more information about these Timer Control registers, see the Timer Control Register Definitions section on page 83.

Hex Address: F00

Table 130. Timer 0 High Byte Register (T0H)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H							

Hex Address: F71

This address range is reserved.

Hex Address: F72

Table 147. ADC Data High Byte Register (ADCD_H)

Bit	7	6	5	4	3	2	1	0
Field	ADCDH							
RESET	X							
R/W	R							
Address	F72H							

Bit	Description
[7:0]	**ADC High Byte** 00h–FFh = The last conversion output is held in the data registers until the next ADC conversion is completed.

Hex Address: F73

Table 148. ADC Data Low Bits Register (ADCD_L)

Bit	7	6	5	4	3	2	1	0
Field	ADCDL		Reserved					
RESET	X		X					
R/W	R		R					
Address	F73H							

Bit Position	Description
[7:6]	**ADC Low Bits** 00–11b = These bits are the two least significant bits of the 10-bit ADC output. These bits are undefined after a reset. The low bits are latched into this register whenever the ADC Data High Byte Register is read.
[5:0]	**Reserved** These bits are reserved and must be programmed to 000000.

Hex Address: FDF

Table 183. Port D Output Data Register (PDOUT)

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDFH							

Hex Addresses: FE0–FEF

This address range is reserved.

Watchdog Timer

For more information about the Watchdog Timer registers, see the <u>Watchdog Timer Control Register Definitions</u> section on page 95.

Hex Address: FF0

The Watchdog Timer Control Register address is shared with the read-only Reset Status Register.

Table 184. Watchdog Timer Control Register (WDTCTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTUNLK							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
Address	FF0H							

Table 185. Reset Status Register (RSTSTAT)

Bit	7	6	5	4	3	2	1	0
Field	POR	STOP	WDT	EXT	Reserved			
RESET	See <u>Table 12</u> on page 29			0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	FF0H							