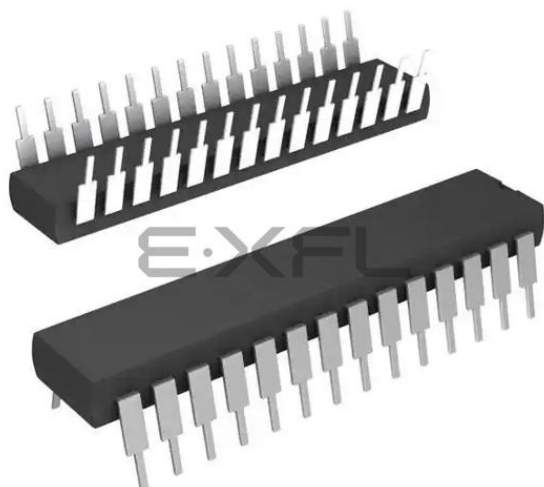




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Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	25
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0431pj020eg

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Revision History

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

Date	Revision Level	Chapter/Section	Description	Page No.
Dec 2012	13	GPIO	Modified GPIO Port D0 language in Shared Reset Pin section and Port Alternate Function Mapping table.	<u>35</u> , <u>36</u>
Sep 2011	12	LED Drive Enable Register	Clarified statement surrounding the Alternate Function Register as it relates to the LED function; revised Sector Based Flash Protection description; revised Packaging chapter.	<u>51</u> , <u>115</u> , <u>199</u>
Dec 2007	11	n/a	Updated all instances of <i>Z8 Encore! XP F0830</i> to <i>Z8 Encore! F0830</i> .	All
Nov 2007	10	DC Characteristics, On-Chip Peripheral AC and DC Electrical Characteristics	Updated Tables 116 and 122.	<u>185</u> , <u>193</u>
Sep 2007	09	Timers, PWM SINGLE OUTPUT Mode, PWM DUAL OUTPUT Mode, Analog-to-Digital Converter, Reference Buffer.	Updated Figures 2 and 4, Table 4.	<u>8</u> , <u>9</u> , <u>11</u> , <u>68</u> , <u>74</u> , <u>75</u> , <u>98</u> , <u>101</u>
Apr 2007	08	Optimizing NVDS Memory Usage for Execution Speed, On-Chip Peripheral AC and DC Electrical Characteristics	Added a note under Table 93 in Nonvolatile Data Storage chapter. Updated Table 121 and Table 122 in Electrical Characteristics chapter. Other style updates.	<u>137</u> , <u>193</u> , <u>193</u>
Dec 2006	07	General Purpose Input/Output	Added PD0 in Table 16.	<u>38</u>
		Overview, Interrupt Controller	Changed the number of interrupts to 17.	<u>1.5</u> , <u>53</u>
		Nonvolatile Data Storage	Updated chapter.	<u>136</u>
		Oscillator Control Register Definitions, AC Characteristics, On-Chip Peripheral AC and DC Electrical Characteristics	Updated Tables 117 and 122. Added Figure 24.	<u>156</u> , <u>189</u> , <u>193</u>
		Ordering Information	Updated Part Number Suffix Designations.	<u>205</u>
		n/a	Removed <i>Preliminary</i> stamp from footer.	All

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Reset and Stop Mode Recovery

The reset controller in the Z8 Encore! F0830 Series controls RESET and Stop Mode Recovery operations. In a typical operation, the following events can cause a reset:

- Power-On Reset (POR)
- Voltage Brown-Out (VBO)
- Watchdog Timer time-out (when configured by the WDT_RES Flash option bit to initiate a reset)
- External $\overline{\text{RESET}}$ pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-Chip Debugger initiated reset (OCDCTL[0] set to 1)

When the device is in STOP Mode, a Stop Mode Recovery event is initiated by either of the following occurrences:

- A Watchdog Timer time-out
- A GPIO port input pin transition on an enabled Stop Mode Recovery source

The VBO circuitry on the device generates a VBO reset when the supply voltage drops below a minimum safe level.

Reset Types

The Z8 Encore! F0830 Series provides different types of Reset operations. Stop Mode Recovery is considered a form of reset. Table 9 lists the types of resets and their operating characteristics. The duration of a system reset is longer if the external crystal oscillator is enabled by the Flash option bits; the result is additional time for oscillator startup.

Port A–D High Drive Enable Subregisters

The Port A–D High Drive Enable Subregister, shown in Table 24, is accessed through the Port A–D Control Register by writing 04H to the Port A–D Address Register. Setting the bits in the Port A–D High Drive Enable subregisters to 1 configures the specified port pins for high-output current drive operation. The Port A–D High Drive Enable Subregister affects the pins directly and, as a result, alternate functions are also affected.

Table 24. Port A–D High Drive Enable Subregisters (PxHDE)

Bit	7	6	5	4	3	2	1	0
Field	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 04H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0]	Port High Drive Enable
PHDE _x	0 = The port pin is configured for standard output current drive. 1 = The port pin is configured for high output current drive.
Note: x indicates the specific GPIO port pin number (7–0).	

LED Drive Level Low Register

The LED Drive Level Low Register, shown in Table 33, contains two control bits for each Port C pin. These two bits select one of four programmable current drive levels for each Port C pin. Each pin is individually programmable.

Table 33. LED Drive Level Low Register (LEDLVLL)

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLL[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F84H							

Bit	Description
[7:0]	LED Level Low Bits
LEDLVLL	{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin. 00 = 3mA. 01 = 7mA. 10 = 13mA. 11 = 20mA.

Analog-to-Digital Converter

The Z8 Encore! MCU includes an eight-channel Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). The ADC converts an analog input signal to a 10-bit binary number. The features of the SAR ADC include:

- Eight analog input sources multiplexed with general purpose I/O ports
- Fast conversion time, less than 11.9µs
- Programmable timing controls
- Interrupt on conversion complete
- Internal voltage reference generator
- Ability to select external reference voltage
- When configuring an ADC using external V_{REF} , PB5 is used as V_{REF} in the 28-pin package

Architecture

The ADC architecture, displayed in Figure 11, consists of an 8-input multiplexer, sample-and-hold amplifier and 10-bit SAR ADC. The ADC digitizes the signal on a selected channel and stores the digitized data in the ADC data registers. In an environment with high electrical noise, an external RC filter must be added at the input pins to reduce high-frequency noise.

$$T_{CONV} = T_{S/H} + T_{CON}$$

$$T_{CONV} = T_S + T_H + 13 * SCLK * 16$$

where:

SCLK = System Clock

T_{CONV} = Total conversion time

T_S = Sample time ($SCLK * ADCST$)

T_{CON} = Conversion time ($13 * SCLK * 16$)

T_H = Hold time ($SCLK * ADCSST$)

DIV = 16 (fixed to divide by 16 for F0830 Series products)

Example: For an F0830 Series MCU running @ 20MHz:

$$T_{CONV} = 1\mu s + 0.5\mu s + 13 * SCLK * DIV$$

$$T_{CONV} = 1\mu s + 0.5\mu s + 13 * (1/20MHz) * 16 = 11.9\mu s$$

Sample Settling Time Register

The Sample Settling Time Register, shown in Table 66, is used to program a delay after the $\overline{\text{SAMPLE/HOLD}}$ signal is asserted and before the START signal is asserted; an ADC conversion then begins. The number of clock cycles required for settling will vary from system to system depending on the system clock period used. The system designer should program this register to contain the number of clocks required to meet a 0.5 μs minimum settling time.

Table 66. Sample Settling Time (ADCSST)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				SST			
RESET	0				1	1	1	1
R/W	R				R/W			
Address	F74H							

Bit	Description
[7:4]	Reserved These bits are reserved and must be programmed to 0000.
[3:0] SST	0h–Fh = Sample settling time in number of system clock periods to meet 0.5 μs minimum.

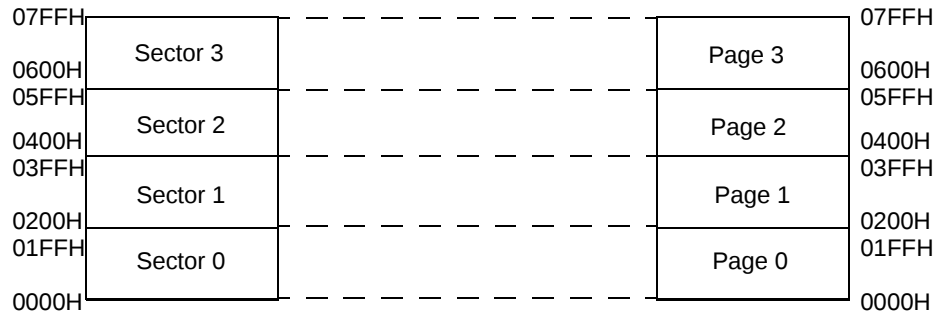


Figure 15. 2K Flash with NVDS

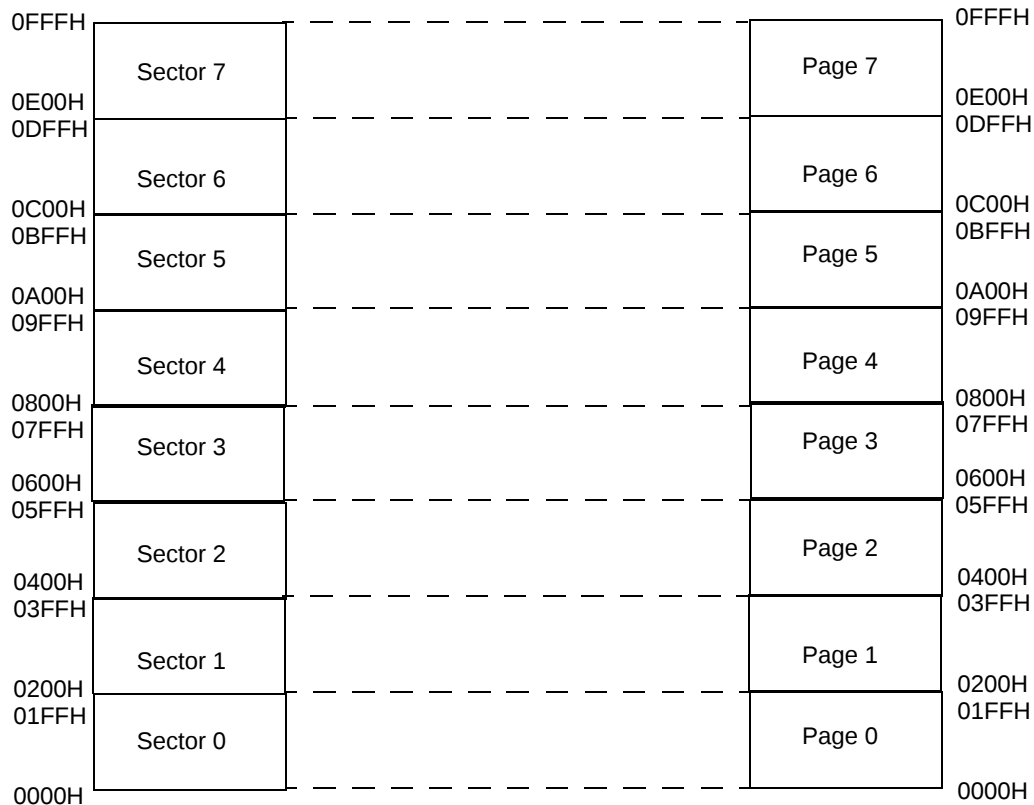


Figure 16. 4K Flash with NVDS

Flash Option Bit Control Register Definitions

This section briefly describes the features of the Trim Bit Address and Data registers.

Trim Bit Address Register

The Trim Bit Address Register, shown in Table 78, contains the target address to access the trim option bits. Trim bit addresses in the range 00h–1Fh map to the information area at addresses 20h–3Fh, as shown in Table 79.

Table 78. Trim Bit Address Register (TRMADR)

Bit	7	6	5	4	3	2	1	0
Field	TRMADR: Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF6H							

Table 79. Trim Bit Address Map

Trim Bit Address	Information Area Address
00h	20h
01h	21h
02h	22h
03h	23h
:	:
1Fh	3Fh

Trim Bit Data Register

The Trim Bit Data Register, shown in Table 80, contains the read or write data to access the trim option bits.

Bit	Description (Continued)
[1:0]	Filter Select
FilterSely	2-bit selection for the clock filter mode. 00 = No filter. 01 = Filter low level noise on high level signal. 10 = Filter high level noise on low level signal. 11 = Filter both.
Notes: x indicates bit values 3–1; y indicates bit values 1–0.	

► **Note:** The bit values used in Table 89 are set at factory and no calibration is required.

Table 90. ClkFlt Delay Control Definition

DlyCtl3, DlyCtl2, DlyCtl1	Low Noise Pulse on High Signal (ns)	High Noise Pulse on Low Signal (ns)
000	5	5
001	7	7
010	9	9
011	11	11
100	13	13
101	17	17
110	20	20
111	25	25
Note: The variation is about 30%.		

Table 121. Nonvolatile Data Storage

Parameter	V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C			V _{DD} = 2.7 to 3.6V T _A = -40°C to +105°C			Units	Notes
	Min	Typ	Max	Min	Typ	Max		
NVDS Byte Read Time				71	–	258	μs	With system clock at 20MHz
NVDS Byte Program Time				126	–	136	μs	With system clock at 20MHz
Data Retention				10	–	–	years	25°C
Endurance				100,000	–	–	cycles	Cumulative write cycles for entire memory

► **Note:** For every 200 writes, a maintenance operation is necessary. In this rare occurrence, the write can take up to 58ms to complete.

Table 122. Analog-to-Digital Converter Electrical Characteristics and Timing

Symbol	Parameter	V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C			V _{DD} = 2.7 to 3.6V T _A = -40°C to +105°C			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
	Resolution				–	10	–	bits	
	Differential Nonlinearity (DNL) ¹				–1	–	+4	LSB	
	Integral Nonlinearity (INL) ¹				–5	–	+5	LSB	
	Gain Error					15		LSB	
	Offset Error				–15	–	15	LSB	PDIP package
					–9	–	9	LSB	Other packages
V _{REF}	On chip reference				1.9	2.0	2.1	V	
	Active Power Consumption					4		mA	
	Power Down Current						1	μA	

Note: ¹When the input voltage is lower than 20mV, the conversion error is out of spec.

Table 122. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

Symbol	Parameter	$V_{DD} = 2.7 \text{ to } 3.6\text{V}$ $T_A = 0^\circ\text{C to } +70^\circ\text{C}$			$V_{DD} = 2.7 \text{ to } 3.6\text{V}$ $T_A = -40^\circ\text{C to } +105^\circ\text{C}$			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Z_{IN}	Input Impedance				10			MΩ	
V_{IN}	Input Voltage Range				0		2.0	V	Internal reference
					0		0.9*V _{DD}		External reference
	Conversion Time				11.9			μs	20MHz (ADC Clock)
	Input Bandwidth					500		KHz	
	Wake Up Time					0.02		ms	Internal reference
						10			External reference
	Input Clock Duty				45	50	55		
	Maximum Input Clock Frequency						20	MHz	

Note: ¹When the input voltage is lower than 20mV, the conversion error is out of spec.

Table 123. Comparator Electrical Characteristics

Symbol	Parameter	$V_{DD} = 2.7 \text{ to } 3.6\text{V}$ $T_A = 0^\circ\text{C to } +70^\circ\text{C}$			$V_{DD} = 2.7 \text{ to } 3.6\text{V}$ $T_A = -40^\circ\text{C to } +105^\circ\text{C}$			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
V_{OS}	Input DC Offset					5		mV	
V_{CREF}	Programmable Internal Reference Voltage Range				0		1.8	V	User-programmable in 200 mV step
V_{CREF}	Programmable internal reference voltage				0.92	1.0	1.08	V	Default (CMP0[REFLV] = 5H)
T_{PROP}	Propagation delay					100		ns	
V_{HYS}	Input hysteresis					8		mV	

Packaging

Zilog's F0830 Series of MCUs includes the Z8F0130, Z8F0131, Z8F0230, Z8F0231, Z8F1232 and Z8F1233 devices, which are available in the following packages:

- 20-Pin Quad Flat No-Lead Package (QFN)
- 20-pin Small Outline Integrated Circuit Package (SOIC)
- 20-pin Plastic Dual-Inline Package (PDIP)
- 20-pin Small Shrink Outline Package (SSOP)
- 28-Pin Quad Flat No-Lead Package (QFN)
- 28-pin Small Outline Integrated Circuit Package (SOIC)
- 28-pin Plastic Dual-Inline Package (PDIP)
- 28-pin Small Shrink Outline Package (SSOP)

Current diagrams for each of these packages are published in Zilog's Packaging Product Specification (PS0072), which is available free for download from the Zilog website.

Hex Address: F71

This address range is reserved.

Hex Address: F72

Table 147. ADC Data High Byte Register (ADCD_H)

Bit	7	6	5	4	3	2	1	0
Field	ADCDH							
RESET	X							
R/W	R							
Address	F72H							

Bit	Description
[7:0]	ADC High Byte 00h–FFh = The last conversion output is held in the data registers until the next ADC conversion is completed.

Hex Address: F73

Table 148. ADC Data Low Bits Register (ADCD_L)

Bit	7	6	5	4	3	2	1	0
Field	ADCDL		Reserved					
RESET	X		X					
R/W	R		R					
Address	F73H							

Bit Position	Description
[7:6]	ADC Low Bits 00–11b = These bits are the two least significant bits of the 10-bit ADC output. These bits are undefined after a reset. The low bits are latched into this register whenever the ADC Data High Byte Register is read.
[5:0]	Reserved These bits are reserved and must be programmed to 000000.

Hex Address: FD3

Table 172. Port A Output Data Register (PAOUT)

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD3H							

Hex Address: FD4

Table 173. Port B GPIO Address Register (PBADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD4H							

Hex Address: FD5

Table 174. Port B Control Registers (PBCTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD5H							

Hex Address: FD6

Table 175. Port B Input Data Registers (PBIN)

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	FD6H							

Hex Address: FDB

Table 180. Port C Output Data Register (PCOUT)

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDBH							

Hex Address: FDC

Table 181. Port D GPIO Address Register (PDADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDCH							

Hex Address: FDD

Table 182. Port D Control Registers (PDCTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDDH							

Hex Address: FDE

This address range is reserved.

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