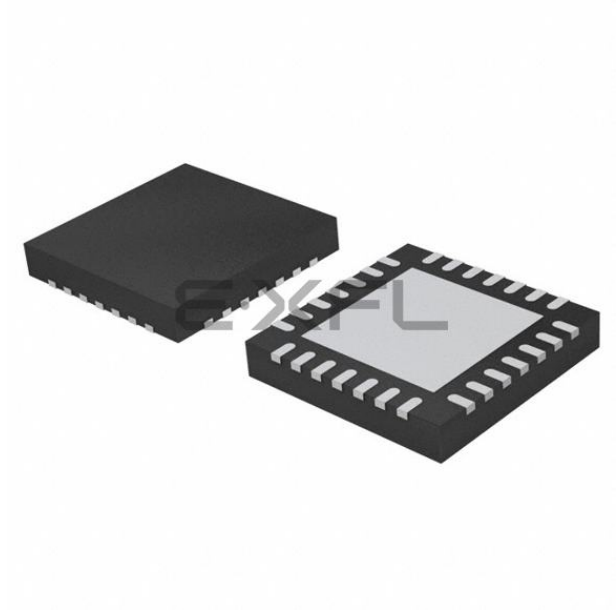

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	25
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0431qj020sg

Part Selection Guide

Table 1 lists the basic features available for each device within the Z8 Encore! F0830 Series product line. See the Ordering Information chapter on page 200 for details.

Table 1. Z8 Encore! F0830 Series Family Part Selection Guide

Part Number	Flash (KB)	RAM (B)	NVDS (64B)	ADC
Z8F1232	12	256	No	Yes
Z8F1233	12	256	No	No
Z8F0830	8	256	Yes	Yes
Z8F0831	8	256	Yes	No
Z8F0430	4	256	Yes	Yes
Z8F0431	4	256	Yes	No
Z8F0230	2	256	Yes	Yes
Z8F0231	2	256	Yes	No
Z8F0130	1	256	Yes	Yes
Z8F0131	1	256	Yes	No

Address Space

The eZ8 CPU can access the following three distinct address spaces:

- The register file addresses access for the general purpose registers and the eZ8 CPU, peripheral and general purpose I/O port control registers
- The program memory addresses access for all of the memory locations having executable code and/or data
- The data memory addresses access for all of the memory locations containing only the data

The following sections describe these three address spaces. For more information about the eZ8 CPU and its address space, refer to the eZ8 CPU Core User Manual (UM0128), which is available for download at www.zilog.com.

Register File

The register file address space in the Z8 Encore! MCU is 4KB (4096 bytes). The register file consists of two sections: control registers and general-purpose registers. When instructions are executed, registers defined as *source* are read and registers defined as *destinations* are written. The architecture of the eZ8 CPU allows all general purpose registers to function as accumulators, address pointers, index registers, stack areas or scratch pad memory.

The upper 256 bytes of the 4KB register file address space are reserved for controlling the eZ8 CPU, on-chip peripherals and the I/O ports. These registers are located at addresses from F00H to FFFH. Some of the addresses within the 256B Control Register section are reserved (unavailable). Reading from a reserved register file address returns an undefined value. Writing to reserved register file addresses is not recommended and can produce unpredictable results.

The on-chip RAM always begins at address 000H in the register file address space. The Z8 Encore! F0830 Series devices contain up to 256B of on-chip RAM. Reading from register file addresses outside the available RAM addresses (and not within the Control Register address space), returns an undefined value. Writing to these register file addresses has no effect.

Architecture

Figure 8 displays a simplified block diagram of a GPIO port pin. In this figure, the ability to accommodate alternate functions and variable port current drive strength is not displayed.

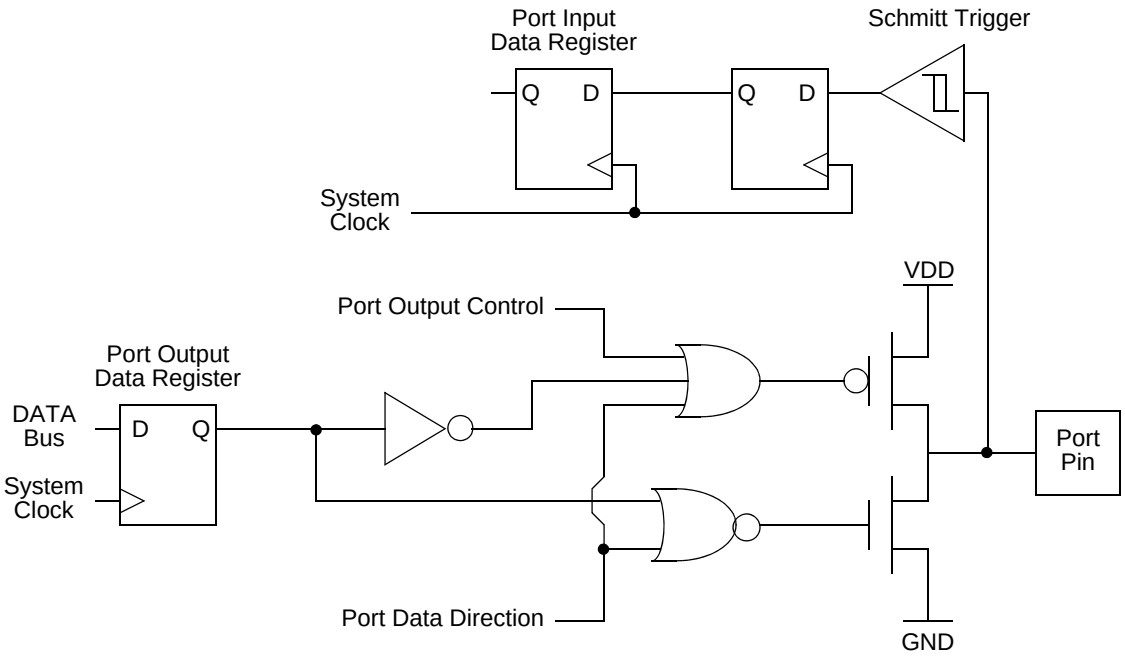

Figure 8. GPIO Port Pin Block Diagram

GPIO Alternate Functions

Many of the GPIO port pins can be used for general purpose input/output and access to on-chip peripheral functions such as the timers and serial communication devices. The Port A–D Alternate Function subregisters configure these pins for either GPIO or Alternate function operation. When a pin is configured for Alternate function, control of the port pin direction (input/output) is passed from the Port A–D data direction registers to the Alternate function assigned to this pin. Table 16 on page 36 lists the alternate functions possible with each port pin. The alternate function associated at a pin is defined through Alternate Function subregisters AFS1 and AFS2.

The crystal oscillator functionality is not controlled by the GPIO block. When the crystal oscillator is enabled in the oscillator control block, the GPIO functionality of PA0 and PA1 is overridden. In that case, pins PA0 and PA1 functions as input and output for the crystal oscillator.

PA0 and PA6 contain two different Timer functions, a timer input and a complementary timer output. Both of these functions require the same GPIO configuration, the selection between the two is based on the TIMER mode. For more details, see the Timers chapter on page 68.

Direct LED Drive

The Port C pins provide a sinked current output, capable of driving an LED without requiring an external resistor. The output sinks current at programmable levels, 3mA, 7mA, 13mA and 20mA. This mode is enabled through the LED Control registers.

For proper function, the LED anode must be connected to V_{DD} and the cathode to the GPIO pin.

Using all Port C pins in LED drive mode with maximum current may result in excessive total current. See the Electrical Characteristics chapter on page 184 for the maximum total current for the applicable package.

Shared Reset Pin

On the 20- and 28-pin devices, the Port D0 pin shares function with a bidirectional reset pin. Unlike all other I/O pins, this pin does not default to GPIO function on power-up. This pin acts as a bidirectional input/output open-drain reset with an internal pull-up until the user software reconfigures it as a GPIO PD0. When in GPIO mode, the Port D0 pin functions as output only, and must be configured as an output. PD0 supports the high drive feature, but not the stop-mode recovery feature.

Crystal Oscillator Override

For systems using a crystal oscillator, the pins PA0 and PA1 are connected to the crystal. When the crystal oscillator is enabled, the GPIO settings are overridden and PA0 and PA1 are disabled. See the Oscillator Control Register Definitions section on page 154.

5V Tolerance

In the 20- and 28-pin versions of this device, any pin, which shares functionality with an ADC, crystal or comparator port is not 5V-tolerant, including PA[1:0], PB[5:0] and PC[2:0]. All other signal pins are 5V-tolerant and can safely handle inputs higher than V_{DD} even with the pull-ups enabled, but with excess power consumption on pull-up resistor.

Interrupt Controller

The Interrupt Controller on the Z8 Encore!® F0830 Series products prioritize the interrupt requests from the on-chip peripherals and the GPIO port pins. The features of the Interrupt Controller include:

- Seventeen interrupt sources using sixteen unique interrupt vectors:
  - Twelve GPIO port pin interrupt sources
  - Five on-chip peripheral interrupt sources (Comparator Output interrupt shares one interrupt vector with PA6)
- Flexible GPIO interrupts
  - Eight selectable rising and falling edge GPIO interrupts
  - Four dual-edge interrupts
- Three levels of individually programmable interrupt priority
- Watchdog Timer can be configured to generate an interrupt
  m

Interrupt requests (IRQs) allow peripheral devices to suspend CPU operation in an orderly manner and force the CPU to start an interrupt service routine (ISR). Usually this interrupt service routine is involved with the exchange of data, status information or control information between the CPU and the interrupting peripheral. When the service routine is completed, the CPU returns to the operation from which it was interrupted.

The eZ8 CPU supports both vectored and polled interrupt handling. For polled interrupts, the Interrupt Controller has no effect on operation. For more information about interrupt servicing by the eZ8 CPU, refer to the eZ8 CPU User Manual (UM0128), which is available for download at www.zilog.com.

Interrupt Vector Listing

Table 34 lists the interrupts available in order of priority. The interrupt vector is stored with the most significant byte (MSB) at the even program memory address and the least significant byte (LSB) at the odd program memory address.

Note: Some port interrupts are not available on the 20-pin and 28-pin packages. The ADC interrupt is unavailable on devices not containing an ADC.

Interrupt Request 1 Register

The Interrupt Request 1 (IRQ1) Register, shown in Table 36, stores interrupt requests for both vectored and polled interrupts. When a request is sent to the Interrupt Controller, the corresponding bit in the IRQ1 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the Interrupt Controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 1 Register to determine if any interrupt requests are pending.

Table 36. Interrupt Request 1 Register (IRQ1)

Bit	7	6	5	4	3	2	1	0
Field	PA7I	PA6CI	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC3H							

Bit	Description
[7] PA7I	**Port A7** 0 = No interrupt request is pending for GPIO Port A. 1 = An interrupt request from GPIO Port A.
[6] PA6CI	**Port A6 or Comparator Interrupt Request** 0 = No interrupt request is pending for GPIO Port A or comparator. 1 = An interrupt request from GPIO Port A or comparator.
[5] PAxI	**Port A Pin *x* Interrupt Request** 0 = No interrupt request is pending for GPIO Port A pin *x*. 1 = An interrupt request from GPIO Port A pin *x* is awaiting service.

Note: x indicates the specific GPIO port pin number (5–0).

Timer Reload High and Low Byte Registers

The Timer 0–1 Reload High and Low Byte (TxRH and TxRL) registers, shown in Tables 52 and 53, store a 16-bit reload value, {TRH[7:0], TRL[7:0]}. Values written to the Timer Reload High Byte Register are stored in a temporary holding register. When a write to the Timer Reload Low Byte Register occurs, the temporary holding register value is written to the Timer High Byte Register. This operation allows simultaneous updates of the 16-bit timer reload value. In COMPARE Mode, the Timer Reload High and Low Byte registers store the 16-bit compare value.

Table 52. Timer 0–1 Reload High Byte Register (TxRH)

Bit	7	6	5	4	3	2	1	0
Field	TRH							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F02H, F0AH							

Table 53. Timer 0–1 Reload Low Byte Register (TxRL)

Bit	7	6	5	4	3	2	1	0
Field	TRL							
RESET	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F03H, F0BH							

Bit	Description
[7:0] TRH, TRL	**Timer Reload Register High and Low** These two bytes form the 16-bit reload value, {TRH[7:0], TRL[7:0]}. This value sets the maximum count value, which initiates a timer reload to 0001H. In COMPARE Mode, these two bytes form the 16-bit compare value.

Timer 0–1 Control Registers

The Timer Control registers are 8-bit read/write registers that control the operation of their associated counter/timers.

Time 0–1 Control Register 0

The Timer Control 0 (TxCTL0) and Timer Control 1 (TxCTL1) registers determine the timer operating mode. These registers also include a programmable PWM deadband delay, two bits to configure the timer interrupt definition, and a status bit to identify if the most recent timer interrupt is caused by an input capture event.

Table 56. Timer 0–1 Control Register 0 (TxCTL0)

Bit	7	6	5	4	3	2	1	0
Field	TMODEHI	TICONFIG		Reserved	PWMD			INPCAP
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F06H, F0EH							

Bit	Description
[7] TMODEHI	**Timer Mode High Bit** This bit along with the TMODE field in the TxCTL1 Register determines the operating mode of the timer. This is the most significant bit of the timer mode selection value. See the TxCTL1 Register description on the next page for additional details.
[6:5] TICONFIG	**Timer Interrupt Configuration** This field configures timer interrupt definition. 0x = Timer interrupt occurs on all of the defined reload, compare and input events. 10 = Timer interrupt occurs only on defined input capture/deassertion events. 11 = Timer interrupt occurs only on defined reload/compare events.
[4]	**Reserved** This bit is reserved and must be programmed to 0.
[3:1] PWMD	**PWM Delay Value** This field is a programmable delay to control the number of system clock cycles delay before the timer output and the timer output complement are forced to their Active state. 000 = No delay. 001 = 2 cycles delay. 010 = 4 cycles delay. 011 = 8 cycles delay. 100 = 16 cycles delay. 101 = 32 cycles delay. 110 = 64 cycles delay. 111 = 128 cycles delay.

Flash Memory

The products in the Z8 Encore! F0830 Series features either 1KB (1024 bytes with NVDS), 2KB (2048 bytes with NVDS), 4KB (4096 bytes with NVDS), 8KB (8192 bytes with NVDS) or 12KB (12288 bytes with no NVDS) of nonvolatile Flash memory with read/write/erase capability. Flash memory can be programmed and erased in-circuit by either user code or through the On-Chip Debugger.

The Flash memory array is arranged in pages with 512 bytes per page. The 512-byte page is the minimum Flash block size that can be erased. Each page is divided into eight rows of 64 bytes.

For program/data protection, Flash memory is also divided into sectors. In the Z8 Encore! F0830 Series, each sector maps to one page (for 1KB, 2KB and 4KB devices), two pages (8KB device) or three pages (12KB device).

The first two bytes of Flash program memory is used as Flash option bits. For more information, see *the* Flash Option Bits chapter on page 124.

Table 69 lists the Flash memory configuration for each device in the Z8 Encore! F0830 Series. Figures 14 through 18 display the memory arrangements for each Flash memory size.

Table 69. Z8 Encore! F0830 Series Flash Memory Configuration

Part Number	Flash Size KB (Bytes)	Flash Pages	Program Memory Addresses	Flash Sector Size (bytes)
Z8F123x	12 (12,288)	24	0000H–2FFFH	1536
Z8F083x	8 (8196)	16	0000H–1FFFH	1024
Z8F043x	4 (4096)	8	0000H–0FFFH	512
Z8F023x	2 (2048)	4	0000H–07FFH	512
Z8F013x	1 (1024)	2	0000H–03FFH	512

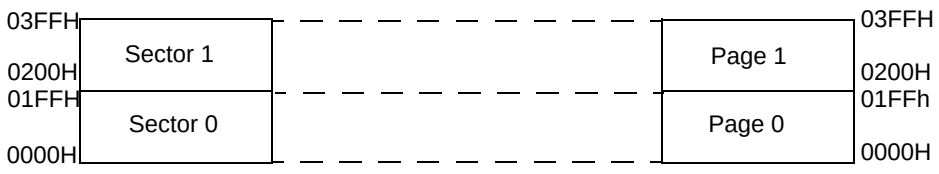

Figure 14. 1K Flash with NVDS

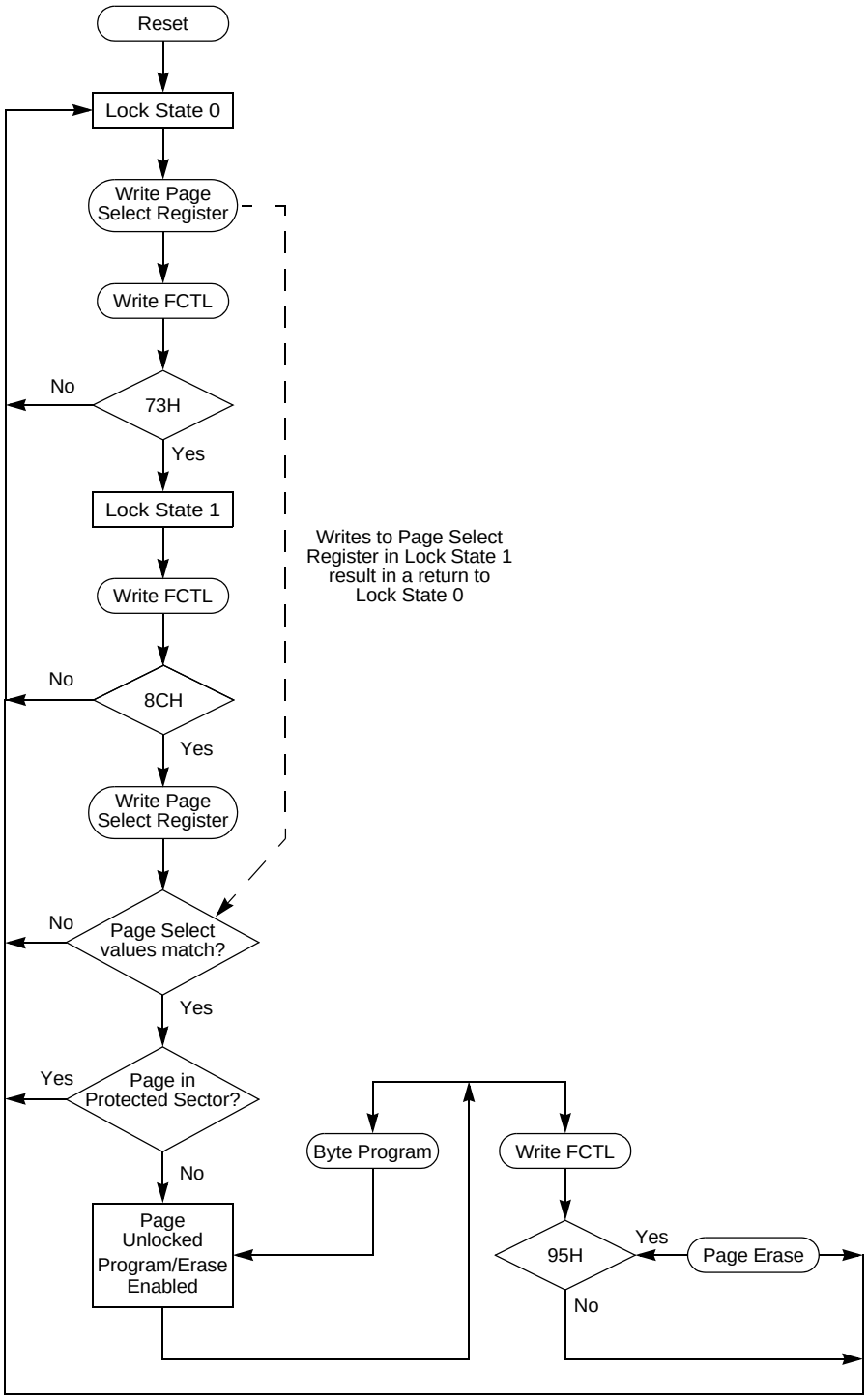

Figure 19. Flash Controller Operation Flow Chart

bits can only be set to 1. Thus, sectors can be protected, but not unprotected, via register write operations. Writing a value other than 5EH to the Flash Control Register deselects the Flash Sector Protect Register and reenables access to the Page Select Register. Observe the following procedure to setup the Flash Sector Protect Register from user code:

1. Write 00H to the Flash Control Register to reset the Flash Controller.
2. Write 5EH to the Flash Control Register to select the Flash Sector Protect Register.
3. Read and/or write the Flash Sector Protect Register which is now at Register File address FF9H.
4. Write 00H to the Flash Control Register to return the Flash Controller to its reset state.

The Sector Protect Register is initialized to 0 on reset, putting each sector into an unprotected state. When a bit in the Sector Protect Register is written to 1, the corresponding sector can no longer be written or erased. After setting a bit in the Sector Protect Register, the bit cannot be cleared by the user.

Byte Programming

Flash memory is enabled for byte programming after unlocking the Flash Controller and successfully enabling either mass erase or page erase. When the Flash Controller is unlocked and mass erase is successfully enabled, all of the program memory locations are available for byte programming. In contrast, when the Flash Controller is unlocked and page erase is successfully enabled, only the locations of the selected page are available for byte programming. An erased Flash byte contains all 1's (FFH). The programming operation can only be used to change bits from 1 to 0. To change a Flash bit (or multiple bits) from 0 to 1 requires execution of either the page erase or mass erase commands.

Byte programming can be accomplished using the On-Chip Debugger's write memory command or eZ8 CPU execution of the LDC or LDCI instructions. Refer to the eZ8 CPU Core User Manual (UM0128), which is available for download on www.zilog.com, for the description of the LDC and LDCI instructions. While the Flash Controller programs the Flash memory, the eZ8 CPU idles, but the system clock and on-chip peripherals continue to operate. To exit programming mode and lock the Flash, write any value to the Flash Control Register, except the mass erase or page erase commands.

Caution: The byte at each address within Flash memory cannot be programmed (any bits written to 0) more than twice before an erase cycle occurs.

Bit	Description (Continued)
[1:0] FilterSel*y*	**Filter Select** 2-bit selection for the clock filter mode. 00 = No filter. 01 = Filter low level noise on high level signal. 10 = Filter high level noise on low level signal. 11 = Filter both.

Notes: x indicates bit values 3–1; y indicates bit values 1–0.

Note: The bit values used in Table 89 are set at factory and no calibration is required.

Table 90. ClkFlt Delay Control Definition

DlyCtl3, DlyCtl2, DlyCtl1	Low Noise Pulse on High Signal (ns)	High Noise Pulse on Low Signal (ns)
000	5	5
001	7	7
010	9	9
011	11	11
100	13	13
101	17	17
110	20	20
111	25	25

Note: The variation is about 30%.

Runtime Counter

The OCD contains a 16-bit runtime counter. It counts system clock cycles between breakpoints. The counter starts counting when the OCD leaves DEBUG Mode and stops counting when it enters DEBUG Mode again or when it reaches the maximum count of FFFFH.

On-Chip Debugger Commands

The host communicates to the On-Chip Debugger by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG Mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash read protect option bit (FRP). The FRP prevents the code in memory from being read out of the Z8 Encore! F0830 Series products. When this option is enabled, several of the OCD commands are disabled.

Table 95 summarizes the On-Chip Debugger commands. This table indicates the commands that operate when the device is not in DEBUG Mode (normal operation) and the commands that are disabled by programming the FRP.

Table 95. On-Chip Debugger Command Summary

Debug Command	Command Byte	Enabled when not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	–
Reserved	01H	–	–
Read OCD Status Register	02H	Yes	–
Read Runtime Counter	03H	–	–
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit
Read OCD Control Register	05H	Yes	–
Write Program Counter	06H	–	Disabled
Read Program Counter	07H	–	Disabled
Write Register	08H	–	Only writes of the Flash Memory Control registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Control register.
Read Register	09H	–	Disabled
Write Program Memory	0AH	–	Disabled
Read Program Memory	0BH	–	Disabled
Write Data Memory	0CH	–	Yes
Read Data Memory	0DH	–	–

ory size and is approximately equal to the system clock period multiplied by the number of bytes in program memory.

```
DBG ← 0EH
DBG → CRC[15:8]
DBG → CRC[7:0]
```

Step Instruction (10H). The step instruction command, steps one assembly instruction at the current program counter (PC) location. If the device is not in DEBUG Mode or the Flash read protect option bit is enabled, the OCD ignores this command.

```
DBG ← 10H
```

Stuff Instruction (11H). The stuff instruction command, steps one assembly instruction and allows specification of the first byte of the instruction. The remaining 0–4 bytes of the instruction are read from program memory. This command is useful for stepping over instructions where the first byte of the instruction has been overwritten by a breakpoint. If the device is not in DEBUG Mode or the Flash read protect option bit is enabled, the OCD ignores this command.

```
DBG ← 11H
DBG ← opcode[7:0]
```

Execute Instruction (12H). The execute instruction command allows sending an entire instruction to be executed to the eZ8 CPU. This command can also step over breakpoints. The number of bytes to send for the instruction depends on the opcode. If the device is not in DEBUG Mode or the Flash read protect option bit is enabled, this command reads and discards one byte.

```
DBG ← 12H
DBG ← 1–5 byte opcode
```

On-Chip Debugger Control Register Definitions

This section describes the features of the On-Chip Debugger Control and Status registers.

OCD Control Register

The OCD Control Register controls the state of the On-Chip Debugger. This register is used to enter or exit DEBUG Mode and to enable the BRK instruction. It can also reset the Z8 Encore! F0830 Series device.

A reset and stop function can be achieved by writing 81H to this register. A *reset and go* function can be achieved by writing 41H to this register. If the device is in DEBUG Mode, a run function can be implemented by writing 40H to this register.

! **Caution:** It is possible to disable the clock failure detection circuitry as well as all functioning clock sources. In this case, the Z8 Encore! F0830 Series device ceases functioning and can only be recovered by power-on-reset.

Oscillator Control Register Definitions

The following section provides the bit definitions for the Oscillator Control Register.

Oscillator Control Register

The Oscillator Control Register (OSCCTL) enables/disables the various oscillator circuits, enables/disables the failure detection/recovery circuitry and selects the primary oscillator, which becomes the system clock.

The Oscillator Control Register must be unlocked before writing. Writing the two step sequence E7H followed by 18H to the Oscillator Control Register unlocks it. The register is locked at successful completion of a register write to the OSCCTL.

Figure 24 displays the oscillator control clock switching flow. See Table 117 on page 189 to review the waiting times of various oscillator circuits.

Table 99. Oscillator Control Register (OSCCTL)

Bit	7	6	5	4	3	2	1	0
Field	INTEN	XTLEN	WDTEN	POFEN	WDFEN	SCKSEL		
RESET	1	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F86H							

Bit	Description
[7] INTEN	**Internal Precision Oscillator Enable** 1 = Internal Precision Oscillator is enabled. 0 = Internal Precision Oscillator is disabled.
[6] XTLEN	**Crystal Oscillator Enable** This setting overrides the GPIO register control for PA0 and PA1. 1 = Crystal oscillator is enabled. 0 = Crystal oscillator is disabled.
[5] WDTEN	**Watchdog Timer Oscillator Enable** 1 = Watchdog Timer Oscillator is enabled. 0 = Watchdog Timer Oscillator is disabled.

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
LDX dst, src	dst ← src	r	ER	84	–	–	–	–	–	–	3	2
		Ir	ER	85							3	3
		R	IRR	86							3	4
		IR	IRR	87							3	5
		r	X(rr)	88							3	4
		X(rr)	r	89							3	4
		ER	r	94							3	2
		ER	Ir	95							3	3
		IRR	R	96							3	4
		IRR	IR	97							3	5
		ER	ER	E8							4	2
		ER	IM	E9							4	2
LEA dst, X(src)	dst ← src + X	r	X(r)	98	–	–	–	–	–	–	3	3
		rr	X(rr)	99							3	5
MULT dst	dst[15:0] ← dst[15:8] * dst[7:0]	RR		F4	–	–	–	–	–	–	2	8
NOP	No operation			0F	–	–	–	–	–	–	1	2
OR dst, src	dst ← dst OR src	r	r	42	–	*	*	0	–	–	2	3
		r	Ir	43							2	4
		R	R	44							3	3
		R	IR	45							3	4
		R	IM	46							3	3
		IR	IM	47							3	4
ORX dst, src	dst ← dst OR src	ER	ER	48	–	*	*	0	–	–	4	3
		ER	IM	49							4	3
POP dst	dst ← @SP SP ← SP + 1	R		50	–	–	–	–	–	–	2	2
		IR		51							2	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 128. Z8 Encore! XP F0830 Series Ordering Matrix

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8F1233QH020EG	12KB	256	No	0	QFN 20-pin
Z8F1232SJ020EG	12KB	256	No	8	SOIC 28-pin
Z8F1232HJ020EG	12KB	256	No	8	SSOP 28-pin
Z8F1232PJ020EG	12KB	256	No	8	PDIP 28-pin
Z8F1232QJ020EG	12KB	256	No	8	QFN 28-pin
Z8F1233SJ020EG	12KB	256	No	0	SOIC 28-pin
Z8F1233HJ020EG	12KB	256	No	0	SSOP 28-pin
Z8F1233PJ020EG	12KB	256	No	0	PDIP 28-pin
Z8F1233QJ020EG	12KB	256	No	0	QFN 28-pin
Z8 Encore! F0830 with 8KB Flash					
Standard Temperature: 0°C to 70°C					
Z8F0830SH020SG	8KB	256	Yes	7	SOIC 20-pin
Z8F0830HH020SG	8KB	256	Yes	7	SSOP 20-pin
Z8F0830PH020SG	8KB	256	Yes	7	PDIP 20-pin
Z8F0830QH020SG	8KB	256	Yes	7	QFN 20-pin
Z8F0831SH020SG	8KB	256	Yes	0	SOIC 20-pin
Z8F0831HH020SG	8KB	256	Yes	0	SSOP 20-pin
Z8F0831PH020SG	8KB	256	Yes	0	PDIP 20-pin
Z8F0831QH020SG	8KB	256	Yes	0	QFN 20-pin
Z8F0830SJ020SG	8KB	256	Yes	8	SOIC 28-pin
Z8F0830HJ020SG	8KB	256	Yes	8	SSOP 28-pin
Z8F0830PJ020SG	8KB	256	Yes	8	PDIP 28-pin
Z8F0830QJ020SG	8KB	256	Yes	8	QFN 28-pin
Z8F0831SJ020SG	8KB	256	Yes	0	SOIC 28-pin
Z8F0831HJ020SG	8KB	256	Yes	0	SSOP 28-pin
Z8F0831PJ020SG	8KB	256	Yes	0	PDIP 28-pin
Z8F0831QJ020SG	8KB	256	Yes	0	QFN 28-pin
Extended Temperature: –40°C to 105°C					
Z8F0830SH020EG	8KB	256	Yes	7	SOIC 20-pin
Z8F0830HH020EG	8KB	256	Yes	7	SSOP 20-pin
Z8F0830PH020EG	8KB	256	Yes	7	PDIP 20-pin
Z8F0830QH020EG	8KB	256	Yes	7	QFN 20-pin
Z8F0831SH020EG	8KB	256	Yes	0	SOIC 20-pin

Hex Address: FD7

Table 176. Port B Output Data Register (PBOUT)

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD7H							

Hex Address: FD8

Table 177. Port C GPIO Address Register (PCADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD8H							

Hex Address: FD9

Table 178. Port C Control Registers (PCCTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD9H							

Hex Address: FDA

Table 179. Port C Input Data Registers (PCIN)

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	FDAH							

Hex Address: FFB

Table 196. Flash Frequency Low Byte Register (FFREQL)

Bit	7	6	5	4	3	2	1	0
Field	FFREQL							
RESET	0							
R/W	R/W							
Address	FFBH							

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Symbols

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