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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	25
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0431sj020sg

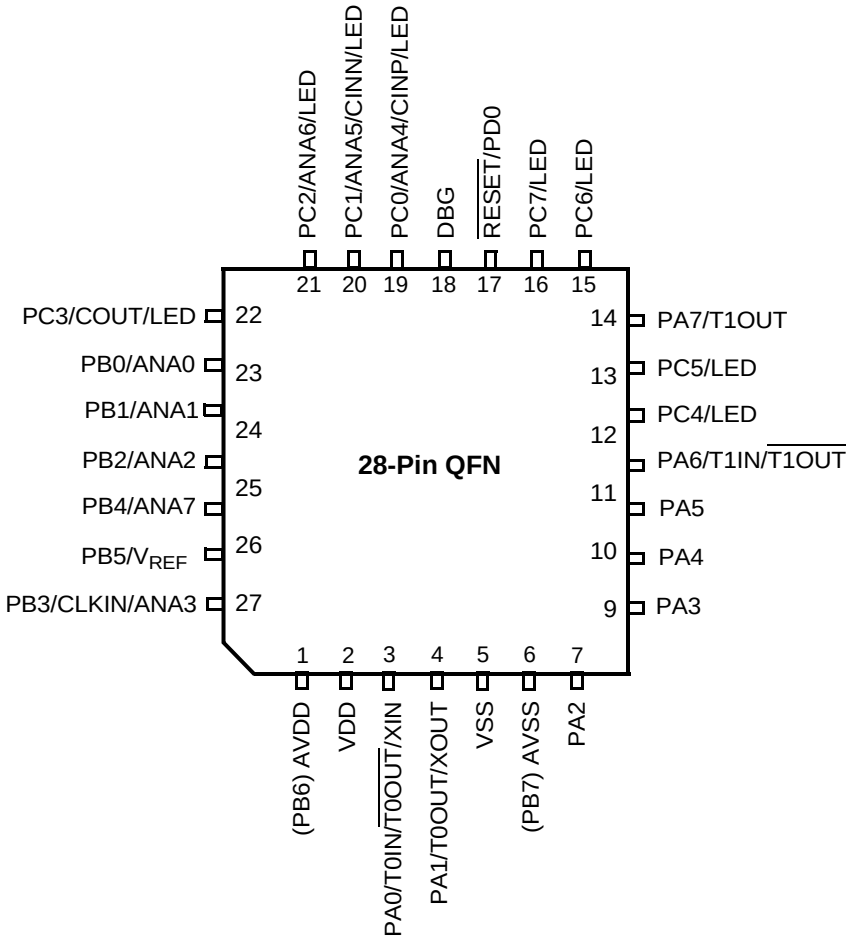

Figure 5. Z8F0830 Series in 28-Pin QFN Package

Table 4. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
Oscillators		
X_{IN}	I	External crystal input. This is the input pin to the crystal oscillator. A crystal can be connected between it and the **XOUT** pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock.
X_{OUT}	O	External crystal output. This pin is the output of the crystal oscillator. A crystal can be connected between it and the **XIN** pin to form the oscillator.
Clock Input		
CLK_{IN}	I	Clock input signal. This pin may be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	O	Direct LED drive capability. All Port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the On-Chip Debugger. **Caution:** The DBG pin is open-drain and requires an external pull-up resistor to ensure proper operation.
Reset		
$\overline{RESET}$	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! forces this pin low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V_{DD}	I	Digital power supply.
AV_{DD}	I	Analog power supply.
V_{SS}	I	Digital ground.
AV_{SS}	I	Analog ground.

Note: The AV_{DD} and AV_{SS} signals are available only in the 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No.
Interrupt Controller (cont'd)				
FCE	Shared interrupt select	IRQSS	00	66
FCF	Interrupt control	IRQCTL	00	67
GPIO Port A				
FD0	Port A address	PAADDR	00	39
FD1	Port A control	PACTL	00	41
FD2	Port A input data	PAIN	XX	41
FD3	Port A output data	PAOUT	00	41
GPIO Port B				
FD4	Port B address	PBADDR	00	39
FD5	Port B control	PBCTL	00	41
FD6	Port B input data	PBIN	XX	41
FD7	Port B output data	PBOUT	00	41
GPIO Port C				
FD8	Port C address	PCADDR	00	39
FD9	Port C control	PCCTL	00	41
FDA	Port C input data	PCIN	XX	41
FDB	Port C output data	PCOUT	00	41
GPIO Port D				
FDC	Port D address	PDADDR	00	39
FDD	Port D control	PDCTL	00	41
FDE	Reserved	—	XX	
FDF	Port D output data	PDOUT	00	41
FE0–FEF	Reserved	—	XX	
Watchdog Timer (WDT)				
FF0	Reset status	RSTSTAT	XX	95
	Watchdog Timer control	WDTCTL	XX	95
FF1	Watchdog Timer reload upper byte	WDTU	FF	96
FF2	Watchdog Timer reload high byte	WDTH	FF	96
FF3	Watchdog Timer reload low byte	WDTL	FF	97
FF4–FF5	Reserved	—	XX	

Note: XX = Undefined.

Reset Sources

Table 10 lists the possible sources of a system reset.

Table 10. Reset Sources and Resulting Reset Type

Operating Mode	Reset Source	Special Conditions
NORMAL or HALT modes	Power-On Reset/Voltage Brown-Out	Reset delay begins after supply voltage exceeds POR level.
	Watchdog Timer time-out when configured for reset	None.
	$\overline{\text{RESET}}$ pin assertion	All reset pulses less than four system clocks in width are ignored.
	On-Chip Debugger initiated reset (OCDCTL[0] set to 1)	System, except the On-Chip Debugger is unaffected by the reset.
STOP Mode	Power-On Reset/Voltage Brown-Out	Reset delay begins after supply voltage exceeds POR level.
	$\overline{\text{RESET}}$ pin assertion	All reset pulses less than 12 ns are ignored.
	DBG pin driven Low	None.

Power-On Reset

Each device in the Z8 Encore! F0830 Series contains an internal Power-On Reset circuit. The POR circuit monitors the digital supply voltage and holds the device in the Reset state until the digital supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold (V_{POR}), the device is held in the Reset state until the POR counter has timed out. If the crystal oscillator is enabled by the option bits, the time-out is longer.

After the Z8 Encore! F0830 Series device exits the Power-On Reset state, the eZ8 CPU fetches the reset vector. Following the Power-On Reset, the POR status bit in the Reset Status (RSTSTAT) Register is set to 1.

Figure 6 displays the Power-On Reset operation. See the Electrical Characteristics chapter on page 184 for the POR threshold voltage (V_{POR}).

Stop Mode Recovery Using the External $\overline{\text{RESET}}$ Pin

When the Z8 Encore! F0830 Series device is in STOP Mode and the external $\overline{\text{RESET}}$ pin is driven low, a system reset occurs. Because of a glitch filter operating on the $\overline{\text{RESET}}$ pin, the low pulse must be greater than the minimum width specified about 12 ns or it is ignored. The EXT bit in the Reset Status (RSTSTAT) Register is set.

Debug Pin Driven Low

Debug reset is initiated when the On-Chip Debugger detects any of the following error conditions on the DBG pin:

- Serial break (a minimum of nine continuous bits Low)
- Framing error (received STOP bit is Low)
- Transmit collision (simultaneous OCD and host transmission detected by the OCD)

When the Z8F0830 Series device is operating in STOP Mode, the debug reset will cause a system reset. The On-Chip Debugger block is not reset, but the remainder of the chip's operations go through a normal system reset. The POR bit in the Reset Status (RSTSTAT) Register is set to 1.

Reset Register Definitions

The following sections define the Reset registers.

Reset Status Register

The Reset Status (RSTSTAT) Register, shown in Table 12, is a read-only register that indicates the source of the most recent Reset event, Stop Mode Recovery event or Watchdog Timer time-out event. Reading this register resets the upper four bits to 0.

This register shares its address with the Watchdog Timer Control Register, which is write-only.

Table 16. Port Alternate Function Mapping (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C[3]	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or comparator input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or comparator input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6	ADC analog input	AFS1[2]: 1
	PC3	COUT	Comparator output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1
Port D[1]	PD0	RESET	Default to be Reset function	N/A

Notes:
1. Because there is only a single alternate function for each Port A and Port D (PD0) pin, the Alternate Function Set registers are not implemented for Port A and Port D (PD0). Enabling alternate function selections (as described in the Port A–D Alternate Function Subregisters section on page 42) automatically enables the associated alternate function.
2. Because there are at most two choices of alternate functions for any Port B pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the Port A–D Alternate Function Subregisters section on page 42) must also be enabled.
3. Because there are at most two choices of alternate functions for any Port C pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the Port A–D Alternate Function Subregisters section on page 42) must also be enabled.

Port A–D Alternate Function Set 2 Subregisters

The Port A–D Alternate Function Set 2 Subregister, shown in Table 28, is accessed through the Port A–D Control Register by writing 08H to the Port A–D Address Register. The Alternate Function Set 2 subregisters select the alternate function available at a port pin. Alternate functions selected by setting or clearing bits in this register are defined in Table 16 in the GPIO Alternate Functions section on page 34.

Note: Alternate function selection on the port pins must also be enabled, as described in the Port A–D Alternate Function Subregisters section on page 42.

Table 28. Port A–D Alternate Function Set 2 Subregisters (PxAFS2)

Bit	7	6	5	4	3	2	1	0
Field	PAFS27	PAFS26	PAFS25	PAFS24	PAFS23	PAFS22	PAFS21	PAFS20
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 08H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0] PAFS2x	**Port Alternate Function Set 2** 0 = The Port Alternate function is selected, as defined in Table 16 in the GPIO Alternate Functions section on page 34. 1 = The Port Alternate function is selected, as defined in Table 16 in the GPIO Alternate Functions section on page 34.

Note: x indicates the specific GPIO port pin number (7–0).

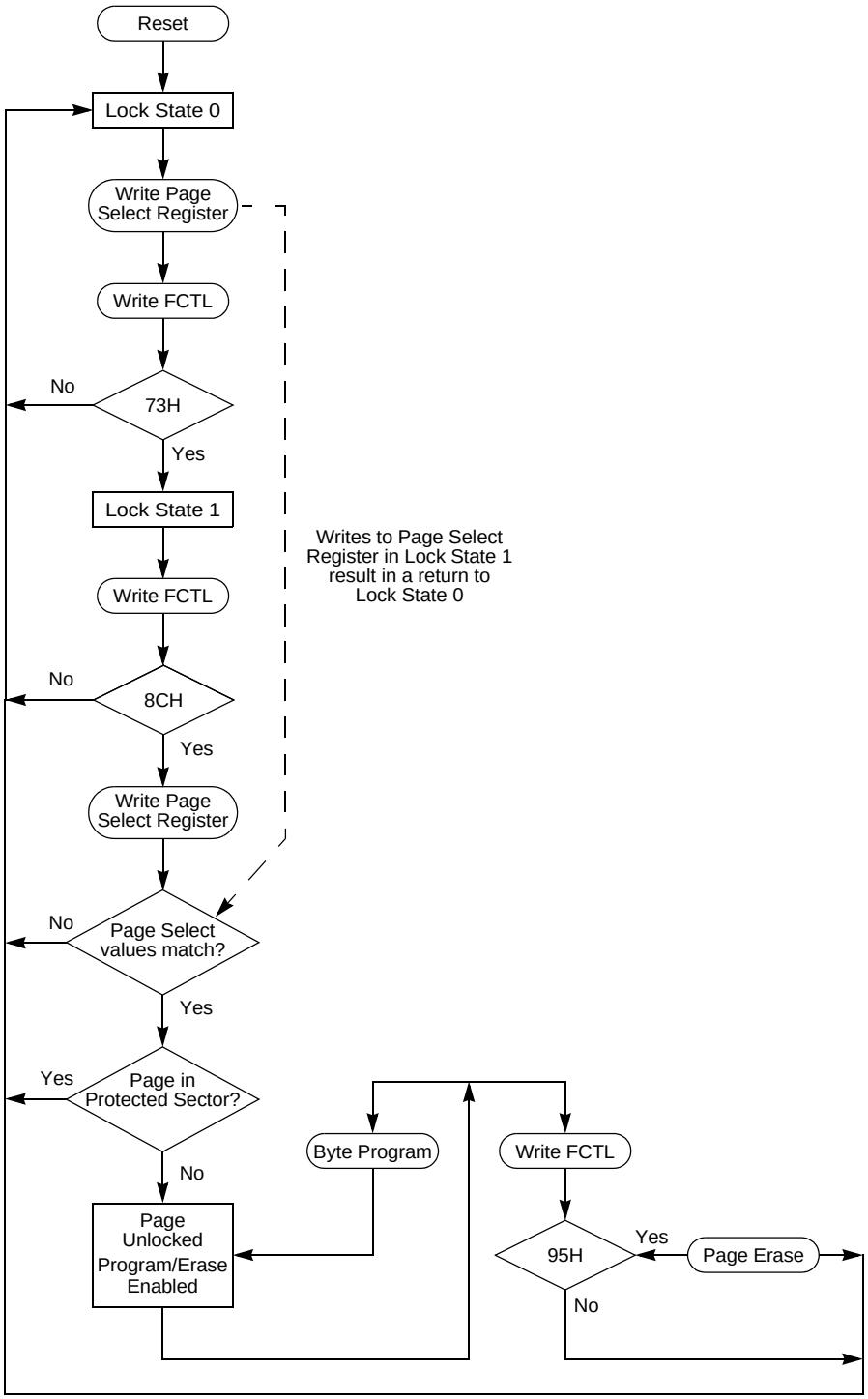

Figure 19. Flash Controller Operation Flow Chart

Flash Page Select Register

The Flash Page Select Register shares address space with the Flash Sector Protect Register. Unless the Flash Controller is locked and written with 5EH, any writes to this address will target the Flash Page Select Register.

The register selects one of the eight available Flash memory pages to be programmed or erased. Each Flash page contains 512-bytes of Flash memory. During a page erase operation, all Flash memory containing addresses with the most significant 7-bits within FPS[6:0] are chosen for program/erase operations.

Table 74. Flash Page Select Register (FPS)

Bit	7	6	5	4	3	2	1	0
Field	INFO_EN	PAGE						
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF9H							

Bit	Description
[7] INFO_EN	**Information Area Enable** 0 = Information area is not selected. 1 = Information area is selected. The information area is mapped into the program memory address space at addresses FE00H through FFFFH.
[6:0] PAGE	**Page Select** This 7-bit field identifies the Flash memory page for page erase and page unlocking. Program memory address[15:9] = PAGE[6:0]. For Z8F04xx and Z8F02xx devices, the upper four bits must always be 0. For Z8F01xx devices, the upper five bits must always be 0.

Note: The bit values used in Table 85 are set at the factory; no calibration is required.

Table 86. Trim Option Bits at 0002H (TIPO)

Bit	7	6	5	4	3	2	1	0
Field	IPO_TRIM							
RESET	U							
R/W	R/W							
Address	Information Page Memory 0022H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:0] IPO_TRIM	**Internal Precision Oscillator Trim Byte** Contains trimming bits for the Internal Precision Oscillator.

Note: The bit values used in Table 86 are set at the factory; no calibration is required.

Table 87. Trim Option Bits at 0003H (TVBO)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				Reserved	VBO_TRIM		
RESET	U				U	1	0	0
R/W	R/W				R/W	R/W		
Address	Information Page Memory 0023H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:3]	**Reserved** These bits are reserved and must be programmed to 11111.
[2] VBO_TRIM	**VBO Trim Values** Contains factory-trimmed values for the oscillator and the VBO.

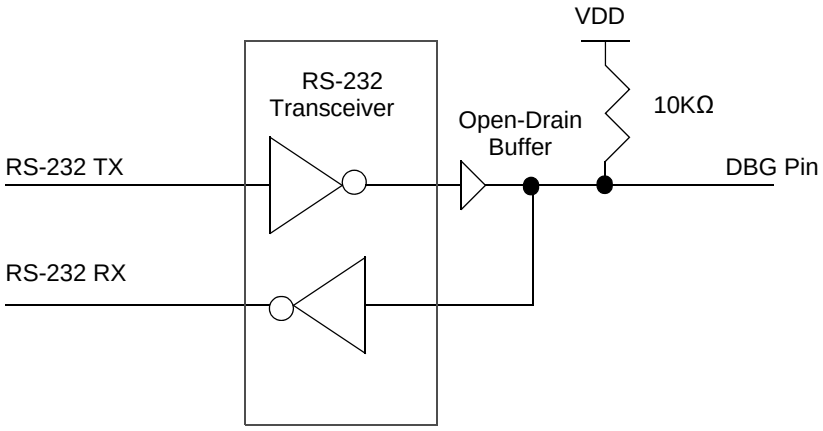

Figure 22. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #2 of 2

DEBUG Mode

The operating characteristics of the devices in DEBUG Mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions
- The system clock operates, unless the device is in STOP Mode
- All enabled on-chip peripherals operate, unless the device is in STOP Mode
- Automatically exits HALT Mode
- Constantly refreshes the Watchdog Timer, if enabled

Entering DEBUG Mode

- The device enters DEBUG Mode after the eZ8 CPU executes a Breakpoint (BRK) instruction
- If the DBG pin is held low during the most recent clock cycle of system reset, the device enters DEBUG Mode on exiting system reset

Exiting DEBUG Mode

The device exits DEBUG Mode following any of these operations:

- Clearing the DBGMODE bit in the OCD Control Register to 0
- Power-On Reset
- Voltage Brown-Out reset

Op Code Maps

A description of the opcode map data and the abbreviations are provided in Figure 28. Table 114 on page 181 lists opcode map abbreviations.

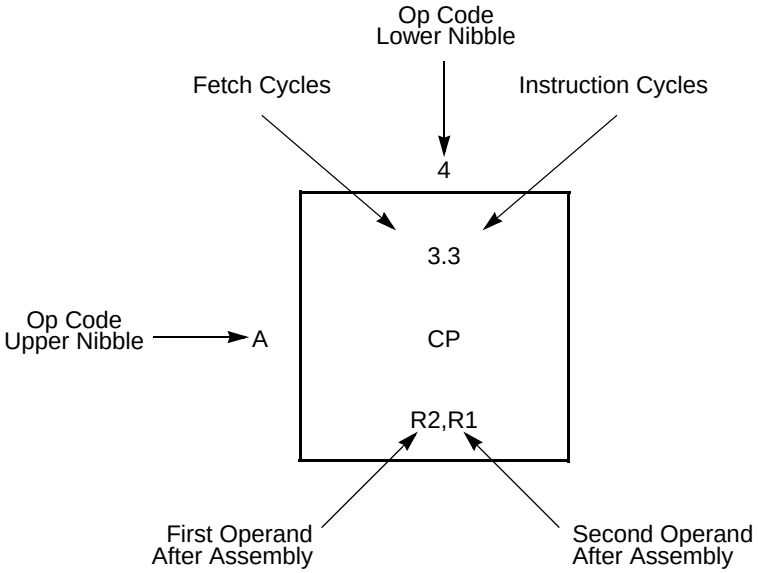

Figure 28. Op Code Map Cell Description

Upper Nibble (Hex) \ Lower Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0																
1																
2																
3																
4																
5																
6																
7	3.2 PUS															
8																
9																
A			3.3 **CPC** r1,r2	3.4 **CPC** r1,Ir2	4.3 **CPC** R2,R1	4.4 **CPC** IR2,R1	4.3 **CPC** R1,IM	4.4 **CPC** IR1,IM	5.3 **CPCX** ER2,ER1	5.3 **CPCX** IM,ER1						
B																
C	3.2 **SRL** R1	3.3 **SRL** IR1														
D																
E									5, 4 **LDWX** ER2,ER1							
F																

Figure 30. Second Op Code Map after 1FH

Table 128. Z8 Encore! XP F0830 Series Ordering Matrix

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8F0831HH020EG	8KB	256	Yes	0	SSOP 20-pin
Z8F0831PH020EG	8KB	256	Yes	0	PDIP 20-pin
Z8F0831QH020EG	8KB	256	Yes	0	QFN 20-pin
Z8F0830SJ020EG	8KB	256	Yes	8	SOIC 28-pin
Z8F0830HJ020EG	8KB	256	Yes	8	SSOP 28-pin
Z8F0830PJ020EG	8KB	256	Yes	8	PDIP 28-pin
Z8F0830QJ020EG	8KB	256	Yes	8	QFN 28-pin
Z8F0831SJ020EG	8KB	256	Yes	0	SOIC 28-pin
Z8F0831HJ020EG	8KB	256	Yes	0	SSOP 28-pin
Z8F0831PJ020EG	8KB	256	Yes	0	PDIP 28-pin
Z8F0831QJ020EG	8KB	256	Yes	0	QFN 28-pin
Z8 Encore! F0830 with 4KB Flash					
Standard Temperature: 0°C to 70°C					
Z8F0430SH020SG	4KB	256	Yes	7	SOIC 20-pin
Z8F0430HH020SG	4KB	256	Yes	7	SSOP 20-pin
Z8F0430PH020SG	4KB	256	Yes	7	PDIP 20-pin
Z8F0430QH020SG	4KB	256	Yes	7	QFN 20-pin
Z8F0431SH020SG	4KB	256	Yes	0	SOIC 20-pin
Z8F0431HH020SG	4KB	256	Yes	0	SSOP 20-pin
Z8F0431PH020SG	4KB	256	Yes	0	PDIP 20-pin
Z8F0431QH020SG	4KB	256	Yes	0	QFN 20-pin
Z8F0430SJ020SG	4KB	256	Yes	8	SOIC 28-pin
Z8F0430HJ020SG	4KB	256	Yes	8	SSOP 28-pin
Z8F0430PJ020SG	4KB	256	Yes	8	PDIP 28-pin
Z8F0430QJ020SG	4KB	256	Yes	8	QFN 28-pin
Z8F0431SJ020SG	4KB	256	Yes	0	SOIC 28-pin
Z8F0431HJ020SG	4KB	256	Yes	0	SSOP 28-pin
Z8F0431PJ020SG	4KB	256	Yes	0	PDIP 28-pin
Z8F0431QJ020SG	4KB	256	Yes	0	QFN 28-pin
Extended Temperature: –40°C to 105°C					
Z8F0430SH020EG	4KB	256	Yes	7	SOIC 20-pin
Z8F0430HH020EG	4KB	256	Yes	7	SSOP 20-pin
Z8F0430PH020EG	4KB	256	Yes	7	PDIP 20-pin

Table 129 lists the pin count by package.

Table 129. Package and Pin Count Description

	Pin Count	
Package	**20**	**28**
PDIP	√	√
QFN	√	√
SOIC	√	√
SSOP	√	√

Appendix A. Register Tables

For the reader's convenience, this appendix lists all F0830 Series registers numerically by hexadecimal address.

General Purpose RAM

In the F0830 Series, the 000–EFF hexadecimal address range is partitioned for general-purpose random access memory, as follows.

Hex Addresses: 000–0FF

This address range is reserved for general-purpose register file RAM. For more details, see the Register File section on page 14.

Hex Addresses: 100–EFF

This address range is reserved.

Timer 0

For more information about these Timer Control registers, see the Timer Control Register Definitions section on page 83.

Hex Address: F00

Table 130. Timer 0 High Byte Register (T0H)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H							

Analog-to-Digital Converter

For more information about these ADC registers, see the ADC Control Register Definitions section on page 101.

Hex Address: F70

Table 146. ADC Control Register 0 (ADCCTL0)

Bit	7	6	5	4	3	2	1	0
Field	START	Reserved	REFEN	ADCEN	Reserved	ANAIN[2:0]		
RESET	0	0	0	0	0	0	0	0
R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F70h							

Bit	Description
[7] START	**ADC Start/Busy** 0 = Writing to 0 has no effect; reading a 0 indicates that the ADC is available to begin a conversion. 1 = Writing to 1 starts a conversion; reading a 1 indicates that a conversion is currently in progress.
[6]	This bit is reserved and must be programmed to 0.
[5] REFEN	**Reference Enable** 0 = Internal reference voltage is disabled allowing an external reference voltage to be used by the ADC. 1 = Internal reference voltage for the ADC is enabled. The internal reference voltage can be measured on the V_{REF} pin.
[4] ADCEN	**ADC Enable** 0 = ADC is disabled for low power operation. 1 = ADC is enabled for normal use.
[3]	This bit is reserved and must be programmed to 0.
[2:0] ANAIN	**Analog Input Select** 000 = ANA0 input is selected for analog to digital conversion. 001 = ANA1 input is selected for analog to digital conversion. 010 = ANA2 input is selected for analog to digital conversion. 011 = ANA3 input is selected for analog to digital conversion. 100 = ANA4 input is selected for analog to digital conversion. 101 = ANA5 input is selected for analog to digital conversion. 110 = ANA6 input is selected for analog to digital conversion. 111 = ANA7 input is selected for analog to digital conversion.

Hex Address: F83

Table 153. LED Drive Level High Register (LEDLVLH)

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F83H							

Hex Address: F84

Table 154. LED Drive Level Low Register (LEDLVLL)

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLL[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F84H							

Hex Address: F85

This address range is reserved.

Oscillator Control

For more information about the Oscillator Control registers, see the Oscillator Control Register Definitions section on page 154.

Hex Address: F86

Table 155. Oscillator Control Register (OSCCTL)

Bit	7	6	5	4	3	2	1	0
Field	INTEN	XTLEN	WDTEN	POFEN	WDFEN	SCKSEL		
RESET	1	0	1	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F86H							

S

T