



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	23
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0830hj020eg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Warning: DO NOT USE THIS PRODUCT IN LIFE SUPPORT SYSTEMS.

LIFE SUPPORT POLICY

ZILOG'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS PRIOR WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF ZILOG CORPORATION.

As used herein

Life support devices or systems are devices which (a) are intended for surgical implant into the body or (b) support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in a significant injury to the user. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system or to affect its safety or effectiveness.

Document Disclaimer

©2012 Zilog, Inc. All rights reserved. Information in this publication concerning the devices, applications or technology described is intended to suggest possible uses and may be superseded. ZILOG, INC. DOES NOT ASSUME LIABILITY FOR OR PROVIDE A REPRESENTATION OF ACCURACY OF THE INFORMATION, DEVICES or TECHNOLOGY DESCRIBED IN THIS DOCUMENT. ZILOG ALSO DOES NOT ASSUME LIABILITY FOR INTELLECTUAL PROPERTY INFRINGEMENT RELATED IN ANY MANNER TO USE OF INFORMATION, DEVICES or TECHNOLOGY DESCRIBED HEREIN OR OTHERWISE. The information contained within this document has been verified according to the general principles of electrical and mechanical engineering.

Z8, Z8 Encore! and Z8 Encore! XP are trademarks or registered trademarks of Zilog, Inc. All other product or service names are the property of their respective owners.

13

Pin Characteristics

Table 5 provides detailed characteristics of each pin available on the Z8 Encore! F0830 Series 20- and 28-pin devices. Data in Table 5 are sorted alphabetically by the pin symbol mnemonic.

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-Up or Pull-Down	Schmitt- Trigger Input	Open Drain Output	5V Tolerance
AV _{DD}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
AV _{SS}	N/A	N/A	N/A	N/A	N/A	N/A	N/A	NA
DBG	I/O	I	N/A	Yes	No	Yes	Yes	Yes
PA[7:0]	I/O	Ι	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PA[7:2] only
PB[7:0]	I/O	I	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PB[7:6] only
PC[7:0]	I/O	Ι	N/A	Yes	Programma- ble pull-up	Yes	Yes, Programma- ble	PC[7:3] only
RESET/PD0	I/O	I/O (defaults <u>to</u> RESET)	Low (in RESET mode)	Yes (PD0 only)	Programma- ble for PD0; always on for RESET	Yes	Programma- ble for PD0; always on for RESET	Yes
V _{DD}	N/A	N/A	N/A	N/A			N/A	N/A
V _{SS}	N/A	N/A	N/A	N/A			N/A	N/A

Table 5. Pin Characteristics (20- and 28-pin Devices)



Note: PB6 and PB7 are available only in devices without an ADC function.

	Reset Characteristics and Latency					
Reset Type	Control Registers	eZ8 CPU	Reset Latency (Delay)			
System Reset	Reset (as applicable)	Reset	About 66 Internal Precision Oscillator Cycles			
System Reset with Crystal Oscillator Enabled	Reset (as applicable)	Reset	About 5000 Internal Precision Oscillator Cycles			
Stop Mode Recovery	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	About 66 Internal Precision Oscillator cycles			
Stop Mode Recovery with crystal oscillator enabled	Unaffected, except WDT_CTL and OSC_CTL registers	Reset	About 5000 Internal Precision Oscillator cycles			

Table 9. Reset and Stop Mode Recovery Characteristics and Latency

During a system RESET or Stop Mode Recovery, the Z8 Encore! F0830 Series device is held in reset for about 66 cycles of the Internal Precision Oscillator. If the crystal oscillator is enabled in the Flash option bits, the reset period is increased to about 5000 IPO cycles. When a reset occurs because of a low voltage condition or Power-On Reset, the reset delay is measured from the time that the supply voltage first exceeds the POR level (discussed later in this chapter). If the external pin reset remains asserted at the end of the reset period, the device remains in reset until the pin is deasserted.

At the beginning of reset, all GPIO pins are configured as inputs with pull-up resistor disabled, except PD0 which is shared with the reset pin. On reset, the Port D0 pin is configured as a bidirectional open-drain reset. This pin is internally driven low during port reset, after which the user code may reconfigure this pin as a general purpose output.

During reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watchdog Timer Oscillator continues to run.

On reset, control registers within the register file that have a defined reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer and Flags) and general purpose RAM are undefined following the reset. The eZ8 CPU fetches the reset vector at program memory addresses 0002H and 0003H and loads that value into the program counter. Program execution begins at the reset vector address.

Because the control registers are reinitialized by a system reset, the system clock after reset is always the IPO. User software must reconfigure the oscillator control block, to enable and select the correct system clock source.

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C ³	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or comparator input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or comparator input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6	ADC analog input	AFS1[2]: 1
	PC3	COUT	Comparator output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1
Port D ¹	PD0	RESET	Default to be Reset function	N/A

Table 16. Port Alternate Function Mapping (Continued)

Notes:

- Because there is only a single alternate function for each Port A and Port D (PD0) pin, the Alternate Function Set registers are not implemented for Port A and Port D (PD0). Enabling alternate function selections (as described in the <u>Port A–D Alternate Function Subregisters</u> section on page 42) automatically enables the associated alternate function.
- Because there are at most two choices of alternate functions for any Port B pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the <u>Port A–D Alternate Function Subregisters</u> section on page 42) must also be enabled.
- Because there are at most two choices of alternate functions for any Port C pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the <u>Port A–D Alternate Function Subregisters</u> section on page 42) must also be enabled.

Port A–D Output Data Register

The Port A–D Output Data Register, shown in Table 30, controls the output data to the pins.

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address			F	D3H, FD7H,	FDBH, FDF	Ή		

Table 30. Port A–D Output Data Register (PxOUT)

Bit Description

[7:0] Port Output Data

PxOUT These bits contain the data to be driven to the port pins. The values are only driven if the corresponding pin is configured as an output and the pin is not configured for Alternate function operation.

0 = Drive a logical 0 (Low).

1= Drive a logical 1 (High). High value is not driven if the drain has been disabled by setting the corresponding port output Control Register bit to 1.

Note: x indicates the specific GPIO port pin number (7–0).



Operation

The timers are 16-bit up-counters. Minimum time-out delay is set by loading the value 0001H into the Timer Reload High and Low Byte registers and setting the prescale value to 1. Maximum time-out delay is set by loading the value 0000H into the Timer Reload High and Low Byte registers and setting the prescale value to 128. If the Timer reaches FFFFH, the timer resets back to 0000H and continues counting.

Timer Operating Modes

The timers can be configured to operate in the following modes:

ONE-SHOT Mode

In ONE-SHOT Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt and the count value in the Timer High and Low Byte registers is reset to 0001H. The timer is automatically disabled and stops counting.

Additionally, if the timer output alternate function is enabled, the timer output pin changes state for one system clock cycle (from Low to High or from High to Low) upon timer

PWM SINGLE OUTPUT Mode

In PWM SINGLE OUTPUT Mode, the timer outputs a pulse width modulated (PWM) output signal through a GPIO port pin. The timer input is the system clock. The timer first counts up to 16-bit PWM match value stored in the timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the timer output toggles. The timer continues counting until it reaches the reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the timer output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The timer output signal returns to a High (1) after the timer reaches the reload value and is reset to 0001H.

If the TPOL bit in the Timer Control Register is set to 0, the timer output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The timer output signal returns to a Low (0) after the timer reaches the reload value and is reset to 0001H.

Observe the following steps for configuring a timer for PWM SINGLE OUTPUT Mode and for initiating PWM operation:

- 1. Write to the Timer Control Register to:
 - Disable the timer
 - Configure the timer for PWM Mode
 - Set the prescale value
 - Set the initial logic level (High or Low) and PWM High/Low transition for the timer output alternate function
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H). This value only affects the first pass in PWM Mode. After the first timer reset in PWM Mode, counting always begins at the reset value of 0001H.
- 3. Write to the PWM High and Low Byte registers to set the PWM value.
- 4. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.
- 5. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 6. Configure the associated GPIO port pin for the timer output alternate function.
- 7. Write to the Timer Control Register to enable the timer and initiate counting.

The PWM period is represented by the following equation:

WDT Reset in Normal Operation

If configured to generate a reset when a time-out occurs, the Watchdog Timer forces the device into the System Reset state. The WDT status bit in the Watchdog Timer Control Register is set to 1. See *the* <u>Reset and Stop Mode Recovery</u> *chapter on page 21* for more information about system reset operations.

WDT Reset in STOP Mode

If configured to generate a reset when a time-out occurs and the device is in STOP Mode, the Watchdog Timer initiates a Stop Mode Recovery. Both the WDT status bit and the STOP bit in the Watchdog Timer Control Register are set to 1 following WDT time-out in STOP Mode. See *the* <u>Reset and Stop Mode Recovery</u> *chapter on page 21* for more information about Stop Mode Recovery operations.

Watchdog Timer Reload Unlock Sequence

Writing the unlock sequence to the Watchdog Timer (WDTCTL) Control Register address, unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address produce no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the reload registers.

The following sequence is required to unlock the Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) for write access:

- 1. Write 55H to the Watchdog Timer Control Register (WDTCTL).
- 2. Write AAH to the Watchdog Timer Control Register (WDTCTL).
- 3. Write the Watchdog Timer Reload Upper Byte Register (WDTU).
- 4. Write the Watchdog Timer Reload High Byte Register (WDTH).
- 5. Write the Watchdog Timer Reload Low Byte Register (WDTL).

All three Watchdog Timer Reload registers must be written in the order listed above. There must be no other register writes between each of these operations. If a register write occurs, the lock state machine resets and no further writes can occur unless the sequence is restarted. The value in the Watchdog Timer Reload registers is loaded into the counter when the Watchdog Timer is first enabled and every time a WDT instruction is executed.

Z8 Encore![®] F0830 Series Product Specification

1FFFH		 Page 15	1FFFH
	Sector 7	Page 14	1DFFH 1C00H
1C00H 18FFH		 Page 13	1BFFH 1A00H
	Sector 6	 Page 12	19FFH 1800H
1800H 17FFH		 Page 11	17FFH 1600H
1400H	Sector 5	 Page 10	15FFH 1400H
13FFH		 Page 9	13FFH
	Sector 4	Page 8	1200H 11FFH
1C00H 0FFFH	Contor 2	Page 7	1C00H 0FFFH
0С00Н	Sector 3	Page 6	0E00H 0DFFH
0BFFH		 Page 5	0C00H 0BFFH
0800H	Sector 2	 Page 4	0A00H 09FFH
07FFH	0 1 1	Page 3	0800H 07FFH
0400H	Sector 1	 Page 2	0600H 05FFH
03FFH	Sector 0	 Page 1	0400H 03FFH
0000H		 Page 0	0200H 0100H
			0000H

Figure 17. 8K Flash with NVDS

110

FHSWP	FWP	Flash Code Protection Description
0	0	Programming and erasing disabled for all Flash program memory. In user code pro- gramming, page erase and mass erase are all disabled. Mass erase is available through the On-Chip Debugger.
0 or 1	1	Programming, page erase and mass erase are enabled for all of the Flash program memory.

Table 71. Flash Code Protection using the Flash Option Bits

At reset, the Flash Controller is locked to prevent accidental program or erasure of Flash memory. To program or erase Flash memory, first write the target page to the page select register. Unlock the Flash Controller by making two consecutive writes to the Flash Control Register with the values 73H and 8CH, sequentially. The page select register must be rewritten with the same page previously stored there. If the two page select writes do not match, the controller reverts to a Locked state. If the two writes match, the selected page becomes active. See Figure 19 for details.

After unlocking a specific page, you can enable either page program or erase. Writing the value 95H causes a page erase only if the active page resides in a sector that is not protected. Any other value written to the Flash Control Register locks the Flash Controller. Mass erase is not allowed in the user code, but is allowed through the debug port.

After unlocking a specific page, the user can also write to any byte on that page. After a byte is written, the page remains unlocked, allowing for subsequent writes to other bytes on the same page. Further writes to the Flash Control Register causes the active page to revert to a Locked state.

Sector Based Flash Protection

The final protection mechanism is implemented on a per-sector basis. The Flash memories of Z8 Encore! devices are divided into maximum number of eight sectors. A sector is oneeighth of the total size of Flash memory, unless this value is smaller than the page size, in which case the sector and page sizes are equal. On Z8 Encore! F0830 Series devices, the sector size is varied according to the Z8 Encore! F0830 Series Flash Memory Configuration shown in Table 69 on page 108 and in Figures 14 through 18, which follow the table

The Flash Sector Protect Register can be configured to prevent sectors from being programmed or erased. After a sector is protected, it cannot be unprotected by user code. The Flash Sector Protect Register is cleared after reset and any previously written protection values is lost. User code must write this register in their initialization routine if they want to enable sector protection.

The Flash Sector Protect Register shares its Register File address with the Page Select Register. The Flash Sector Protect Register is accessed by writing the Flash Control Register with 5EH. After the Flash Sector Protect Register is selected, it can be accessed at the Page Select Register address. When user code writes the Flash Sector Protect Register,

Flash Option Bit Control Register Definitions

This section briefly describes the features of the Trim Bit Address and Data registers.

Trim Bit Address Register

The Trim Bit Address Register, shown in Table 78, contains the target address to access the trim option bits. Trim bit addresses in the range 00h–1Fh map to the information area at addresses 20h–3Fh, as shown in Table 79.

Bit	7	6	5	4	3	2	1	0
Field	TRMADR: Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				FF	6H			

Table 78. Trim Bit Address Register (TRMADR)

Table 79. Thin bit Address Map					
Trim Bit Address	Information Area Address				
00h	20h				
01h	21h				
02h	22h				
03h	23h				
:	:				
1Fh	3Fh				

Table 79. Trim Bit Address Map

Trim Bit Data Register

The Trim Bit Data Register, shown in Table 80, contains the read or write data to access the trim option bits.

Note: The bit values used in Table 87 are set at the factory; no calibration is required.

VBO_TRIM	Trigger Voltage Level
000	1.7
001	1.6
101	2.2
110	2.0
100	2.4
111	1.8

Table 88. VBO Trim Definition

On-chip Flash memory is only guaranteed to perform write operations when voltage supplies exceed 2.7 V. Write operations at voltages below 2.7 V will yield unpredictable results.

Table 89. Trim Option Bits at 0006H (TCLKFLT)

Bit	7	6	5	4	3	2	1	0
Field	DivBy4	Reserved	DlyCtl1	DlyCtl2	DlyCtl3	Reserved	FilterSel1	FilterSel0
RESET	0	1	0	0	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Information Page Memory 0026H							
Note: U = Unchanged by Reset. R/W = Read/Write.								

Bit	Description
[7]	Output Frequency Selection
DivBy4	0 = Output frequency is input frequency.
	1 = Output frequency is 1/4 of the input frequency.
[6]	Reserved
	This bit is reserved and must be programmed to 1.
[5:3]	Delay Control
DlyCtl <i>x</i>	3-bit selection for the pulse width that can be filtered. See Table 90 for Delay Control values at
	3.3V operation voltage.
[2]	Reserved
	This bit is reserved and must be programmed to 1.
Notes: x	indicates bit values 3–1; y indicates bit values 1–0.
-	

>

On-Chip Debugger

The Z8 Encore! devices contain an integrated On-Chip Debugger (OCD) that provides the following advanced debugging features:

- Reading and writing of the register file
- Reading and writing of program and data memory
- Setting of breakpoints and watchpoints
- Executing eZ8 CPU instructions

Architecture

The On-Chip Debugger consists of four primary functional blocks: transmitter, receiver, autobaud detector/generator and debug controller. Figure 20 displays the architecture of the On-Chip Debugger.



Figure 20. On-Chip Debugger Block Diagram

ister, the user code must wait at least 5000 IPO cycles for the crystal to stabilize. After this period, the crystal oscillator may be selected as the system clock.

Figure 25 displays a recommended configuration for connection with an external fundamental-mode, parallel-resonant crystal operating at 20MHz. Recommended 20MHz crystal specifications are provided in Table 100. Resistor R₁ is optional and limits total power dissipation by the crystal. Printed circuit board layout must add no more than 4pF of stray capacitance to either the X_{IN} or X_{OUT} pins. If oscillation does not occur, reduce the values of capacitors C₁ and C₂ to decrease loading.



Figure 25. Recommended 20MHz Crystal Oscillator Configuration

Parameter	Value	Units	Comments
Frequency	20	MHz	
Resonance	Parallel		
Mode	Fundamental		
Series Resistance (R _S)	60	Ω	Maximum
Load Capacitance (CL)	30	pF	Maximum
Shunt Capacitance (C ₀)	7	pF	Maximum
Drive Level	1	mW	Maximum

Table 100. Recommended Crystal Oscillator Specifications

Abbreviation	Description	Abbreviation	Description
b	Bit position	IRR	Indirect Register Pair
CC	Condition code	р	Polarity (0 or 1)
Х	8-bit signed index or displace- ment	r	4-bit Working Register
DA	Destination address	R	8-bit register
ER	Extended Addressing Register	r1, R1, Ir1, Irr1, IR1, rr1, RR1, IRR1, ER1	Destination address
IM	Immediate data value	r2, R2, Ir2, Irr2, IR2, rr2, RR2, IRR2, ER2	Source address
lr	Indirect Working Register	RA	Relative
IR	Indirect Register	rr	Working Register Pair
Irr	Indirect Working Register Pair	RR	Register Pair

Table 114. Op Code Map Abbreviations

	Lower Nibble (Hex)															
	0	1	2	3	4	5	6	7	8	9	А	В	С	D	Е	F
	1.1	2.2	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3	2.3	2.2	2.2	3.2	1.2	1.2
0	BRK	SRP	ADD	ADD	ADD		ADD	ADD			DJNZ	JR	LD	JP	INC	NOP
	2.2	1111	r1,r2	r1,Ir2	R2,R1	1R2,R1	R1,IM	1R1,IM	ERZ,ER1	IM,ER1	r1,X	CC, X	r1,IM	CC,DA	ri	See 2nd
1	RLC	RLC	ADC	ADC	ADC	ADC	ADC	ADC	ADCX	ADCX						Op Code
-	R1	IR1	r1,r2	r1,Ir2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						Map
	2.2	2.3	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						
2			SUB	SUB	SUB P2 P1	SUB			SUBX	SUBX						
	22	23	23	2.4	3.3	3.4	33	3.4	4 3	13						
3	DEC	DEC	SBC	SBC	SBC	SBC	SBC	SBC	SBCX	SBCX						
	R1	IR1	r1,r2	r1,Ir2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
	2.2	2.3	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						
4	DA R1	DA IR1	0R r1 r2	UR	0R R2 R1	UR IR2 R1			ORX ER2 ER1							
	2.2	2.3	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						1.2
5	POP	POP	AND	AND	AND	AND	AND	AND	ANDX	ANDX						WDT
	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
6	2.2 COM	2.3 COM	2.3 TCM	2.4 TCM	3.3 TCM	3.4 TCM	3.3 TCM	3.4 TCM	4.3 TCMX	4.3 TCMX						1.2 STOP
0	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						0101
	2.2	2.3	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						1.2
7	PUSH	PUSH	ТМ	ТМ	ТМ	ТМ	ТМ	ТМ	тмх	ТМХ						HALT
	R2	IR2	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						4.0
8	DECW	DECW	LDE	LDEI		LDX	LDX	LDX	LDX	LDX						DI
-	RR1	IRR1	r1,Irr2	lr1,lrr2	r1,ER2	lr1,ER2	IRR2,R1	IRR2,IR1	r1,rr2,X	rr1,r2,X						
	2.2	2.3	2.5	2.9	3.2	3.3	3.4	3.5	3.3	3.5						1.2
9	RL R1	RL IR1	r2 lrr1	LDEI	r2 FR1	LDX Ir2 ER1			LEA	LEA						EI
	2.5	2.6	2.3	2.4	3.3	3.4	3.3	3.4	4.3	4.3						1.4
А	INCW	INCW	CP	CP	CP	CP	CP	CP	CPX	CPX						RET
	RR1	IRR1	r1,r2	r1,Ir2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
R	2.2 CL R	2.3 CI R	2.3 XOR	2.4 XOR	3.3 XOR	3.4 XOR	3.3 XOR	3.4 XOR	4.3 XORX	4.3 XORX						1.5 IRFT
D	R1	IR1	r1,r2	r1,lr2	R2,R1	IR2,R1	R1,IM	IR1,IM	ER2,ER1	IM,ER1						
	2.2	2.3	2.5	2.9	2.3	2.9		3.4	3.2							1.2
С	RRC	RRC	LDC	LDCI	JP	LDC		LD	PUSHX							RCF
	R1	1R1	r1,Irr2	111,1112		111,1112	2.2	r1,r2,X	ER2							1.0
D	SRA	SRA	LDC	LDCI		BSWAP	CALL	3.4 LD	POPX							SCF
	R1	IR1	r2,Irr1	lr2,lrr1	IRR1	R1	DA	r2,r1,X	ER1							
_	2.2	2.3	2.2	2.3	3.2	3.3	3.2	3.3	4.2	4.2						1.2
F	R1	IR1	BII nhr1	LD r1 lr2	LD R2 R1	LD IR2 R1	R1 IM		ER2 ER1							LCF
	2.2	2.3	2.6	2.3	2.8	3.3	3.3	3.4								
F	SWAP	SWAP	TRAP	LD	MULT	LD	BTJ	BTJ				V		🗡		
	R1	IR1	Vector	lr1 r2	RR1	R2 IR1	nhr1 X	n h lr1 X	1	1		V	I V	I V	I V	1

Figures 29 and 30 provide information about each of the eZ8 CPU instructions.

Figure 29. First Op Code Map

Upper Nibble (Hex)

Figure 31 displays the typical current consumption while operating at 25 $^{\circ}$ C, 3.3V, versus the system clock frequency in HALT Mode.

Figure 31. I_{CC} Versus System Clock Frequency (HALT Mode)

	V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C			V _{DD} = 2.7 to 3.6V T _A = -40°C to +105°C				
Parameter	Min	Тур	Max	Min	Тур	Мах	Units	Notes
NVDS Byte Read Time				71	-	258	μs	Withsystemclockat 20MHz
NVDS Byte Pro- gram Time				126	-	136	μs	Withsystemclockat 20MHz
Data Retention				10	_	_	years	25°C
Endurance				100,000	_	-	cycles	Cumulative write cycles for entire memory

Table 121. Nonvolatile Data Storage

Note: For every 200 writes, a maintenance operation is necessary. In this rare occurrence, the write can take up to 58 ms to complete.

Table 122. Analog-to-Digital Converter Electrical Characteristics and Timing

		V _{DD} = 2.7 to 3.6V T _A = 0°C to +70°C			V _{DD} = 2.7 to 3.6V T _A = -40°C to +105°C			_	
Symbol	Parameter	Min	Тур	Max	Min	Тур	Max	Units	Conditions
	Resolution				_	10	_	bits	
	Differential Nonlinearity (DNL) ¹				-1	_	+4	LSB	
	Integral Nonlinearity (INL) ¹				-5	_	+5	LSB	
	Gain Error					15		LSB	
	Offset Error				-15	_	15	LSB	PDIP package
	=				-9	_	9	LSB	Other packages
V _{REF}	On chip reference				1.9	2.0	2.1	V	
	Active Power Consumption					4		mA	
	Power Down Current						1	μA	

Note: ¹When the input voltage is lower than 20mV, the conversion error is out of spec.

193

>

Analog-to-Digital Converter

For more information about these ADC registers, see the <u>ADC Control Register Defini-</u> tions section on page 101.

Hex Address: F70

Bit	7	6	5	4	3	2	1	0		
Field	START	Reserved	REFEN	ADCEN	Reserved	ANAIN[2:0]				
RESET	0	0	0	0	0	0	0	0		
R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
Address	F70h									

Table 146. ADC Control Register 0 (ADCCTL0)

Bit	Description
[7] START	 ADC Start/Busy 0 = Writing to 0 has no effect; reading a 0 indicates that the ADC is available to begin a conversion. 1 = Writing to 1 starts a conversion; reading a 1 indicates that a conversion is currently in progress.
[6]	This bit is reserved and must be programmed to 0.
[5] REFEN	 Reference Enable 0 = Internal reference voltage is disabled allowing an external reference voltage to be used by the ADC. 1 = Internal reference voltage for the ADC is enabled. The internal reference voltage can be measured on the V_{REF} pin.
[4] ADCEN	ADC Enable 0 = ADC is disabled for low power operation. 1 = ADC is enabled for normal use.
[3]	This bit is reserved and must be programmed to 0.
[2:0] ANAIN	 Analog Input Select 000 = ANA0 input is selected for analog to digital conversion. 001 = ANA1 input is selected for analog to digital conversion. 010 = ANA2 input is selected for analog to digital conversion. 011 = ANA3 input is selected for analog to digital conversion. 100 = ANA4 input is selected for analog to digital conversion. 101 = ANA5 input is selected for analog to digital conversion. 101 = ANA6 input is selected for analog to digital conversion. 111 = ANA7 input is selected for analog to digital conversion.

Z8 Encore![®] F0830 Series Product Specification

Hex Addresses: FC9–FCC

This address range is reserved.

Hex Address: FCD

Table 166. Interrupt Edge Select Register (IRQES)

Bit	7	6	5	4	3	2	1	0			
Field	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0			
RESET	0	0	0	0	0	0	0	0			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
Address		FCDH									

Hex Address: FCE

Table 167. Shared Interrupt Select Register (IRQSS)

Bit	7	6	5	4	3	2	1	0				
Field	Reserved	PA6CS		Reserved								
RESET	0	0	0	0	0	0	0	0				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
Address	FCEH											

Hex Address: FCF

Table 168. Interrupt Control Register (IRQCTL)

Bit	7	6	5	4	3	2	1	0				
Field	IRQE		Reserved									
RESET	0	0	0	0	0	0	0	0				
R/W	R/W	R	R	R	R	R	R	R				
Address			FCFH									