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### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f0830ph020eg">https://www.e-xfl.com/product-detail/zilog/z8f0830ph020eg</a>

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The eZ8 CPU fetches the reset vector at program memory addresses 0002H and 0003H and loads that value into the program counter. Program execution begins at the reset vector address. Following Stop Mode Recovery, the STOP bit in the Reset Status (RSTSTAT) Register is set to 1. Table 11 lists the Stop Mode Recovery sources and resulting actions. The following sections provide more details about each of the Stop Mode Recovery sources.

**Table 11. Stop Mode Recovery Sources and Resulting Action**

Operating Mode	Stop Mode Recovery Source	Action
STOP Mode	Watchdog Timer time-out when configured for Reset	Stop Mode Recovery
	Watchdog Timer time-out when configured for interrupt	Stop Mode Recovery followed by interrupt (if interrupts are enabled)
	Data transition on any GPIO port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery
	Assertion of external $\overline{\text{RESET}}$ Pin	System reset
	Debug pin driven Low	System reset

## Stop Mode Recovery using WDT Time-Out

If the Watchdog Timer times out during STOP Mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status (RSTSTAT) Register, the WDT and STOP bits are set to 1. If the Watchdog Timer is configured to generate an interrupt upon time-out and the Z8 Encore! F0830 Series device is configured to respond to interrupts, the eZ8 CPU services the WDT interrupt request following the normal Stop Mode Recovery sequence.

## Stop Mode Recovery using GPIO Port Pin Transition

Each of the GPIO port pins may be configured as a Stop Mode Recovery input source. If any GPIO pin is enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery. In the Reset Status (RSTSTAT) Register, the STOP bit is set to 1.

---

**!** **Caution:** In STOP Mode, the GPIO Port Input Data registers (PxIN) are disabled. These Port Input Data registers record the port transition only if the signal stays on the port pin through the end of the Stop Mode Recovery delay. As a result, short pulses on the port pin can initiate Stop Mode Recovery without being written to the Port Input Data Register or without initiating an interrupt (if enabled for that pin).

---

## GPIO Interrupts

Many of the GPIO port pins can be used as interrupt sources. Some port pins can be configured to generate an interrupt request on either the rising edge or falling edge of the input pin signal. Other port pin interrupt sources, generate an interrupt when any edge occurs (both rising and falling). See the [Interrupt Controller](#) chapter on page 53 for more information about interrupts using the GPIO pins.

## GPIO Control Register Definitions

Four registers for each port provide access to GPIO control, input data and output data; Table 17 lists these port registers. Use the Port A–D Address and Control registers together to provide access to subregisters for port configuration and control.

**Table 17. GPIO Port Registers and Subregisters**

Port Register Mnemonic	Port Register Name
PxADDR	Port A–D Address Register (selects subregisters)
PxCTL	Port A–D Control Register (provides access to subregisters)
PxIN	Port A–D Input Data Register
PxOUT	Port A–D Output Data Register
Port Subregister Mnemonic	Port Register Name
PxDD	Data Direction
PxAF	Alternate Function
PxOC	Output Control (open-drain)
PxHDE	High Drive Enable
PxSMRE	Stop Mode Recovery Source Enable
PxPUE	Pull-Up Enable
PxAFS1	Alternate Function Set 1
PxAFS2	Alternate Function Set 2

## IRQ1 Enable High and Low Bit Registers

Table 41 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit registers, shown in Tables 42 and 43, form a priority-encoded enabling service for interrupts in the Interrupt Request 1 Register. Priority is generated by setting the bits in each register.

**Table 41. IRQ1 Enable and Priority Encoding**

IRQ1ENH[x]	IRQ1ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

Note: x indicates register bits in the address range 7–0.

**Table 42. IRQ1 Enable High Bit Register (IRQ1ENH)**

Bit	7	6	5	4	3	2	1	0
Field	PA7ENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC4H							

Bit	Description
[7] PA7ENH	Port A Bit[7] Interrupt Request Enable High Bit
[6] PA6CENH	Port A Bit[7] or Comparator Interrupt Request Enable High Bit
[5:0] PAxENH	Port A Bit[x] Interrupt Request Enable High Bit See the interrupt port select register for selection of either Port A or Port D as the interrupt source.

Note: x indicates register bits in the address range 5–0.

Bit	Description (Continued)
[2:0]	<b>Timer Mode</b>
TMODE	<p>This field along with the TMODEHI bit in TxCTL0 register determines the operating mode of the timer. TMODEHI is the most significant bit of the timer mode selection value.</p> <p>0000 = ONE-SHOT Mode.  0001 = CONTINUOUS Mode.  0010 = COUNTER Mode.  0011 = PWM SINGLE OUTPUT Mode.  0100 = CAPTURE Mode.  0101 = COMPARE Mode.  0110 = GATED Mode.  0111 = CAPTURE/COMPARE Mode.  1000 = PWM DUAL OUTPUT Mode.  1001 = CAPTURE RESTART Mode.  1010 = COMPARATOR COUNTER Mode.</p>

## Watchdog Timer Control Register Definitions

This section defines the features of the following Watchdog Timer Control registers.

Watchdog Timer Control Register (WDTCTL): see page 95

Watchdog Timer Reload Low Byte Register (WDTL): see page 97

Watchdog Timer Reload Upper Byte Register (WDTU): see page 96

Watchdog Timer Reload High Byte Register (WDTH): see page 96

### Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) Register is a write-only control register. Writing the unlock sequence: 55H, AAH to the WDTCTL Register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address have no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the reload registers.

This register address is shared with the read-only Reset Status Register.

**Table 59. Watchdog Timer Control Register (WDTCTL)**

Bit	7	6	5	4	3	2	1	0
Field	WDTUNLK							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
Address	FF0H							

Bit	Description
[7:0] WDTUNLK	<b>Watchdog Timer Unlock</b> The user software must write the correct unlocking sequence to this register before it is allowed to modify the contents of the Watchdog Timer Reload registers.



**Table 62. Watchdog Timer Reload Low Byte Register (WDTL)**

Bit	7	6	5	4	3	2	1	0
Field	WDTL							
RESET	0	0	0	0	0	0	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF3H							
Note: *A read returns the current WDT count value; a write sets the appropriate reload value.								

Bit	Description
[7:0]	<b>WDT Reload Low</b>
WDTL	Least significant byte (LSB), bits[7:0] of the 24-bit WDT reload value.

# Comparator

The Z8 Encore! F0830 Series devices feature a general purpose comparator that compares two analog input signals. A GPIO (CINP) pin provides the positive comparator input. The negative input (CINN) can be taken from either an external GPIO pin or from an internal reference. The output is available as an interrupt source or can be routed to an external pin using the GPIO multiplex. The comparator includes the following features:

- Positive input is connected to a GPIO pin
- Negative input can be connected to either a GPIO pin or a programmable internal reference
- Output can be either an interrupt source or an output to an external pin

## Operation

One of the comparator inputs can be connected to an internal reference that is a user-selectable reference and is user-programmable with 200mV resolution.

The comparator can be powered down to save supply current. For details, see the [Power Control Register 0](#) section on page 31.

---

**! Caution:** As a result of the propagation delay of the comparator, Zilog does not recommend enabling the comparator without first disabling interrupts and waiting for the comparator output to settle. This delay prevents spurious interrupts after comparator enabling.

---

The following example shows how to safely enable the comparator:

```
di
ld cmp0,r0; load some new configuration
nop
nop      ; wait for output to settle
clr irq0 ; clear any spurious interrupts pending
ei
```

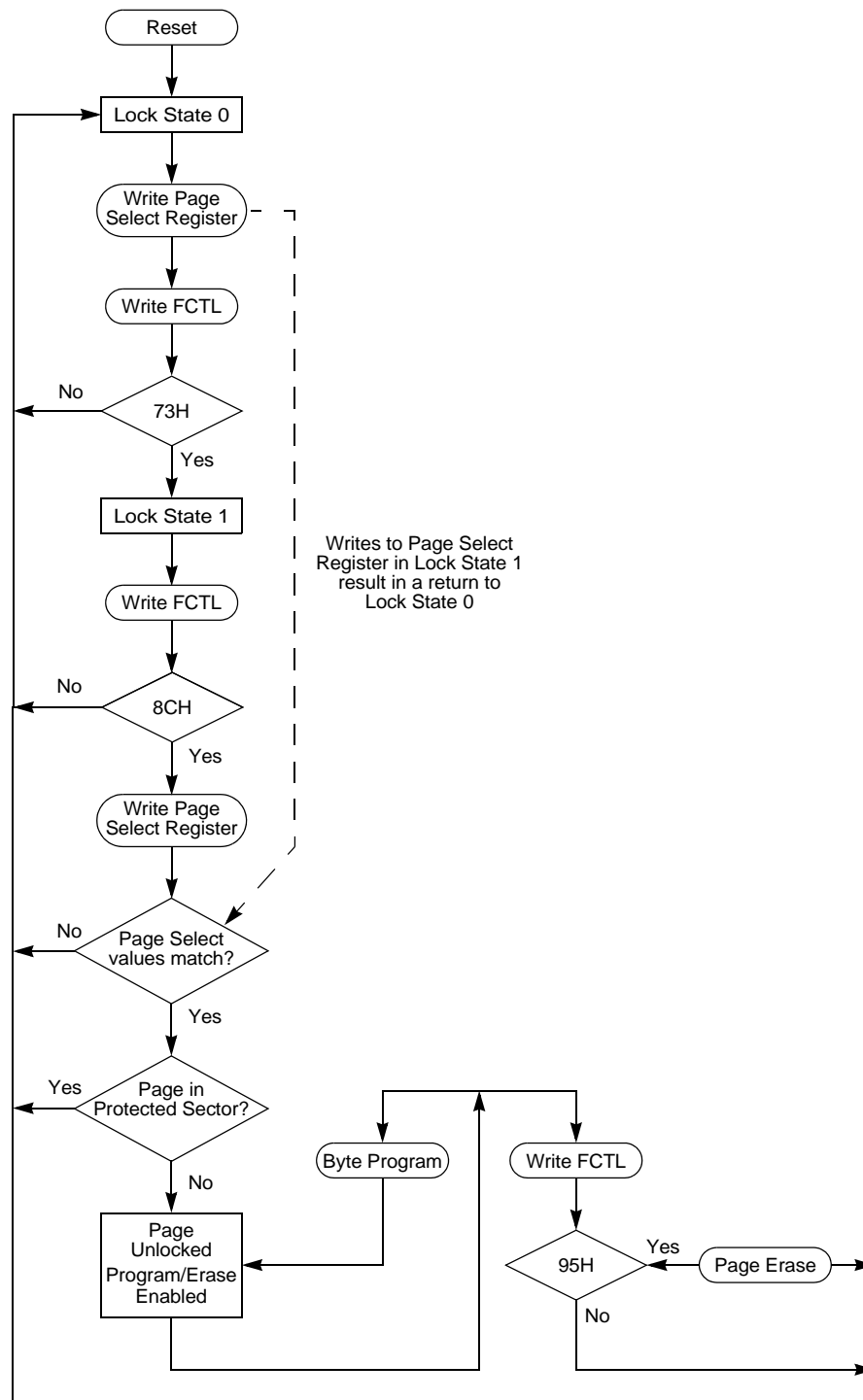


Figure 19. Flash Controller Operation Flow Chart

## Runtime Counter

The OCD contains a 16-bit runtime counter. It counts system clock cycles between break-points. The counter starts counting when the OCD leaves DEBUG Mode and stops counting when it enters DEBUG Mode again or when it reaches the maximum count of FFFFH.

## On-Chip Debugger Commands

The host communicates to the On-Chip Debugger by sending OCD commands using the DBG interface. During normal operation, only a subset of the OCD commands are available. In DEBUG Mode, all OCD commands become available unless the user code and control registers are protected by programming the Flash read protect option bit (FRP). The FRP prevents the code in memory from being read out of the Z8 Encore! F0830 Series products. When this option is enabled, several of the OCD commands are disabled.

Table 95 summarizes the On-Chip Debugger commands. This table indicates the commands that operate when the device is not in DEBUG Mode (normal operation) and the commands that are disabled by programming the FRP.

**Table 95. On-Chip Debugger Command Summary**

Debug Command	Command Byte	Enabled when not in DEBUG Mode?	Disabled by Flash Read Protect Option Bit
Read OCD Revision	00H	Yes	—
Reserved	01H	—	—
Read OCD Status Register	02H	Yes	—
Read Runtime Counter	03H	—	—
Write OCD Control Register	04H	Yes	Cannot clear DBGMODE bit
Read OCD Control Register	05H	Yes	—
Write Program Counter	06H	—	Disabled
Read Program Counter	07H	—	Disabled
Write Register	08H	—	Only writes of the Flash Memory Control registers are allowed. Additionally, only the Mass Erase command is allowed to be written to the Flash Control register.
Read Register	09H	—	Disabled
Write Program Memory	0AH	—	Disabled
Read Program Memory	0BH	—	Disabled
Write Data Memory	0CH	—	Yes
Read Data Memory	0DH	—	—

**Read OCD Control Register (05H).** The read OCD Control Register command reads the value of the OCDCTL register.

```
DBG ← 05H
DBG → OCDCTL[7:0]
```

**Write Program Counter (06H).** The write program counter command, writes the data that follows to the eZ8 CPU's program counter (PC). If the device is not in DEBUG Mode or if the Flash read protect option bit is enabled, the program counter (PC) values are discarded.

```
DBG ← 06H
DBG ← ProgramCounter[15:8]
DBG ← ProgramCounter[7:0]
```

**Read Program Counter (07H).** The read program counter command, reads the value in the eZ8 CPU's program counter (PC). If the device is not in DEBUG Mode or if the Flash read protect option bit is enabled, this command returns FFFFH.

```
DBG ← 07H
DBG → ProgramCounter[15:8]
DBG → ProgramCounter[7:0]
```

**Write Register (08H).** The write register command, writes data to the register file. Data can be written 1–256 bytes at a time (256 bytes can be written by setting size to 0). If the device is not in DEBUG Mode, the address and data values are discarded. If the Flash read protect option bit is enabled, only writes to the Flash control registers are allowed and all other register write data values are discarded.

```
DBG ← 08H
DBG ← {4'h0, Register Address[11:8]}
DBG ← Register Address[7:0]
DBG ← Size[7:0]
DBG ← 1-256 data bytes
```

**Read Register (09H).** The read register command, reads data from the register file. Data can be read 1–256 bytes at a time (256 bytes can be read by setting size to 0). If the device is not in DEBUG Mode or if the Flash read protect option bit is enabled, this command returns FFH for all of the data values.

```
DBG ← 09H
DBG ← {4'h0, Register Address[11:8]}
DBG ← Register Address[7:0]
DBG ← Size[7:0]
DBG → 1-256 data bytes
```

**Write Program Memory (0AH).** The write program memory command, writes data to program memory. This command is equivalent to the LDC and LDCI instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). The on-chip Flash Controller must be written to and unlocked for the programming operation to occur. If the Flash Controller is not unlocked, the data is discarded. If the device is not in DEBUG Mode or if the Flash read protect option bit is enabled, the data is discarded.

# Oscillator Control

The Z8 Encore! F0830 Series device uses five possible clocking schemes. Each one of these is user-selectable.

- On-chip precision trimmed RC oscillator
- On-chip oscillator using off-chip crystal or resonator
- On-chip oscillator using external RC network
- External clock drive
- On-chip low precision Watchdog Timer Oscillator

In addition, Z8 Encore! F0830 Series devices contain clock failure detection and recovery circuitry, allowing continued operation despite a failure of the primary oscillator.

## Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures. A description of the specific operation of each oscillator is outlined further in this document.

## System Clock Selection

The oscillator control block selects from the available clocks. *Table 98* describes each clock source and its usage.

Table 110. Logical Instructions

Mnemonic	Operands	Instruction
AND	dst, src	Logical AND
ANDX	dst, src	Logical AND using Extended Addressing
COM	dst	Complement
OR	dst, src	Logical OR
ORX	dst, src	Logical OR using Extended Addressing
XOR	dst, src	Logical Exclusive OR
XORX	dst, src	Logical Exclusive OR using Extended Addressing

Table 111. Program Control Instructions

Mnemonic	Operands	Instruction
BRK	—	On-chip Debugger Break
BTJ	p, bit, src, DA	Bit Test and Jump
BTJNZ	bit, src, DA	Bit Test and Jump if Non-Zero
BTJZ	bit, src, DA	Bit Test and Jump if Zero
CALL	dst	Call Procedure
DJNZ	dst, src, RA	Decrement and Jump Non-Zero
IRET	—	Interrupt Return
JP	dst	Jump
JP cc	dst	Jump Conditional
JR	DA	Jump Relative
JR cc	DA	Jump Relative Conditional
RET	—	Return
TRAP	vector	Software Trap

Table 112. Rotate and Shift Instructions

Mnemonic	Operands	Instruction
BSWAP	dst	Bit Swap
RL	dst	Rotate Left
RLC	dst	Rotate Left through Carry

**Table 128. Z8 Encore! XP F0830 Series Ordering Matrix**

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8F1233QH020EG	12KB	256	No	0	QFN 20-pin
Z8F1232SJ020EG	12KB	256	No	8	SOIC 28-pin
Z8F1232HJ020EG	12KB	256	No	8	SSOP 28-pin
Z8F1232PJ020EG	12KB	256	No	8	PDIP 28-pin
Z8F1232QJ020EG	12KB	256	No	8	QFN 28-pin
Z8F1233SJ020EG	12KB	256	No	0	SOIC 28-pin
Z8F1233HJ020EG	12KB	256	No	0	SSOP 28-pin
Z8F1233PJ020EG	12KB	256	No	0	PDIP 28-pin
Z8F1233QJ020EG	12KB	256	No	0	QFN 28-pin
<b>Z8 Encore! F0830 with 8KB Flash</b>					
<b>Standard Temperature: 0°C to 70°C</b>					
Z8F0830SH020SG	8KB	256	Yes	7	SOIC 20-pin
Z8F0830HH020SG	8KB	256	Yes	7	SSOP 20-pin
Z8F0830PH020SG	8KB	256	Yes	7	PDIP 20-pin
Z8F0830QH020SG	8KB	256	Yes	7	QFN 20-pin
Z8F0831SH020SG	8KB	256	Yes	0	SOIC 20-pin
Z8F0831HH020SG	8KB	256	Yes	0	SSOP 20-pin
Z8F0831PH020SG	8KB	256	Yes	0	PDIP 20-pin
Z8F0831QH020SG	8KB	256	Yes	0	QFN 20-pin
Z8F0830SJ020SG	8KB	256	Yes	8	SOIC 28-pin
Z8F0830HJ020SG	8KB	256	Yes	8	SSOP 28-pin
Z8F0830PJ020SG	8KB	256	Yes	8	PDIP 28-pin
Z8F0830QJ020SG	8KB	256	Yes	8	QFN 28-pin
Z8F0831SJ020SG	8KB	256	Yes	0	SOIC 28-pin
Z8F0831HJ020SG	8KB	256	Yes	0	SSOP 28-pin
Z8F0831PJ020SG	8KB	256	Yes	0	PDIP 28-pin
Z8F0831QJ020SG	8KB	256	Yes	0	QFN 28-pin
<b>Extended Temperature: -40°C to 105°C</b>					
Z8F0830SH020EG	8KB	256	Yes	7	SOIC 20-pin
Z8F0830HH020EG	8KB	256	Yes	7	SSOP 20-pin
Z8F0830PH020EG	8KB	256	Yes	7	PDIP 20-pin
Z8F0830QH020EG	8KB	256	Yes	7	QFN 20-pin
Z8F0831SH020EG	8KB	256	Yes	0	SOIC 20-pin



Table 129 lists the pin count by package.

**Table 129. Package and Pin Count Description**

<b>Package</b>	<b>Pin Count</b>	
	<b>20</b>	<b>28</b>
PDIP	√	√
QFN	√	√
SOIC	√	√
SSOP	√	√

**Hex Address: F05**

**Table 135. Timer 0 PWM Low Byte Register (T0PWML)**

Bit	7	6	5	4	3	2	1	0
Field	PWML							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F05H							

**Hex Address: F06**

**Table 136. Timer 0 Control Register 0 (T0CTL0)**

Bit	7	6	5	4	3	2	1	0
Field	TMODEHI	TICONFIG		Reserved	PWMD			INPCAP
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F06H							

**Hex Address: F07**

**Table 137. Timer 0 Control Register 1 (T0CTL1)**

Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F07H							

**Hex Address: F08**

**Table 138. Timer 1 High Byte Register (T1H)**

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F08H							

**Hex Addresses: F87–F8F**

This address range is reserved.

## Comparator 0

For more information about the Comparator Register, see the [Comparator Control Register Definitions](#) section on page 107.

**Hex Address: F90****Table 156. Comparator Control Register (CMP0)**

Bit	7	6	5	4	3	2	1	0
Field	Reserved	INNSEL	REFLVL				Reserved	
RESET	0	0	0	1	0	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F90H							

**Hex Addresses: F91–FBF**

This address range is reserved.

## Interrupt Controller

For more information about the Interrupt Control registers, see the [Interrupt Control Register Definitions](#) section on page 57.

**Hex Address: FC0****Table 157. Interrupt Request 0 Register (IRQ0)**

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1I	T0I	Reserved	Reserved	Reserved	Reserved	ADCI
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC0H							

**Hex Address: FD3**

**Table 172. Port A Output Data Register (PAOUT)**

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD3H							

**Hex Address: FD4**

**Table 173. Port B GPIO Address Register (PBADDR)**

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD4H							

**Hex Address: FD5**

**Table 174. Port B Control Registers (PBCTL)**

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FD5H							

**Hex Address: FD6**

**Table 175. Port B Input Data Registers (PBIN)**

Bit	7	6	5	4	3	2	1	0
Field	PIN7	PIN6	PIN5	PIN4	PIN3	PIN2	PIN1	PIN0
RESET	X	X	X	X	X	X	X	X
R/W	R	R	R	R	R	R	R	R
Address	FD6H							

### Hex Address: FF1

**Table 186. Watchdog Timer Reload Upper Byte Register (WDTU)**

Bit	7	6	5	4	3	2	1	0
Field	WDTU							
RESET	0	0	0	0	0	0	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF1H							
Note: *Read returns the current WDT count value; write sets the appropriate reload value.								

### Hex Address: FF2

**Table 187. Watchdog Timer Reload High Byte Register (WDTH)**

Bit	7	6	5	4	3	2	1	0
Field	WDTH							
RESET	0	0	0	0	0	1	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF2H							
Note: *Read returns the current WDT count value; write sets the appropriate reload value.								

### Hex Address: FF3

**Table 188. Watchdog Timer Reload Low Byte Register (WDTL)**

Bit	7	6	5	4	3	2	1	0
Field	WDTL							
RESET	0	0	0	0	0	0	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF3H							
Note: *Read returns the current WDT count value; write sets the appropriate reload value.								

### Hex Addresses: FF4–FF5

This address range is reserved.