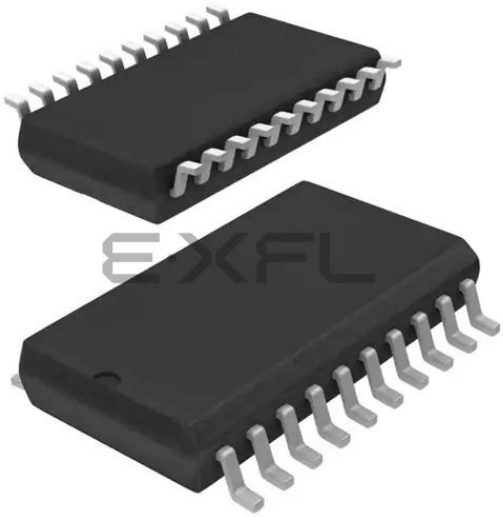

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0830sh020sg

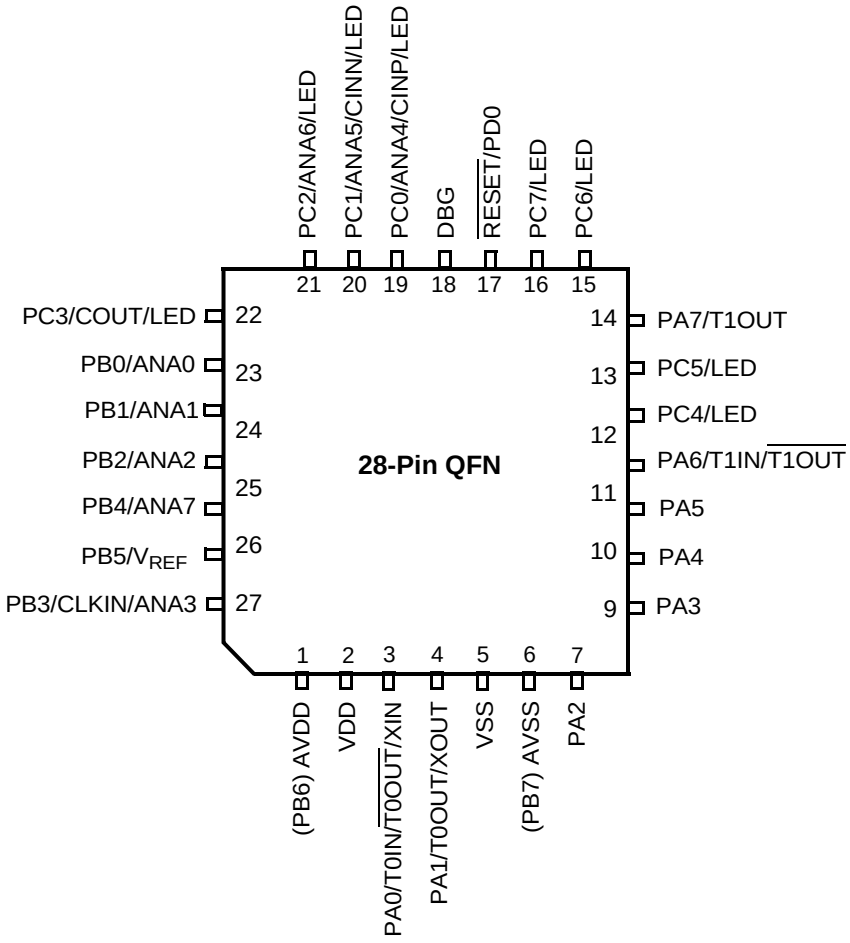

Figure 5. Z8F0830 Series in 28-Pin QFN Package

Signal Descriptions

Table 4 describes the Z8 Encore! F0830 Series signals. See the Pin Configurations section on page 7 to determine the signals available for each specific package style.

Table 4. Signal Descriptions

Signal Mnemonic	I/O	Description
General-Purpose I/O Ports A–D		
PA[7:0]	I/O	Port A. These pins are used for general purpose I/O.
PB[7:0]	I/O	Port B. These pins are used for general purpose I/O. PB6 and PB7 are available only in those devices without an ADC.
PC[7:0]	I/O	Port C. These pins are used for general purpose I/O.
PD[0]	I/O	Port D. This pin is used for general purpose output only.
Note: PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_{DD} and AV_{SS}.		
Timers		
T0OUT/T1OUT	O	Timer output 0–1. These signals are the output from the timers.
$\overline{T0OUT}$/$\overline{T1OUT}$	O	Timer complement output 0–1. These signals are output from the timers in PWM DUAL OUTPUT Mode.
T0IN/T1IN	I	Timer Input 0–1. These signals are used as the capture, gating and counter inputs. The T0IN signal is multiplexed $\overline{T0OUT}$ signals.
Comparator		
CINP/CINN	I	Comparator inputs. These signals are the positive and negative inputs to the comparator.
COUT	O	Comparator output. This is the output of the comparator.
Analog		
ANA[7:0]	I	Analog port. These signals are used as inputs to the analog-to-digital converter (ADC).
V_{REF}	I/O	Analog-to-digital converter reference voltage input. **Note:** When configuring ADC using external V_{REF}, PB5 is used as V_{REF} in 28-pin package.
Note: The AV_{DD} and AV_{SS} signals are available only in the 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.		

Table 4. Signal Descriptions (Continued)

Signal Mnemonic	I/O	Description
Oscillators		
X_{IN}	I	External crystal input. This is the input pin to the crystal oscillator. A crystal can be connected between it and the **XOUT** pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock.
X_{OUT}	O	External crystal output. This pin is the output of the crystal oscillator. A crystal can be connected between it and the **XIN** pin to form the oscillator.
Clock Input		
CLK_{IN}	I	Clock input signal. This pin may be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	O	Direct LED drive capability. All Port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the On-Chip Debugger. **Caution:** The DBG pin is open-drain and requires an external pull-up resistor to ensure proper operation.
Reset		
$\overline{RESET}$	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! forces this pin low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V_{DD}	I	Digital power supply.
AV_{DD}	I	Analog power supply.
V_{SS}	I	Digital ground.
AV_{SS}	I	Analog ground.

Note: The AV_{DD} and AV_{SS} signals are available only in the 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

The Voltage Brown-Out circuit can be either enabled or disabled during STOP Mode. Operations during STOP Mode is set by the VBO_AO Flash option bit. See the Flash Option Bits chapter on page 124 for information about configuring VBO_AO.

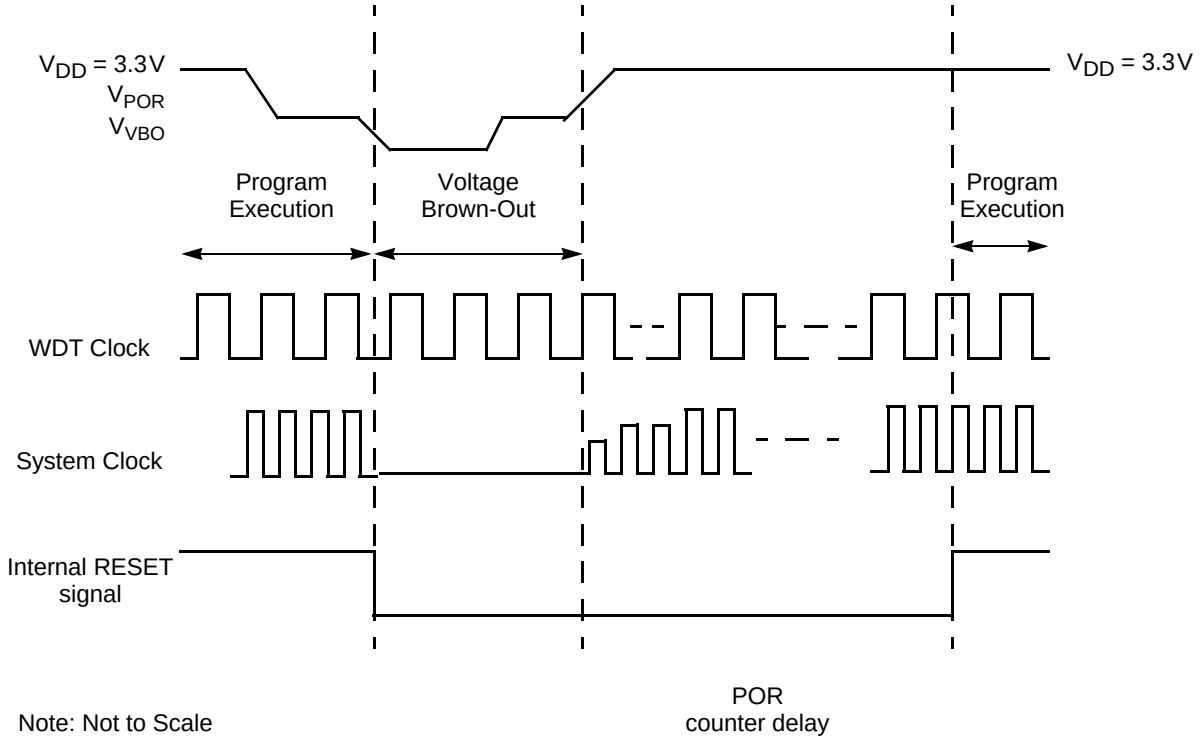

Figure 7. Voltage Brown-Out Reset Operation

Watchdog Timer Reset

If the device is operating in NORMAL or STOP Mode, the Watchdog Timer can initiate a system reset at time-out if the WDT_RES Flash option bit is programmed to 1; this state is the unprogrammed state of the WDT_RES Flash option bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt – not a system reset – at time-out. The WDT status bit in the Reset Status (RSTSTAT) Register is set to 1 to signify that the reset was initiated by the Watchdog Timer.

External Reset Input

The $\overline{\text{RESET}}$ pin has a Schmitt-triggered input and an internal pull-up resistor. After the $\overline{\text{RESET}}$ pin is asserted for a minimum of four system clock cycles, the device progresses through the system reset sequence. Because of the possible asynchronicity of the system

General Purpose Input/Output

The Z8 Encore! F0830 Series products support a maximum of 25 port pins (Ports A–D) for General Purpose Input/Output (GPIO) operations. Each port contains control and data registers. The GPIO control registers determine data direction, open-drain, output drive current, programmable pull-ups, Stop Mode Recovery functionality and alternate pin functions. Each port pin is individually programmable. In addition, the Port C pins are capable of direct LED drive at programmable drive strengths.

GPIO Port Availability by Device

Table 15 lists the port pins available with each device and package type.

Table 15. Port Availability by Device and Package Type

Devices	Package	10-Bit ADC	Port A	Port B	Port C	Port D	Total I/O
Z8F1232, Z8F0830, Z8F0430, Z8F0230, Z8F0130	20-pin	Yes	[7:0]	[3:0]	[3:0]	[0]	17
Z8F1233, Z8F0831 Z8F0431, Z8F0231 Z8F0131	20-pin	No	[7:0]	[3:0]	[3:0]	[0]	17
Z8F1232, Z8F0830, Z8F0430, Z8F0230, Z8F0130	28-pin	Yes	[7:0]	[5:0]	[7:0]	[0]	23
Z8F1233, Z8F0831 Z8F0431, Z8F0231 Z8F0131	28-pin	No	[7:0]	[7:0]	[7:0]	[0]	25

Note: 20-pin and 28-pin and 10-bit ADC Enabled or Disabled can be selected via the option bits.

External Clock Setup

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for Alternate function CLKIN. Write to the Oscillator Control Register (see the Oscillator Control Register Definitions section on page 154) to select the PB3 as the system clock.

Table 16. Port Alternate Function Mapping

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port A[1]	PA0	T0IN/$\overline{\text{T0OUT}}$	Timer 0 input/Timer 0 output complement	N/A
		Reserved		
	PA1	T0OUT	Timer 0 output	
		Reserved		
	PA2	Reserved	Reserved	
		Reserved		
	PA3	Reserved	Reserved	
		Reserved		
	PA4	Reserved	Reserved	
		Reserved		
	PA5	Reserved	Reserved	
		Reserved		
	PA6	T1IN/$\overline{\text{T1OUT}}$	Timer 1 input/Timer 1 output complement	
		Reserved		
	PA7	T1OUT	Timer 1 output	
		Reserved		

Notes:
1. Because there is only a single alternate function for each Port A and Port D (PD0) pin, the Alternate Function Set registers are not implemented for Port A and Port D (PD0). Enabling alternate function selections (as described in the Port A–D Alternate Function Subregisters section on page 42) automatically enables the associated alternate function.
2. Because there are at most two choices of alternate functions for any Port B pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the Port A–D Alternate Function Subregisters section on page 42) must also be enabled.
3. Because there are at most two choices of alternate functions for any Port C pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the Port A–D Alternate Function Subregisters section on page 42) must also be enabled.

Port A–D Output Control Subregisters

The Port A–D Output Control Subregister, shown in Table 23, is accessed through the Port A–D Control Register by writing 03H to the Port A–D Address Register. Setting the bits in the Port A–D Output Control subregisters to 1 configures the specified port pins for open-drain operation. These subregisters affect the pins directly and, as a result, alternate functions are also affected.

Table 23. Port A–D Output Control Subregisters (PxOC)

Bit	7	6	5	4	3	2	1	0
Field	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 03H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0] POCx	**Port Output Control** These bits function independently of the Alternate function bit and always disable the drains, if set to 1. 0 = The drains are enabled for any OUTPUT Mode (unless overridden by the Alternate function). 1 = The drain of the associated pin is disabled (OPEN-DRAIN mode).

Note: x indicates the specific GPIO port pin number (7–0).

IRQ1 Enable High and Low Bit Registers

Table 41 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit registers, shown in Tables 42 and 43, form a priority-encoded enabling service for interrupts in the Interrupt Request 1 Register. Priority is generated by setting the bits in each register.

Table 41. IRQ1 Enable and Priority Encoding

IRQ1ENH[*x*]	IRQ1ENL[*x*]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

Note: *x* indicates register bits in the address range 7–0.

Table 42. IRQ1 Enable High Bit Register (IRQ1ENH)

Bit	7	6	5	4	3	2	1	0
Field	PA7ENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC4H							

Bit	Description
[7] PA7ENH	**Port A Bit[7] Interrupt Request Enable High Bit**
[6] PA6CENH	**Port A Bit[7] or Comparator Interrupt Request Enable High Bit**
[5:0] PA*x*ENH	**Port A Bit[*x*] Interrupt Request Enable High Bit** See the interrupt port select register for selection of either Port A or Port D as the interrupt source.

Note: *x* indicates register bits in the address range 5–0.

Shared Interrupt Select Register

The shared interrupt select (IRQSS) register determines the source of the PADxS interrupts. See Table 48. The shared interrupt select register selects between Port A and alternate sources for the individual interrupts.

Because these shared interrupts are edge-triggered, it is possible to generate an interrupt just by switching from one shared source to another. For this reason, an interrupt must be disabled before switching between sources.

Table 48. Shared Interrupt Select Register (IRQSS)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	PA6CS	Reserved					
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FCEH							

Bit	Description
[7]	**Reserved** This bit is reserved and must be programmed to 0.
[6] PA6CS	**PA6/Comparator Selection** 0 = PA6 is used for the interrupt caused by PA6CS interrupt request. 1 = The comparator is used for the interrupt caused by PA6CS interrupt request.
[5:0]	**Reserved** These registers are reserved and must be programmed to 000000.

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$$

If TPOL is set to 1, the ratio of the PWM output high time to the total period is represented by:

$$\text{PWM Output High Time Ratio (\%)} = \frac{\text{PWM Value}}{\text{Reload Value}} \times 100$$

CAPTURE Mode

In CAPTURE Mode, the current timer count value is recorded when the appropriate external timer input transition occurs. The capture count value is written to the timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines if the capture occurs on a rising edge or a falling edge of the timer input signal.

When the capture event occurs, an interrupt is generated and the timer continues counting. The INPCAP bit in the TxCTL1 Register is set to indicate the timer interrupt because of an input capture event.

The timer continues counting up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt and continues counting. The INPCAP bit in the TxCTL1 Register clears, indicating that the timer interrupt has not occurred because of an input capture event.

Observe the following steps for configuring a timer for CAPTURE Mode and initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for CAPTURE Mode
   - Set the prescale value
   - Set the capture edge (rising or falling) for the timer input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Clear the timer PWM High and Low Byte registers to 0000H. Clearing these registers allows user software to determine if interrupts were generated either by a capture event or by a reload. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt were generated by a reload.

5. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and Reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting the TICONFIG field of the TxCTL1 Register.
6. Configure the associated GPIO port pin for the timer input alternate function.
7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time between the timer start and the capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

CAPTURE RESTART Mode

In CAPTURE RESTART Mode, the current timer count value is recorded when the acceptable external timer input transition occurs. The capture count value is written to the timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines whether the capture occurs on a rising edge or a falling edge of the timer input signal. When the capture event occurs, an interrupt is generated and the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in the TxCTL1 Register is set to indicate that the timer interrupt has been caused by an input capture event.

If no capture event occurs, the timer counts up to 16-bit compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in the TxCTL1 Register is cleared to indicate that the timer interrupt has not been caused by an input capture event.

Observe the following steps for configuring a timer for CAPTURE RESTART Mode and for initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for CAPTURE RESTART Mode; setting the mode also involves writing to TMODEHI bit in the TxCTL1 Register
   - Set the prescale value
   - Set the capture edge (rising or falling) for the timer input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).

tion and reload events. The user can configure the timer interrupt to be generated only at the input deassertion event or the reload event by setting the TICONFIG field of the TxCTL1 Register.

5. Configure the associated GPIO port pin for the timer input alternate function.
6. Write to the Timer Control Register to enable the timer.
7. Assert the timer input signal to initiate the counting.

CAPTURE/COMPARE Mode

In CAPTURE/COMPARE Mode, the timer begins counting on the first external timer input transition. The acceptable transition (rising edge or falling edge) is set by the TPOL bit in the Timer Control Register. The timer input is the system clock.

Every subsequent acceptable transition (after the first) of the timer input signal, captures the current count value. The capture value is written to the timer PWM High and Low Byte registers. When the capture event occurs, an interrupt is generated, the count value in the Timer High and Low Byte registers is reset to 0001H and the counting resumes. The INPCAP bit in the TxCTL1 Register is set to indicate that the timer interrupt is caused by an input capture event.

If no capture event occurs, the timer counts up to the 16-bit compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the compare value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in the TxCTL1 Register is cleared to indicate that the timer interrupt has not been caused by an input capture event.

Observe the following steps for configuring a timer for CAPTURE/COMPARE Mode and for initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for CAPTURE/COMPARE Mode.
   - Set the prescale value.
   - Set the capture edge (rising or falling) for the timer input.
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).
3. Write to the Timer Reload High and Low Byte registers to set the compare value.
4. Enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.By default, the timer interrupt are generated for both input capture and Reload events. The user can configure the timer interrupt to be generated only at the input capture event or the reload event by setting TICONFIG field of the TxCTL1 Register.
5. Configure the associated GPIO port pin for the timer input alternate function.

Timer Control Register Definitions

This section defines the features of the following Timer Control registers.

Timer 0–1 High and Low Byte Registers: see page 83

Timer Reload High and Low Byte Registers: see page 85

Timer 0–1 PWM High and Low Byte Registers: see page 86

Timer 0–1 Control Registers: see page 87

Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers, shown in Tables 50 and 51, contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register content when the timer is enabled; however, when the timer is disabled, a read from the TxL reads the TxL Register content directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations; therefore, simultaneous 16-bit writes are not possible. If either the timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low byte) at the next clock edge. The counter continues counting from the new value.

Table 50. Timer 0–1 High Byte Register (TxH)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H, F08H							

Table 51. Timer 0–1 Low Byte Register (TxL)

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H, F09H							

Watchdog Timer Reload Upper, High and Low Byte Registers

The Watchdog Timer Reload Upper, High and Low Byte (WDTU, WDTH, WDTL) registers, shown in Tables 60 through 62, form the 24-bit reload value that is loaded into the Watchdog Timer when a WDT instruction executes. This 24-bit value ranges across bits [23:0] to encompass the three bytes {WDTU[7:0], WDTH[7:0], WDTL[7:0]}. Writing to these registers sets the appropriate reload value; reading from these registers returns the current Watchdog Timer count value.

Caution: The 24-bit WDT reload value must not be set to a value less than 000004H.

Table 60. Watchdog Timer Reload Upper Byte Register (WDTU)

Bit	7	6	5	4	3	2	1	0
Field	WDTU							
RESET	0	0	0	0	0	0	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF1H							

Note: *A read returns the current WDT count value; a write sets the appropriate reload value.

Bit	Description
[7:0] WDTU	**WDT Reload Upper Byte** Most significant byte (MSB), Bits[23:16], of the 24-bit WDT reload value.

Table 61. Watchdog Timer Reload High Byte Register (WDTH)

Bit	7	6	5	4	3	2	1	0
Field	WDTH							
RESET	0	0	0	0	0	1	0	0
R/W	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*
Address	FF2H							

Note: *A read returns the current WDT count value; a write sets the appropriate reload value.

Bit	Description
[7:0] WDTH	**WDT Reload High Byte** Middle byte, bits[15:8] of the 24-bit WDT reload value.

Crystal Oscillator

The products in the Z8 Encore! F0830 Series contain an on-chip crystal oscillator for use with external crystals with 32kHz to 20MHz frequencies. In addition, the oscillator supports external RC networks with oscillation frequencies up to 4MHz or ceramic resonators with frequencies up to 8MHz. The on-chip crystal oscillator can be used to generate the primary system clock for the internal eZ8 CPU and the majority of its on-chip peripherals. Alternatively, the X_{IN} input pin can also accept a CMOS-level clock input signal (32kHz–20MHz). If an external clock generator is used, the X_{OUT} pin must remain unconnected. The on-chip crystal oscillator also contains a clock filter function. To see the settings for this clock filter, see Table 90 on page 133. By default, however, this clock filter is disabled; therefore, no divide to the input clock (namely, the frequency of the signal on the X_{IN} input pin) can determine the frequency of the system clock when using the default settings.

Note: Although the X_{IN} pin can be used as an input for an external clock generator, the CLKIN pin is better suited for such use. See *the* System Clock Selection *section on page 151* for more information.

Operating Modes

The Z8 Encore! F0830 Series products support the following four OSCILLATOR Modes:

- Minimum power for use with very low frequency crystals (32kHz to 1MHz)
- Medium power for use with medium frequency crystals or ceramic resonators (0.5MHz to 8MHz)
- Maximum power for use with high frequency crystals (8MHz to 20MHz)
- On-chip oscillator configured for use with external RC networks (<4MHz)

The OSCILLATOR Mode is selected using user-programmable Flash option bits. See the Flash Option Bits chapter on page 124 for more information.

Crystal Oscillator Operation

The XTLDIS Flash option bit controls whether the crystal oscillator is enabled during reset. The crystal may later be disabled after reset if a new oscillator has been selected as the system clock. If the crystal is manually enabled after reset through the OSCCTL Reg-

Table 117. AC Characteristics (Continued)

		V_{DD} = 2.7 to 3.6V T_A = 0°C to +70°C		V_{DD} = 2.7 to 3.6V T_A = –40°C to +105°C			
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**	**Conditions**
T_{XINR}	System Clock Rise Time			–	3	ns	T_{CLK} = 50 ns
T_{XINF}	System Clock Fall Time			–	3	ns	T_{CLK} = 50 ns
$T_{XTALSET}$	Crystal Oscillator Setup Time			–	30,000	cycle	Crystal oscillator cycles
T_{IPOSET}	Internal Precision Oscillator Startup Time			–	25	µs	Startup time after enable
T_{WDTSET}	WDT Startup Time			–	50	µs	Startup time after reset

On-Chip Peripheral AC and DC Electrical Characteristics

Table 118. Power-On Reset and Voltage Brown-Out Electrical Characteristics and Timing

		T_A = 0°C to +70°C			T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ[1]**	**Max**	**Units**	**Conditions**
V_{POR}	Power-On Reset Voltage Threshold				2.20	2.45	2.70	V	$V_{DD} = V_{POR}$ (default VBO trim)
V_{VBO}	Voltage Brown-Out Reset Voltage Threshold				2.15	2.40	2.65	V	$V_{DD} = V_{VBO}$ (default VBO trim)
	V_{POR} to V_{VBO} hysteresis					50	75	mV	
	Starting V_{DD} voltage to ensure valid Power-On Reset.				–	V_{SS}	–	V	
T_{ANA}	Power-On Reset Analog Delay				–	50	–	µs	$V_{DD} > V_{POR}$; T_{POR} Digital Reset delay follows T_{ANA}

Note: [1]Data in the typical column is from characterization at 3.3V and 0°C. These values are provided for design guidance only and are not tested in production.

Hex Address: F74

Table 149. ADC Sample Settling Time (ADCSST)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				SST			
RESET	0				1	1	1	1
R/W	R				R/W			
Address	F74H							

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3:0] SST	**Sample Settling Time** 0h–Fh = Number of system clock periods to meet 0.5 µs minimum.

Hex Address: F75

Table 150. ADC Sample Time (ADCST)

Bit	7	6	5	4	3	2	1	0
Field	Reserved		ST					
RESET	0		1	1	1	1	1	1
R/W	R/W		R/W					
Address	F75H							

Bit	Description
[7:6]	**Reserved** This register is reserved and must be programmed to 0.
[5:0] ST	**Sample/Hold Time** 0h–Fh = Number of system clock periods to meet 1 µs minimum.

Hex Addresses: F77–F7F

This address range is reserved.

Hex Address: FDB

Table 180. Port C Output Data Register (PCOUT)

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDBH							

Hex Address: FDC

Table 181. Port D GPIO Address Register (PDADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDCH							

Hex Address: FDD

Table 182. Port D Control Registers (PDCTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDDH							

Hex Address: FDE

This address range is reserved.

Trim Bit Control

For more information about the Trim Bit Control registers, see the Flash Option Bit Control Register Definitions section on page 126.

Hex Address: FF6

Table 189. Trim Bit Address Register (TRMADR)

Bit	7	6	5	4	3	2	1	0
Field	TRMADR - Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF6H							

Hex Address: FF7

Table 190. Trim Bit Data Register (TRMDR)

Bit	7	6	5	4	3	2	1	0
Field	TRMDR - Trim Bit Data							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF7H							

Flash Memory Controller

For more information about the Flash Control registers, see the Flash Control Register Definitions section on page 118.

Hex Address: FF8

Table 191. Flash Control Register (FCTL)

Bit	7	6	5	4	3	2	1	0
Field	FCMD							
RESET	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
Address	FF8H							

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