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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0831hj020sg

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The Voltage Brown-Out circuit can be either enabled or disabled during STOP Mode. Operations during STOP Mode is set by the VBO_AO Flash option bit. See the [Flash Option Bits](#) chapter on page 124 for information about configuring VBO_AO.

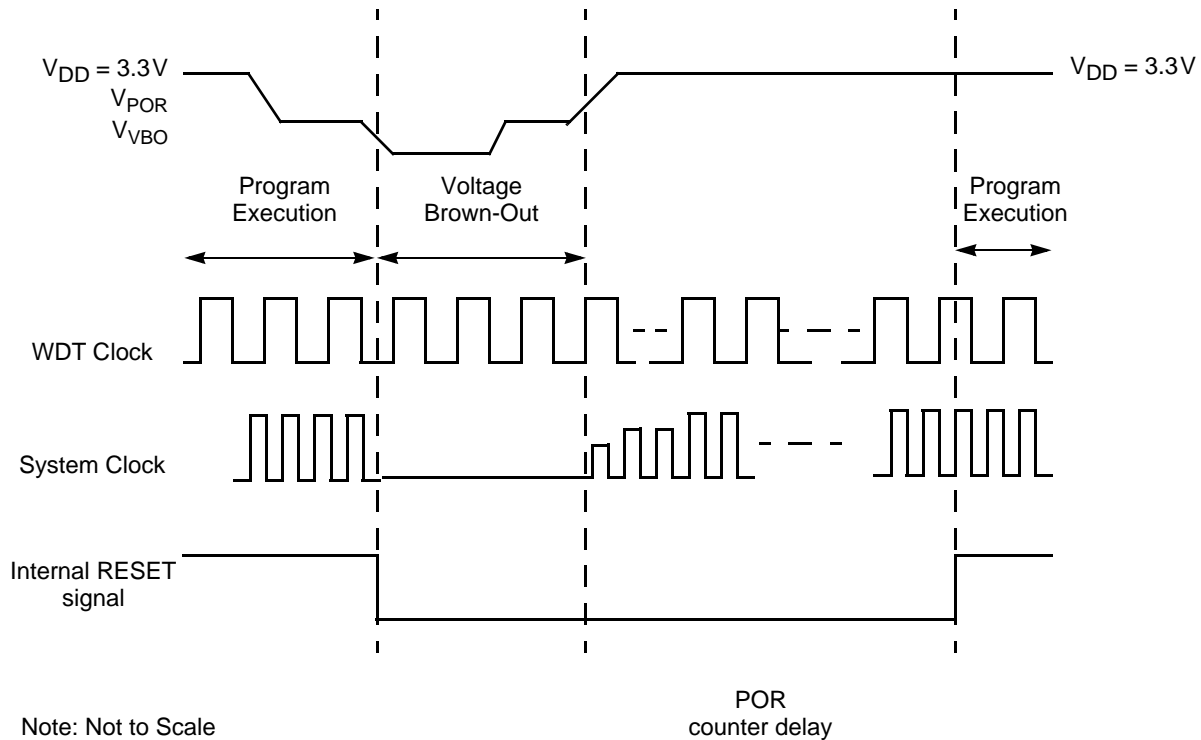


Figure 7. Voltage Brown-Out Reset Operation

Watchdog Timer Reset

If the device is operating in NORMAL or STOP Mode, the Watchdog Timer can initiate a system reset at time-out if the WDT_RES Flash option bit is programmed to 1; this state is the unprogrammed state of the WDT_RES Flash option bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt – not a system reset – at time-out. The WDT status bit in the Reset Status (RSTSTAT) Register is set to 1 to signify that the reset was initiated by the Watchdog Timer.

External Reset Input

The $\overline{\text{RESET}}$ pin has a Schmitt-triggered input and an internal pull-up resistor. After the $\overline{\text{RESET}}$ pin is asserted for a minimum of four system clock cycles, the device progresses through the system reset sequence. Because of the possible asynchronicity of the system

HALT Mode

Executing the eZ8 CPU HALT instruction places the device into HALT Mode. In HALT Mode, the operating characteristics are:

- Primary oscillator is enabled and continues to operate
- System clock is enabled and continues to operate
- eZ8 CPU is stopped
- Program counter (PC) stops incrementing
- Watchdog Timer's internal RC oscillator continues to operate
- If enabled, the Watchdog Timer continues to operate
- All other on-chip peripherals continue to operate

The eZ8 CPU can be brought out of HALT Mode by any one of the following operations:

- Interrupt
- Watchdog Timer time-out (interrupt or reset)
- Power-On Reset
- Voltage Brown-Out reset
- External $\overline{\text{RESET}}$ pin assertion

To minimize current in HALT Mode, all GPIO pins that are configured as digital inputs must be driven to V_{DD} when pull-up register bit is enabled or to one of power rail (V_{DD} or GND) when pull-up register bit is disabled.

Peripheral Level Power Control

In addition to the STOP and HALT modes, it is possible to disable each peripheral on each of the Z8 Encore! F0830 Series devices. Disabling a given peripheral minimizes its power consumption.

Power Control Register Definitions

Power Control Register 0

Each bit of the following registers disables a peripheral block, either by gating its system clock input or by removing power from the block.

Table 16. Port Alternate Function Mapping (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port B²	PB0	Reserved		AFS1[0]: 0
		ANA0	ADC analog input	AFS1[0]: 1
	PB1	Reserved		AFS1[1]: 0
		ANA1	ADC analog input	AFS1[1]: 1
	PB2	Reserved		AFS1[2]: 0
		ANA2	ADC analog input	AFS1[2]: 1
	PB3	CLKIN	External input clock	AFS1[3]: 0
		ANA3	ADC analog input	AFS1[3]: 1
	PB4	Reserved		AFS1[4]: 0
		ANA7	ADC analog input	AFS1[4]: 1
	PB5	Reserved		AFS1[5]: 0
		V _{REF}	ADC reference voltage	AFS1[5]: 1
	PB6	Reserved		AFS1[6]: 0
		Reserved		AFS1[6]: 1
	PB7	Reserved		AFS1[7]: 0
		Reserved		AFS1[7]: 1

Notes:

1. Because there is only a single alternate function for each Port A and Port D (PD0) pin, the Alternate Function Set registers are not implemented for Port A and Port D (PD0). Enabling alternate function selections (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) automatically enables the associated alternate function.
2. Because there are at most two choices of alternate functions for any Port B pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) must also be enabled.
3. Because there are at most two choices of alternate functions for any Port C pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) must also be enabled.

Port A–D High Drive Enable Subregisters

The Port A–D High Drive Enable Subregister, shown in Table 24, is accessed through the Port A–D Control Register by writing 04H to the Port A–D Address Register. Setting the bits in the Port A–D High Drive Enable subregisters to 1 configures the specified port pins for high-output current drive operation. The Port A–D High Drive Enable Subregister affects the pins directly and, as a result, alternate functions are also affected.

Table 24. Port A–D High Drive Enable Subregisters (PxHDE)

Bit	7	6	5	4	3	2	1	0
Field	PHDE7	PHDE6	PHDE5	PHDE4	PHDE3	PHDE2	PHDE1	PHDE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 04H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0]	Port High Drive Enable
PHDEx	0 = The port pin is configured for standard output current drive. 1 = The port pin is configured for high output current drive.
Note: x indicates the specific GPIO port pin number (7–0).	

Port A–D Stop Mode Recovery Source Enable Subregisters

The Port A–D Stop Mode Recovery Source Enable Subregister, shown in Table 25, is accessed through the Port A–D Control Register by writing 05H to the Port A–D Address Register. Setting the bits in the Port A–D Stop Mode Recovery Source Enable subregisters to 1 configures the specified port pins as a Stop Mode Recovery source. During STOP Mode, any logic transition on a port pin enabled as a Stop Mode Recovery source initiates a Stop Mode Recovery event.

Table 25. Port A–D Stop Mode Recovery Source Enable Subregisters (PxSMRE)

Bit	7	6	5	4	3	2	1	0
Field	PSMRE7	PSMRE6	PSMRE5	PSMRE4	PSMRE3	PSMRE2	PSMRE1	PSMRE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 05H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0]	Port Stop Mode Recovery Source Enable
PSMREx	0 = The port pin is not configured as a Stop Mode Recovery source. Transitions on this pin during STOP Mode do not initiate Stop Mode Recovery. 1 = The port pin is configured as a Stop Mode Recovery source. Any logic transition on this pin during STOP Mode initiates Stop Mode Recovery.

Note: x indicates the specific GPIO port pin number (7–0).

Interrupt Request 2 Register

The Interrupt Request 2 (IRQ2) Register, shown in Table 37, stores interrupt requests for both vectored and polled interrupts. When a request is sent to the Interrupt Controller, the corresponding bit in the IRQ2 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the Interrupt Controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 2 Register to determine if any interrupt requests are pending.

Table 37. Interrupt Request 2 Register (IRQ2)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				PC3I	PC2I	PC1I	PC0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC6H							

Bit	Description
[7:4]	Reserved These registers are reserved and must be programmed to 0000.
[3]	Port C Pin x Interrupt Request
PCxI	0 = No interrupt request is pending for GPIO Port C pin x. 1 = An interrupt request from GPIO Port C pin x is awaiting service.

Note: x indicates the specific GPIO port pin number (3–0).

IRQ0 Enable High and Low Bit Registers

Table 38 lists the priority control values for IRQ0. The IRQ0 Enable High and Low Bit registers, shown in Tables 39 and 40, form a priority-encoded enabling service for interrupts in the Interrupt Request 0 Register. Priority is generated by setting the bits in each register.

Table 38. IRQ0 Enable and Priority Encoding

IRQ0ENH[x]	IRQ0ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

Note: x indicates the register bits in the range 7–0.

Table 39. IRQ0 Enable High Bit Register (IRQ0ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1ENH	T0ENH	Reserved				ADCENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC1H							

Bit	Description
[7]	Reserved This bit is reserved and must be programmed to 0.
[6] T1ENH	Timer 1 Interrupt Request Enable High Bit
[5] T0ENH	Timer 0 Interrupt Request Enable High Bit
[4:1]	Reserved These registers are reserved and must be programmed to 0000.
[0] ADCENH	ADC Interrupt Request Enable High Bit

Table 40. IRQ0 Enable Low Bit Register (IRQ0ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1ENL	T0ENL	Reserved				ADCENL
RESET	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R	R	R/W
Address	FC2H							

Bit	Description
[7]	Reserved This bit is reserved and must be programmed to 0.
[6] T1ENL	Timer 1 Interrupt Request Enable Low Bit
[5] T0ENL	Timer 0 Interrupt Request Enable Low Bit
[4:1]	Reserved These registers are reserved and must be programmed to 0000.
[0] ADCENL	ADC Interrupt Request Enable Low Bit

Timer 0–1 PWM High and Low Byte Registers

The Timer 0–1 PWM High and Low Byte (TxPWMH and TxPWML) registers, shown in Tables 54 and 55, control PWM operations. These registers also store the capture values for the CAPTURE and CAPTURE/COMPARE modes.

Table 54. Timer 0–1 PWM High Byte Register (TxPWMH)

Bit	7	6	5	4	3	2	1	0
Field	PWMH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F04H, F0CH							

Table 55. Timer 0–1 PWM Low Byte Register (TxPWML)

Bit	7	6	5	4	3	2	1	0
Field	PWML							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F05H, F0DH							

Bit	Description
[7:0]	Pulse Width Modulator High and Low Bytes
PWMH, PWML	These two bytes, {PWMH[7:0], PWML[7:0]}, form a 16-bit value that is compared to the current 16-bit timer count. When a match occurs, the PWM output changes state. The PWM output value is set by the TPOL bit in the Timer Control Register (TxCTL1). The TxPWMH and TxPWML registers also store the 16-bit captured timer value when operating in capture or CAPTURE/COMPARE modes.

ADC Timing

Each ADC measurement consists of three phases:

1. Input sampling (programmable, minimum of 1.0 μ s)
2. Sample-and-hold amplifier settling (programmable, minimum of 0.5 μ s)
3. Conversion is 13 ADCLK cycles

Figures 12 and 13 display the timing of an ADC conversion.

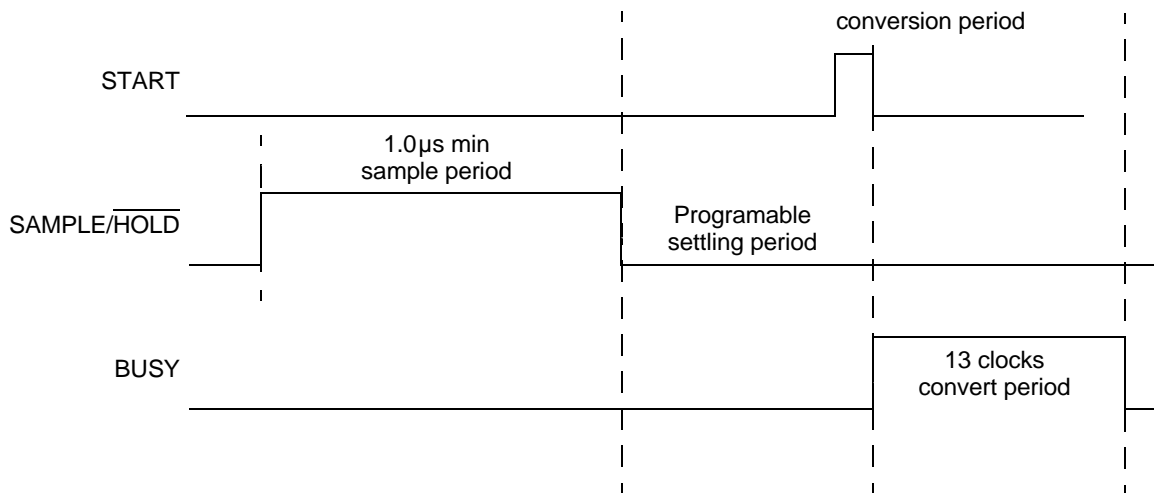


Figure 12. ADC Timing Diagram

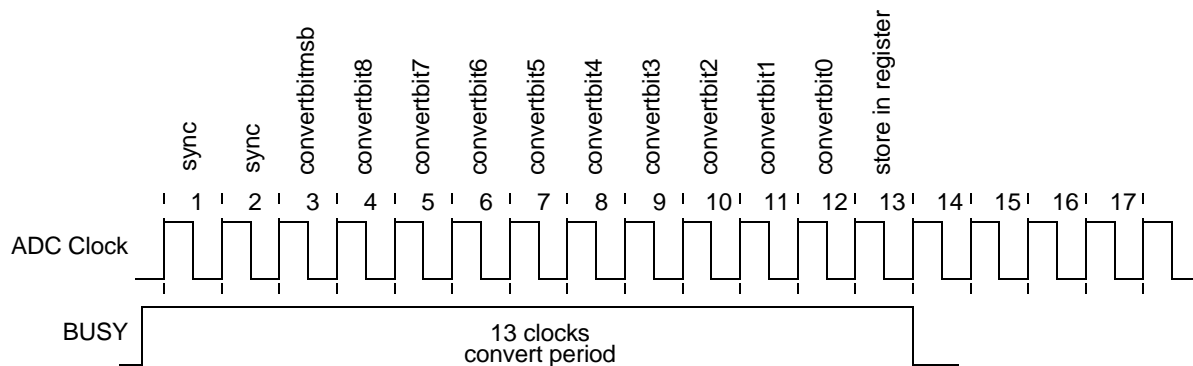


Figure 13. ADC Convert Timing

Flash Option Bit Control Register Definitions

This section briefly describes the features of the Trim Bit Address and Data registers.

Trim Bit Address Register

The Trim Bit Address Register, shown in Table 78, contains the target address to access the trim option bits. Trim bit addresses in the range 00h–1Fh map to the information area at addresses 20h–3Fh, as shown in Table 79.

Table 78. Trim Bit Address Register (TRMADR)

Bit	7	6	5	4	3	2	1	0
Field	TRMADR: Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF6H							

Table 79. Trim Bit Address Map

Trim Bit Address	Information Area Address
00h	20h
01h	21h
02h	22h
03h	23h
:	:
1Fh	3Fh

Trim Bit Data Register

The Trim Bit Data Register, shown in Table 80, contains the read or write data to access the trim option bits.

Oscillator Control

The Z8 Encore! F0830 Series device uses five possible clocking schemes. Each one of these is user-selectable.

- On-chip precision trimmed RC oscillator
- On-chip oscillator using off-chip crystal or resonator
- On-chip oscillator using external RC network
- External clock drive
- On-chip low precision Watchdog Timer Oscillator

In addition, Z8 Encore! F0830 Series devices contain clock failure detection and recovery circuitry, allowing continued operation despite a failure of the primary oscillator.

Operation

This chapter discusses the logic used to select the system clock and handle primary oscillator failures. A description of the specific operation of each oscillator is outlined further in this document.

System Clock Selection

The oscillator control block selects from the available clocks. *Table 98* describes each clock source and its usage.

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
CLR dst	dst ← 00H	R		B0	–	–	–	–	–	–	2	2
		IR		B1							2	3
COM dst	dst ← ~dst	R		60	–	*	*	0	–	–	2	2
		IR		61							2	3
CP dst, src	dst - src	r	r	A2	*	*	*	*	–	–	2	3
		r	lr	A3							2	4
		R	R	A4							3	3
		R	IR	A5							3	4
		R	IM	A6							3	3
		IR	IM	A7							3	4
CPC dst, src	dst - src - C	r	r	1F A2	*	*	*	*	–	–	3	3
		r	lr	1F A3							3	4
		R	R	1F A4							4	3
		R	IR	1F A5							4	4
		R	IM	1F A6							4	3
		IR	IM	1F A7							4	4
CPCX dst, src	dst - src - C	ER	ER	1F A8	*	*	*	*	–	–	5	3
		ER	IM	1F A9							5	3
CPX dst, src	dst - src	ER	ER	A8	*	*	*	*	–	–	4	3
		ER	IM	A9							4	3
DA dst	dst ← DA(dst)	R		40	*	*	*	X	–	–	2	2
		IR		41							2	3
DEC dst	dst ← dst - 1	R		30	–	*	*	*	–	–	2	2
		IR		31							2	3
DECW dst	dst ← dst - 1	RR		80	–	*	*	*	–	–	2	5
		IRR		81							2	6
DI	IRQCTL[7] ← 0			8F	–	–	–	–	–	–	1	2

Note: Flags Notation:

* = Value is a function of the result of the operation.

– = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

Table 128. Z8 Encore! XP F0830 Series Ordering Matrix

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8F0430QH020EG	4KB	256	Yes	7	QFN 20-pin
Z8F0431SH020EG	4KB	256	Yes	0	SOIC 20-pin
Z8F0431HH020EG	4KB	256	Yes	0	SSOP 20-pin
Z8F0431PH020EG	4KB	256	Yes	0	PDIP 20-pin
Z8F0431QH020EG	4KB	256	Yes	0	QFN 20-pin
Z8F0430SJ020EG	4KB	256	Yes	8	SOIC 28-pin
Z8F0430HJ020EG	4KB	256	Yes	8	SSOP 28-pin
Z8F0430PJ020EG	4KB	256	Yes	8	PDIP 28-pin
Z8F0430QJ020EG	4KB	256	Yes	8	QFN 28-pin
Z8F0431SJ020EG	4KB	256	Yes	0	SOIC 28-pin
Z8F0431HJ020EG	4KB	256	Yes	0	SSOP 28-pin
Z8F0431PJ020EG	4KB	256	Yes	0	PDIP 28-pin
Z8F0431QJ020EG	4KB	256	Yes	0	QFN 28-pin
Z8 Encore! F0830 with 2KB Flash					
Standard Temperature: 0°C to 70°C					
Z8F0230SH020SG	2KB	256	Yes	7	SOIC 20-pin
Z8F0230HH020SG	2KB	256	Yes	7	SSOP 20-pin
Z8F0230PH020SG	2KB	256	Yes	7	PDIP 20-pin
Z8F0230QH020SG	2KB	256	Yes	7	QFN 20-pin
Z8F0231SH020SG	2KB	256	Yes	0	SOIC 20-pin
Z8F0231HH020SG	2KB	256	Yes	0	SSOP 20-pin
Z8F0231PH020SG	2KB	256	Yes	0	PDIP 20-pin
Z8F0231QH020SG	2KB	256	Yes	0	QFN 20-pin
Z8F0230SJ020SG	2KB	256	Yes	8	SOIC 28-pin
Z8F0230HJ020SG	2KB	256	Yes	8	SSOP 28-pin
Z8F0230PJ020SG	2KB	256	Yes	8	PDIP 28-pin
Z8F0230QJ020SG	2KB	256	Yes	8	QFN 28-pin
Z8F0231SJ020SG	2KB	256	Yes	0	SOIC 28-pin
Z8F0231HJ020SG	2KB	256	Yes	0	SSOP 28-pin
Z8F0231PJ020SG	2KB	256	Yes	0	PDIP 28-pin
Z8F0231QJ020SG	2KB	256	Yes	0	QFN 28-pin

Table 129 lists the pin count by package.

Table 129. Package and Pin Count Description

Package	Pin Count	
	20	28
PDIP	√	√
QFN	√	√
SOIC	√	√
SSOP	√	√

Appendix A. Register Tables

For the reader's convenience, this appendix lists all F0830 Series registers numerically by hexadecimal address.

General Purpose RAM

In the F0830 Series, the 000–EFF hexadecimal address range is partitioned for general-purpose random access memory, as follows.

Hex Addresses: 000–0FF

This address range is reserved for general-purpose register file RAM. For more details, see the [Register File](#) section on page 14.

Hex Addresses: 100–EFF

This address range is reserved.

Timer 0

For more information about these Timer Control registers, see the [Timer Control Register Definitions](#) section on page 83.

Hex Address: F00

Table 130. Timer 0 High Byte Register (T0H)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H							

Hex Address: FC1

Table 158. IRQ0 Enable High Bit Register (IRQ0ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1ENH	T0ENH	Reserved	Reserved	Reserved	Reserved	ADCENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC1H							

Hex Address: FC2

Table 159. IRQ0 Enable Low Bit Register (IRQ0ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved	T1ENL	T0ENL	Reserved	Reserved	Reserved	Reserved	ADCENL
RESET	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R	R	R/W
Address	FC2H							

Hex Address: FC3

Table 160. Interrupt Request 1 Register (IRQ1)

Bit	7	6	5	4	3	2	1	0
Field	PA7I	PA6CI	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC3H							

Hex Address: FC4

Table 161. IRQ1 Enable High Bit Register (IRQ1ENH)

Bit	7	6	5	4	3	2	1	0
Field	PA7ENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC4H							

Hex Address: FDB

Table 180. Port C Output Data Register (PCOUT)

Bit	7	6	5	4	3	2	1	0
Field	POUT7	POUT6	POUT5	POUT4	POUT3	POUT2	POUT1	POUT0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDBH							

Hex Address: FDC

Table 181. Port D GPIO Address Register (PDADDR)

Bit	7	6	5	4	3	2	1	0
Field	PADDR[7:0]							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDCH							

Hex Address: FDD

Table 182. Port D Control Registers (PDCTL)

Bit	7	6	5	4	3	2	1	0
Field	PCTL							
RESET	00H							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FDDH							

Hex Address: FDE

This address range is reserved.

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