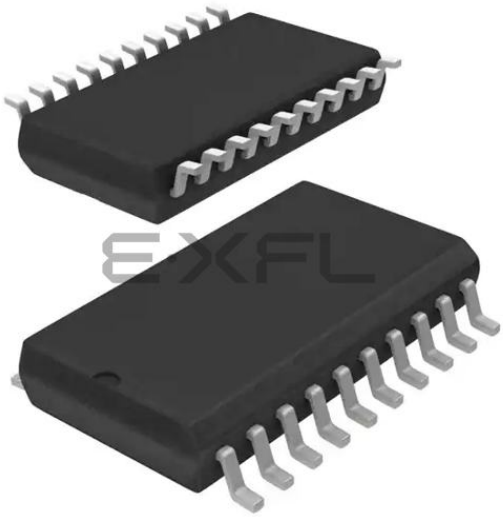

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0831sh020sg

Data Memory

The Z8 Encore! F0830 Series does not use the eZ8 CPU's 64KB data memory address space.

Flash Information Area

Table 7 maps the Z8 Encore! F0830 Series Flash information area. The 128-byte information area is accessed, by setting bit 7 of the Flash Page Select Register to 1. When access is enabled, the Flash information area is mapped into program memory and overlays these 128 bytes at addresses FE00H to FE7FH. When information area access is enabled, all reads from these program memory addresses return information area data rather than program memory data. Access to the Flash information area is read-only.

Table 7. Z8 Encore! F0830 Series Flash Memory Information Area Map

Program Memory Address (Hex)	Function
FE00–FE3F	Zilog option bits
FE40–FE53	Part Number 20-character ASCII alphanumeric code Left-justified and filled with FH
FE54–FE5F	Reserved
FE60–FE7F	Reserved
FE80–FFFF	Reserved

Port A–D Output Control Subregisters

The Port A–D Output Control Subregister, shown in Table 23, is accessed through the Port A–D Control Register by writing 03H to the Port A–D Address Register. Setting the bits in the Port A–D Output Control subregisters to 1 configures the specified port pins for open-drain operation. These subregisters affect the pins directly and, as a result, alternate functions are also affected.

Table 23. Port A–D Output Control Subregisters (PxOC)

Bit	7	6	5	4	3	2	1	0
Field	POC7	POC6	POC5	POC4	POC3	POC2	POC1	POC0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 03H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0] POCx	**Port Output Control** These bits function independently of the Alternate function bit and always disable the drains, if set to 1. 0 = The drains are enabled for any OUTPUT Mode (unless overridden by the Alternate function). 1 = The drain of the associated pin is disabled (OPEN-DRAIN mode).

Note: x indicates the specific GPIO port pin number (7–0).

reload. For the timer output to make a state change at a ONE-SHOT time-out (rather than a single cycle pulse), first set the TPOL bit in the Timer Control Register to the start value before enabling ONE-SHOT Mode. After starting the timer, set TPOL to the opposite bit value.

Observe the following steps for configuring a timer for ONE-SHOT Mode and for initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for ONE-SHOT Mode
   - Set the prescale value
   - Set the initial output level (High or Low) if using the timer output Alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
5. If using the timer output function, configure the associated GPIO port pin for the timer output alternate function.
6. Write to the Timer Control Register to enable the timer and initiate counting.

In ONE-SHOT Mode, the system clock always provides the timer input. The timer period is calculated with the following equation:

$$\text{One-Shot Mode Time-Out Period (s)} = \frac{(\text{Reload Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

CONTINUOUS Mode

In CONTINUOUS Mode, the timer counts up to the 16-bit reload value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and the counting resumes. Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps for configuring a timer for CONTINUOUS Mode and for initiating the count:

1. Write to the Timer Control Register to:

- Disable the timer
- Configure the timer for CONTINUOUS Mode
- Set the prescale value
- If using the timer output Alternate function, set the initial output level (High or Low)

2. Write to the Timer High and Low Byte registers to set the starting count value (usually 0001H). This action only affects the first pass in CONTINUOUS Mode. After the first timer reload in CONTINUOUS Mode, counting always begins at the reset value of 0001H.
3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Enable the timer interrupt (if appropriate) and set the timer interrupt priority by writing to the relevant interrupt registers.
5. Configure the associated GPIO port pin (if using the timer output function) for the timer output alternate function.
6. Write to the Timer Control Register to enable the timer and initiate counting.

In CONTINUOUS Mode, the system clock always provides the timer input. The timer period is calculated with the following equation:

$$\text{Continuous Mode Time-Out Period (s)} = \frac{\text{Reload Value} \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first time-out period.

COUNTER Mode

In COUNTER Mode, the timer counts input transitions from a GPIO port pin. The timer input is taken from the GPIO port pin: timer input alternate function. The TPOL bit in the Timer Control Register determines whether the count occurs on the rising edge or the falling edge of the timer input signal. In COUNTER Mode, the prescaler is disabled.

Caution: The input frequency of the timer input signal must not exceed one-fourth the system clock frequency.

Upon reaching the reload value stored in the Timer Reload High and Low Byte registers, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. Additionally, if the timer output alternate function

5. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and Reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting the TICONFIG field of the TxCTL1 Register.
6. Configure the associated GPIO port pin for the timer input alternate function.
7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time between the timer start and the capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

CAPTURE RESTART Mode

In CAPTURE RESTART Mode, the current timer count value is recorded when the acceptable external timer input transition occurs. The capture count value is written to the timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines whether the capture occurs on a rising edge or a falling edge of the timer input signal. When the capture event occurs, an interrupt is generated and the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in the TxCTL1 Register is set to indicate that the timer interrupt has been caused by an input capture event.

If no capture event occurs, the timer counts up to 16-bit compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in the TxCTL1 Register is cleared to indicate that the timer interrupt has not been caused by an input capture event.

Observe the following steps for configuring a timer for CAPTURE RESTART Mode and for initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for CAPTURE RESTART Mode; setting the mode also involves writing to TMODEHI bit in the TxCTL1 Register
   - Set the prescale value
   - Set the capture edge (rising or falling) for the timer input
2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).

3. Write to the Timer Reload High and Low Byte registers to set the reload value.
4. Clear the timer PWM High and Low Byte registers to 0000H. This allows user software to determine if interrupts are generated by either a capture event or a reload. If the PWM High and Low Byte registers still contain 0000H after the interrupt, the interrupt were generated by a reload.
5. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and Reload events. The user can configure the timer interrupt to be generated only at the input capture event or the reload event by setting the TICONFIG field of the TxCTL1 Register.
6. Configure the associated GPIO port pin for the timer input alternate function.
7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time between the timer start and the capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

COMPARE Mode

In COMPARE Mode, the timer counts up to 16-bit maximum compare value stored in the Timer Reload High and Low Byte registers. The timer input is the system clock. Upon reaching the compare value, the timer generates an interrupt and counting continues (the timer value is not reset to 0001H). Additionally, if the timer output alternate function is enabled, the timer output pin changes state (from Low to High or from High to Low) upon compare.

If the timer reaches FFFFH, the timer resets to 0000H and continues counting.

Observe the following steps for configuring a timer for COMPARE Mode and for initiating the count:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for COMPARE Mode
   - Set the prescale value
   - Set the initial logic level (High or Low) for the timer output alternate function
2. Write to the Timer High and Low Byte registers to set the starting count value.
3. Write to the Timer Reload High and Low Byte registers to set the compare value.

ADC Control Register 0

The ADC Control 0 Register, shown in Table 63, initiates an A/D conversion and provides ADC status information.

Table 63. ADC Control Register 0 (ADCCTL0)

Bit	7	6	5	4	3	2	1	0
Field	START	Reserved	REFEN	ADCEN	Reserved	ANAIN[2:0]		
RESET	0	0	0	0	0	0	0	0
R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F70h							

Bit	Description
[7] START	**ADC Start/Busy** 0 = Writing to 0 has no effect; reading a 0 indicates that the ADC is available to begin a conversion. 1 = Writing to 1 starts a conversion; reading a 1 indicates that a conversion is currently in progress.
[6]	**Reserved** This bit is reserved and must be programmed to 0.
[5] REFEN	**Reference Enable** 0 = Internal reference voltage is disabled allowing an external reference voltage to be used by the ADC. 1 = Internal reference voltage for the ADC is enabled. The internal reference voltage can be measured on the V_{REF} pin.
[4] ADCEN	**ADC Enable** 0 = ADC is disabled for low power operation. 1 = ADC is enabled for normal use.
[3]	**Reserved** This bit is reserved and must be programmed to 0.
[2:0] ANAIN	**Analog Input Select** 000 = ANA0 input is selected for analog to digital conversion. 001 = ANA1 input is selected for analog to digital conversion. 010 = ANA2 input is selected for analog to digital conversion. 011 = ANA3 input is selected for analog to digital conversion. 100 = ANA4 input is selected for analog to digital conversion. 101 = ANA5 input is selected for analog to digital conversion. 110 = ANA6 input is selected for analog to digital conversion. 111 = ANA7 input is selected for analog to digital conversion.

ADC Data High Byte Register

The ADC Data High Byte Register, listed in Table 64, contains the upper eight bits of the ADC output. Access to the ADC Data High Byte Register is read-only. Reading the ADC Data High Byte Register latches data in the ADC Low Bits Register.

Table 64. ADC Data High Byte Register (ADCD_H)

Bit	7	6	5	4	3	2	1	0
Field	ADCDH							
RESET	X							
R/W	R							
Address	F72H							

Bit	Description
[7:0] ADCDH	**ADC High Byte** 00h–FFh = The last conversion output is held in the data registers until the next ADC conversion is completed.

ADC Data Low Bits Register

The ADC Data Low Bits Register, shown in Table 65, contains the lower bits of the ADC output. Access to the ADC Data Low Bits Register is read-only. Reading the ADC Data High Byte Register latches lower bits of the ADC in the ADC Data Low Bits Register.

Table 65. ADC Data Low Bits Register (ADCD_L)

Bit	7	6	5	4	3	2	1	0
Field	ADCDL		Reserved					
RESET	X		X					
R/W	R		R					
Address	F73H							

Bit	Description
[7:6] ADCDL	**ADC Low Bits** 00–11b = These bits are the two least-significant bits of the 10-bit ADC output. These bits are undefined after a reset. The low bits are latched into this register whenever the ADC Data High Byte Register is read.
[5:0]	**Reserved** These bits are reserved and must be programmed to 000000.

Flash Option Bits

Programmable Flash option bits allow user configuration of certain aspects of Z8 Encore! F0830 Series operation. The feature configuration data is stored in the Flash program memory and read during reset. The features available for control through the Flash option bits are:

- Watchdog Timer time-out response selection–interrupt or system reset
- Watchdog Timer enabled at reset
- The ability to prevent unwanted read access to user code in program memory
- The ability to prevent accidental programming and erasure of all or a portion of the user code in program memory
- Voltage Brown-Out configuration always enabled or disabled during STOP Mode to reduce STOP Mode power consumption
- OSCILLATOR Mode selection for high, medium and low power crystal oscillators or external RC oscillator
- Factory trimming information for the Internal Precision Oscillator and VBO voltage

Operation

This section describes the type and configuration of the programmable Flash option bits.

Option Bit Configuration by Reset

Each time the Flash option bits are programmed or erased, the device must be reset for the change to be effective. During any Reset operation (system reset or Stop Mode Recovery), the Flash option bits are automatically read from Flash program memory and written to the Option Configuration registers, which control Z8 Encore! F0830 Series device operation. Option bit control is established before the device exits reset and the eZ8 CPU begins code execution. The Option Configuration registers are not part of the register file and are not accessible for read or write access.

Option Bit Types

This section describes the two types of Flash option bits offered in the F0830 Series.

User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits is provided because these locations contain application specific device configurations. The information contained here is lost when page 0 of program memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered by the user. Program memory can be erased without endangering these values. It is possible to alter working values of these bits by accessing the trim bit address and data registers, but these working values are lost after a power loss.

There are 32 bytes of trim data. To modify one of these values, the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data Register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data Register returns the working value of the target trim data byte.

Note: The trim address range is from information address 20–3F only. The remaining information page is not accessible via the Trim Bit Address and Data registers.

During reset, the first 43 system clock cycles perform 43 Flash accesses. The six bits of the counter provide the lower six bits of the Flash memory address. All other address bits are set to 0. The option bit registers use the 6-bit address from the counter as an address and latch the data from the Flash on the positive edge of the IPO clock, allowing for a maximum of 344-bits (43 bytes) of option information to be read from Flash.

Because option information is stored in both the first two bytes of program memory and in the information area of Flash memory, the data must be placed in specific locations to be read correctly. In this case, the first two bytes at addresses 0 and 1 in program memory are read out and the remainder of the bytes are read out of the Flash information area.

- Watchdog Timer reset
- Asserting the $\overline{\text{RESET}}$ pin Low to initiate a reset
- Driving the DBG pin Low while the device is in STOP Mode initiates a system reset

OCD Data Format

The OCD interface uses the asynchronous data format defined for RS-232. Each character is transmitted as 1 start bit, 8 data bits (least-significant bit first) and 1 stop bit. See Figure 23.

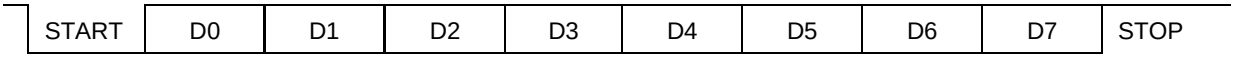

Figure 23. OCD Data Format

OCD Autobaud Detector/Generator

To run over a range of baud rates (data bits per second) with various system clock frequencies, the On-Chip Debugger contains an autobaud detector/generator. After a reset, the OCD is idle until it receives data. The OCD requires that the first character sent from the host is the character 80H. The character 80H has eight continuous bits low (one Start bit plus 7 data bits), framed between high bits. The autobaud detector measures this period and sets the OCD baud rate generator accordingly.

The autobaud detector/generator is clocked by the system clock. The minimum baud rate is the system clock frequency divided by 512. For optimal operation with asynchronous datastreams, the maximum recommended baud rate is the system clock frequency divided by 8. The maximum possible baud rate for asynchronous datastreams is the system clock frequency divided by 4, but this theoretical maximum is possible only for low noise designs with clean signals. Table 94 lists minimum and recommended maximum baud rates for sample crystal frequencies.

Table 94. OCD Baud-Rate Limits

System Clock Frequency (MHz)	Recommended Maximum Baud Rate (kbps)	Recommended Standard PC Baud Rate (bps)	Minimum Baud Rate (kbps)
20.0	2500.0	1,843,200	39
1.0	125.0	115,200	1.95
0.032768 (32 KHz)	4.096	2400	0.064

```
DBG ← 0AH
DBG ← Program Memory Address[15:8]
DBG ← Program Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG ← 1–65536 data bytes
```

Read Program Memory (0BH). The read program memory command, reads data from program memory. This command is equivalent to the LDC and LDCI instructions. Data can be read 1–65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG Mode or if the Flash read protect option bit is enabled, this command returns FFH for the data.

```
DBG ← 0BH
DBG ← Program Memory Address[15:8]
DBG ← Program Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG → 1–65536 data bytes
```

Write Data Memory (0CH). The write data memory command, writes data to data memory. This command is equivalent to the LDE and LDEI instructions. Data can be written 1–65536 bytes at a time (65536 bytes can be written by setting size to 0). If the device is not in DEBUG Mode or if the flash read protect option bit is enabled, the data is discarded.

```
DBG ← 0CH
DBG ← Data Memory Address[15:8]
DBG ← Data Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG ← 1–65536 data bytes
```

Read Data Memory (0DH). The read data memory command, reads from data memory. This command is equivalent to the LDE and LDEI instructions. Data can be read from 1 to 65536 bytes at a time (65536 bytes can be read by setting size to 0). If the device is not in DEBUG Mode, this command returns FFH for the data.

```
DBG ← 0DH
DBG ← Data Memory Address[15:8]
DBG ← Data Memory Address[7:0]
DBG ← Size[15:8]
DBG ← Size[7:0]
DBG → 1–65536 data bytes
```

Read Program Memory CRC (0EH). The read program memory CRC command, computes and returns the cyclic redundancy check (CRC) of program memory using the 16-bit CRC-CCITT polynomial. If the device is not in DEBUG Mode, this command returns FFFFH for the CRC value. Unlike the other OCD read commands, there is a delay from issuing of the command until the OCD returns the data. The OCD reads program memory, calculates the CRC value and returns the result. The delay is a function of program mem-

Bit	Description (Continued)
[4] POFEN	**Primary Oscillator Failure Detection Enable** 1 = Failure detection and recovery of primary oscillator is enabled. 0 = Failure detection and recovery of primary oscillator is disabled.
[3] WDFEN	**Watchdog Timer Oscillator Failure Detection Enable** 1 = Failure detection of Watchdog Timer Oscillator is enabled. 0 = Failure detection of Watchdog Timer Oscillator is disabled.
[2:0] SCKSEL	**System Clock Oscillator Select** 000 = Internal Precision Oscillator functions as system clock at 5.53 MHz. 001 = Internal Precision Oscillator functions as system clock at 32 kHz. 010 = Crystal oscillator or external RC oscillator functions as system clock. 011 = Watchdog Timer Oscillator functions as system clock. 100 = External clock signal on PB3 functions as system clock. 101 = Reserved. 110 = Reserved. 111 = Reserved.

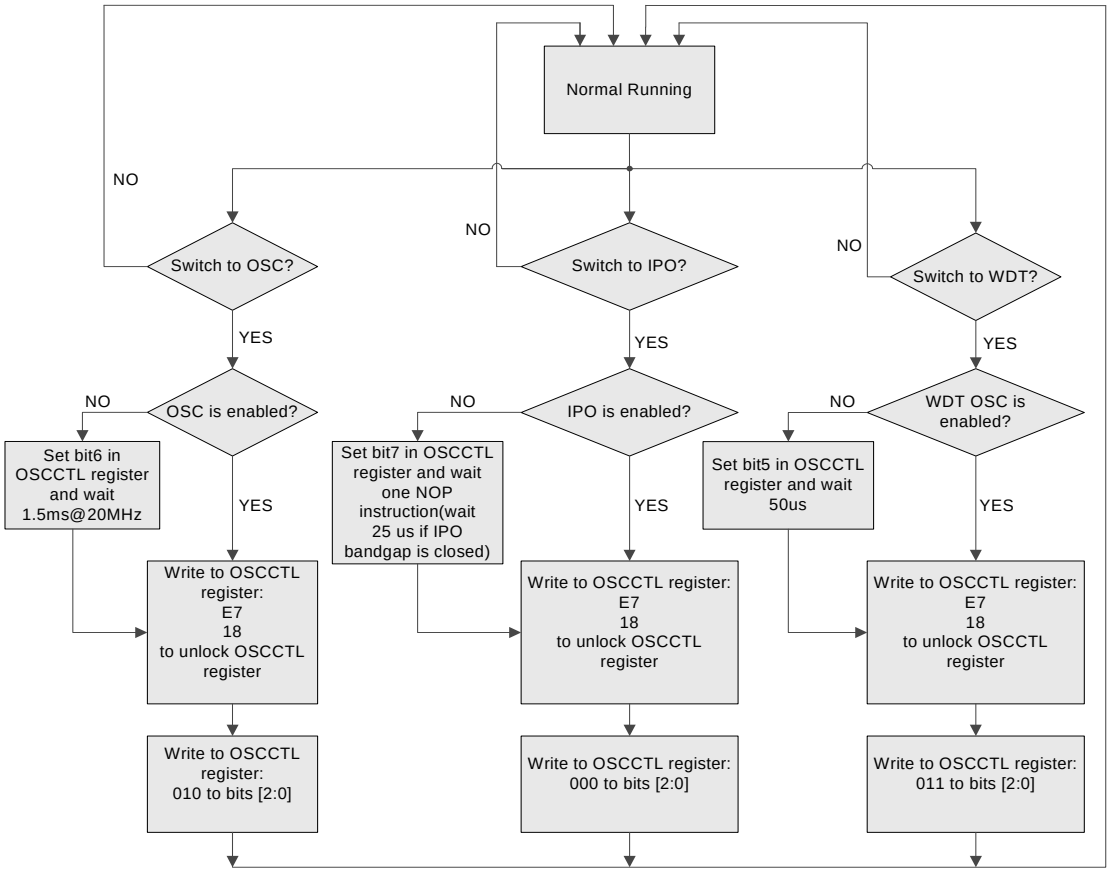

Figure 24. Oscillator Control Clock Switching Flow Chart

Internal Precision Oscillator

The Internal Precision Oscillator (IPO) is designed for use without external components. The user can either manually trim the oscillator for a nonstandard frequency or use the automatic factory-trimmed version to achieve a 5.53MHz frequency with ±4% accuracy and 45%~55% duty cycle over the operating temperature and supply voltage of the device. The maximum start-up time of the IPO is 25µs. IPO features include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53MHz or 32.8kHz (contains both a FAST and a SLOW mode)
- Trimming possible through Flash option bits, with user override
- Elimination of crystals or ceramic resonators in applications where high timing accuracy is not required

Operation

The internal oscillator is an RC relaxation oscillator with a minimized sensitivity to power supply variations. By using ratio-tracking thresholds, the effect of power supply voltage is cancelled out. The dominant source of oscillator error is the absolute variance of chip-level fabricated components, such as capacitors. An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed, the oscillator frequency is stable and does not require subsequent calibration. Trimming was performed during manufacturing and is not necessary for the user to repeat unless a frequency other than 5.53MHz (FAST mode) or 32.8kHz (SLOW mode) is required.

Note: The user can power down the IPO block for minimum system power.

By default, the oscillator is configured through the Flash option bits. However, the user code can override these trim values, as described in *the* Trim Bit Address Space *section on page 129*.

Select one of two frequencies for the oscillator: 5.53MHz or 32.8 kHz, using the OSCSEL bits described in the Oscillator Control chapter on page 151.

eZ8 CPU Instruction Summary

Table 113 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect upon the Flags register, the number of CPU clock cycles required for the instruction fetch and the number of CPU clock cycles required for the instruction execution.

Table 113. eZ8 CPU Instruction Summary

Assembly Mnemonic	Symbolic Operation	Address Mode dst	Address Mode src	Op Code(s) (Hex)	Flags C	Z	S	V	D	H	Fetch Cycles	Instr. Cycles
ADC dst, src	dst ← dst + src + C	r	r	12	*	*	*	*	0	*	2	3
		r	Ir	13							2	4
		R	R	14							3	3
		R	IR	15							3	4
		R	IM	16							3	3
		IR	IM	17							3	4
ADCX dst, src	dst ← dst + src + C	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19							4	3
ADD dst, src	dst ← dst + src	r	r	02	*	*	*	*	0	*	2	3
		r	Ir	03							2	4
		R	R	04							3	3
		R	IR	05							3	4
		R	IM	06							3	3
		IR	IM	07							3	4
ADDX dst, src	dst ← dst + src	ER	ER	08	*	*	*	*	0	*	4	3
		ER	IM	09							4	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Table 122. Analog-to-Digital Converter Electrical Characteristics and Timing (Continued)

		V_{DD} = 2.7 to 3.6V T_A = 0°C to +70°C			V_{DD} = 2.7 to 3.6V T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Z_{IN}	Input Impedance				10			MΩ	
V_{IN}	Input Voltage Range				0		2.0	V	Internal reference
					0		0.9*VDD		External reference
	Conversion Time				11.9			µs	20MHz (ADC Clock)
	Input Bandwidth					500		KHz	
	Wake Up Time					0.02		ms	Internal reference
						10			External reference
	Input Clock Duty				45	50	55		
	Maximum Input Clock Frequency						20	MHz	

Note: [1]When the input voltage is lower than 20mV, the conversion error is out of spec.

Table 123. Comparator Electrical Characteristics

		V_{DD} = 2.7 to 3.6V T_A = 0°C to +70°C			V_{DD} = 2.7 to 3.6V T_A = –40°C to +105°C				
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
V_{OS}	Input DC Offset					5		mV	
V_{CREF}	Programmable Internal Reference Voltage Range				0		1.8	V	User-programmable in 200 mV step
V_{CREF}	Programmable internal reference voltage				0.92	1.0	1.08	V	Default (CMP0[REFLVL]=5H)
T_{PROP}	Propagation delay					100		ns	
V_{HYS}	Input hysteresis					8		mV	

Low Power Control

For more information about the Power Control Register, see the Power Control Register Definitions section on page 31.

Hex Address: F80

Table 151. Power Control Register 0 (PWRCTL0)

Bit	7	6	5	4	3	2	1	0
Field	Reserved			VBO	Reserved	Reserved	COMP	Reserved
RESET	1	0	0	0	1	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F80H							

Hex Address: F81

This address range is reserved.

LED Controller

For more information about the LED Drive registers, see the GPIO Control Register Definitions section on page 39.

Hex Address: F82

Table 152. LED Drive Enable (LEDEN)

Bit	7	6	5	4	3	2	1	0
Field	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F82H							

Trim Bit Control

For more information about the Trim Bit Control registers, see the Flash Option Bit Control Register Definitions section on page 126.

Hex Address: FF6

Table 189. Trim Bit Address Register (TRMADR)

Bit	7	6	5	4	3	2	1	0
Field	TRMADR - Trim Bit Address (00H to 1FH)							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF6H							

Hex Address: FF7

Table 190. Trim Bit Data Register (TRMDR)

Bit	7	6	5	4	3	2	1	0
Field	TRMDR - Trim Bit Data							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF7H							

Flash Memory Controller

For more information about the Flash Control registers, see the Flash Control Register Definitions section on page 118.

Hex Address: FF8

Table 191. Flash Control Register (FCTL)

Bit	7	6	5	4	3	2	1	0
Field	FCMD							
RESET	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
Address	FF8H							