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#### Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f1232ph020eg

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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# **Revision History**

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

Data	Revision	Chantor/Soction	Description	Page
Dale	Level	Chapter/Section	Description	NO.
Dec 2012	13	GPIO	Modified GPIO Port D0 language in Shared Reset Pin section and Port Alternate Func- tion Mapping table.	<u>35, 36</u>
Sep 2011	12	LED Drive Enable Register	Clarified statement surrounding the Alternate Function Register as it relates to the LED function; revised Sector Based Flash Protec- tion description; revised Packaging chapter.	<u>51,</u> <u>115,</u> <u>199</u>
Dec 2007	11	n/a	Updated all instances of <i>Z8 Encore! XP</i> <i>F0830</i> to <i>Z8 Encore! F0830</i> .	All
Nov 2007	10	DC Characteristics, On-Chip Peripheral AC and DC Electri- cal Characteristics	Updated Tables 116 and and 122.	<u>185,</u> 193
Sep 2007	09	Timers, PWM SINGLE OUT- PUT Mode, PWM DUAL OUT- PUT Mode, Analog-to-Digital Converter, Reference Buffer.	Updated Figures 2 and 4, Table 4.	<u>8, 9,</u> <u>11, 68,</u> <u>74, 75,</u> <u>98,</u> <u>101</u>
Apr 2007	08	Optimizing NVDS Memory Usage for Execution Speed, On-Chip Peripheral AC and DC Electrical Characteristics	Added a note under Table 93 in Nonvolatile Data Storage chapter. Updated Table 121 and Table 122 in Electrical Characteristics chapter. Other style updates.	<u>137,</u> <u>193,</u> <u>193</u>
Dec	07	General Purpose Input/Output	Added PD0 in Table 16.	<u>38</u>
2006		Overview, Interrupt Controller	Changed the number of interrupts to 17.	<u>1,5, 53</u>
		Nonvolatile Data Storage	Updated chapter.	<u>136</u>
		Oscillator Control Register Defi- nitions, AC Characteristics, On- Chip Peripheral AC and DC Electrical Characteristics	Updated Tables 117 and 122. Added Figure 24.	<u>156,</u> <u>189,</u> <u>193</u>
		Ordering Information	Updated Part Number Suffix Designations.	<u>205</u>
		n/a	Removed Preliminary stamp from footer.	All

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#### **Reset Controller**

The Z8 Encore! F0830 Series products are reset using any one of the following: the RESET pin, Power-On Reset, Watchdog Timer (WDT) time-out, STOP Mode exit or Voltage Brown-Out (VBO) warning signal. The RESET pin is bidirectional; i.e., it functions as a reset source as well as a reset indicator.

## **On-Chip Debugger**

The Z8 Encore! F0830 Series products feature an integrated On-Chip Debugger (OCD). The OCD provides a rich set of debugging capabilities, such as reading and writing registers, programming Flash memory, setting breakpoints and executing code. The OCD uses one single-pin interface for communication with an external host.

## **Acronyms and Expansions**

This document references a number of acronyms; each is expanded in Table 2 for the reader's understanding.

Acronyms	Expansions
ADC	Analog-to-Digital Converter
NVDS	Nonvolatile Data Storage
WDT	Watchdog Timer
GPIO	General-Purpose Input/Output
OCD	On-Chip Debugger
POR	Power-On Reset
VBO	Voltage Brown-Out
IPO	Internal Precision Oscillator
PDIP	Plastic Dual Inline Package
SOIC	Small Outline Integrated Circuit
SSOP	Small Shrink Outline Package
QFN	Quad Flat No Lead
IRQ	Interrupt request
ISR	Interrupt service routine
MSB	Most significant byte
LSB	Least significant byte
PWM	Pulse Width Modulation
SAR	Successive Approximation Regis-

#### Table 2. Acronyms and Expansions

# **Pin Description**

The Z8 Encore! F0830 Series products are available in a variety of package styles and pin configurations. This chapter describes the signals and the pin configurations for each of the package styles. For information about the physical package specifications, see the <u>Packaging</u> chapter on page 199.

# **Available Packages**

Table 3 lists the package styles that are available for each device in the Z8 Encore! F0830 Series product line.

Part Number	ADC	20-pin QFN	20-pin SOIC	20-pin SSOP	20-pin PDIP	28-pin QFN	28-pin SOIC	28-pin SSOP	28-pin PDIP
Z8F1232	Yes	Х	Х	Х	Х	Х	Х	Х	Х
Z8F1233	No	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0830	Yes	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0831	No	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0430	Yes	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0431	No	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0230	Yes	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0231	No	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0130	Yes	Х	Х	Х	Х	Х	Х	Х	Х
Z8F0131	No	Х	Х	Х	Х	Х	Х	Х	Х

Table 3. Z8 Encore! F0830 Series Package Options

# **Pin Configurations**

Figures 2 and 3 display the pin configurations of all of the packages available in the Z8 Encore! F0830 Series. See <u>Table 4</u> on page 11 for a description of the signals. Analog input alternate functions (ANAx) are not available on the following devices:

- Z8F0831
- Z8F0431
- Z8F0131
- Z8F0231
- Z8F1233

Signal Mnemonic	I/O	Description
Oscillators		
X <sub>IN</sub>	I	External crystal input. This is the input pin to the crystal oscillator. A crystal can be connected between it and the <b>XOUT</b> pin to form the oscillator. In addition, this pin is used with external RC networks or external clock drivers to provide the system clock.
X <sub>OUT</sub>	0	External crystal output. This pin is the output of the crystal oscillator. A crystal can be connected between it and the <b>XIN</b> pin to form the oscillator.
Clock Input		
CLKIN	Ι	Clock input signal. This pin may be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All Port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the On-Chip Debugger.
		<b>Caution:</b> The DBG pin is open-drain and requires an external pull-up resistor to ensure proper operation.
Reset		
RESET	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! forces this pin low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V <sub>DD</sub>	I	Digital power supply.
AV <sub>DD</sub>	Ι	Analog power supply.
V <sub>SS</sub>	Ι	Digital ground.
AV <sub>SS</sub>	Ι	Analog ground.
Note: The AV <sub>DD</sub> and <i>A</i> and PB7 on 28-	AV <sub>SS</sub> sig pin pacł	nals are available only in the 28-pin packages with ADC. They are replaced by PB6 kages without ADC.

#### Table 4. Signal Descriptions (Continued)

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# **Register Map**

Table 8 provides an address map of the Z8 Encore! F0830 Series register file. Not all devices and package styles in the Z8 Encore! F0830 Series support the ADC or all of the GPIO ports. Consider registers for unimplemented peripherals as reserved.

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No.
General Purpose	RAM			
000–0FF	General purpose register file RAM	—	XX	
100-EFF	Reserved	_	XX	
Timer 0				
F00	Timer 0 high byte	T0H	00	83
F01	Timer 0 low byte	TOL	01	83
F02	Timer 0 reload high byte	TORH	FF	85
F03	Timer 0 reload low byte	TORL	FF	85
F04	Timer 0 PWM high byte	<b>T0PWMH</b>	00	86
F05	Timer 0 PWM low byte	TOPWML	00	86
F06	Timer 0 control 0	T0CTL0	00	87
F07	Timer 0 control 1	T0CTL1	00	88
Timer 1				
F08	Timer 1 high byte	T1H	00	83
F09	Timer 1 low byte	T1L	01	83
F0A	Timer 1 reload high byte	T1RH	FF	85
F0B	Timer 1 reload low byte	T1RL	FF	85
F0C	Timer 1 PWM high byte	T1PWMH	00	86
F0D	Timer 1 PWM low byte	T1PWML	00	86
F0E	Timer 1 control 0	T1CTL0	00	87
F0F	Timer 1 control 1	T1CTL1	00	83
F10–F6F	Reserved		XX	
Analog-to-Digita	I Converter (ADC)			
F70	ADC control 0	ADCCTL0	00	102
F71	Reserved	_	XX	
F72	ADC data high byte	ADCD_H	XX	103

#### Table 8. Register File Address Map

Note: XX = Undefined.

• Writing 1 to the IRQE bit in the Interrupt Control Register

Interrupts are globally disabled by any of the following actions:

- Execution of a DI (disable interrupt) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the Interrupt Controller
- Writing a 0 to the IRQE bit in the Interrupt Control Register
- Reset
- Execution of a trap instruction
- Illegal instruction Trap
- Primary oscillator fail trap
- Watchdog Oscillator fail trap

#### **Interrupt Vectors and Priority**

The Interrupt Controller supports three levels of interrupt priority. Level 3 is the highest priority, level 2 is the second highest priority and level 1 is the lowest priority. If all of the interrupts are enabled with identical interrupt priority (all as level 2 interrupts, for example), the interrupt priority is assigned from highest to lowest as specified in <u>Table 34</u> on page 54. Level 3 interrupts are always assigned higher priority than level 2 interrupts and level 2 interrupts are assigned higher priority than level 1 interrupts. Within each interrupt priority level (level 1, level 2 or level 3), priority is assigned as specified in Table 34, above. Reset, Watchdog Timer interrupt (if enabled), primary oscillator fail trap, Watchdog Oscillator fail trap and illegal instruction trap always have highest (level 3) priority.

#### **Interrupt Assertion**

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the interrupt request register is cleared. Writing 0 to the corresponding bit in the interrupt request register clears the interrupt request.

**Caution:** Zilog recommends not using a coding style that clears bits in the Interrupt Request registers. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost. See Example 1, which follows.

**Example 1.** A poor coding style that can result in lost interrupt requests:

## Interrupt Edge Select Register

The interrupt edge select (IRQES) register determines whether an interrupt is generated for the rising edge or falling edge on the selected GPIO Port A or Port D input pin. See Table 47.

Bit	7	6	5	4	3	2	1	0
Field	IES7	IES6	IES5	IES4	IES3	IES2	IES1	IES0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address				FC	DH			

#### Table 47. Interrupt Edge Select Register (IRQES)

# Bit Description [7] Interrupt Edge Select x IESx 0 = An interrupt request is generated on the falling edge of the PAx input or PDx. 1 = An interrupt request is generated on the rising edge of the PAx input or PDx. Note: x indicates register bits in the address range 7–0.

- 5. Enable the timer interrupt, if appropriate and set the timer interrupt priority by writing to the relevant interrupt registers. By default, the timer interrupt is generated for both input capture and Reload events. If appropriate, configure the timer interrupt to be generated only at the input capture event or the reload event by setting the TICONFIG field of the TxCTL1 Register.
- 6. Configure the associated GPIO port pin for the timer input alternate function.
- 7. Write to the Timer Control Register to enable the timer and initiate counting.

In CAPTURE Mode, the elapsed time between the timer start and the capture event can be calculated using the following equation:

Capture Elapsed Time (s) =  $\frac{(Capture Value - Start Value) \times Prescale}{System Clock Frequency (Hz)}$ 

#### **CAPTURE RESTART Mode**

In CAPTURE RESTART Mode, the current timer count value is recorded when the acceptable external timer input transition occurs. The capture count value is written to the timer PWM High and Low Byte registers. The timer input is the system clock. The TPOL bit in the Timer Control Register determines whether the capture occurs on a rising edge or a falling edge of the timer input signal. When the capture event occurs, an interrupt is generated and the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in the TxCTL1 Register is set to indicate that the timer interrupt has been caused by an input capture event.

If no capture event occurs, the timer counts up to 16-bit compare value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes. The INPCAP bit in the TxCTL1 Register is cleared to indicate that the timer interrupt has not been caused by an input capture event.

Observe the following steps for configuring a timer for CAPTURE RESTART Mode and for initiating the count:

- 1. Write to the Timer Control Register to:
  - Disable the timer
  - Configure the timer for CAPTURE RESTART Mode; setting the mode also involves writing to TMODEHI bit in the TxCTL1 Register
  - Set the prescale value
  - Set the capture edge (rising or falling) for the timer input
- 2. Write to the Timer High and Low Byte registers to set the starting count value (typically 0001H).

Bit	Description
[7:0]	Timer High and Low Bytes
TH, TL	These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

# **Timer 0–1 Control Registers**

The Timer Control registers are 8-bit read/write registers that control the operation of their associated counter/timers.

### Time 0–1 Control Register 0

The Timer Control 0 (TxCTL0) and Timer Control 1 (TxCTL1) registers determine the timer operating mode. These registers also include a programmable PWM deadband delay, two bits to configure the timer interrupt definition, and a status bit to identify if the most recent timer interrupt is caused by an input capture event.

						-		
Bit	7	6	5	4	3	2	1	0
Field	TMODEHI	TICO	NFIG	Reserved		PWMD		INPCAP
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F06H, F0EH							

Table 56. Timer 0–	Control Register	0 (TxCTL0)
--------------------	------------------	------------

Bit	Description
[7] TMODEHI	<b>Timer Mode High Bit</b> This bit along with the TMODE field in the TxCTL1 Register determines the operating mode of the timer. This is the most significant bit of the timer mode selection value. See the TxCTL1 Register description on the next page for additional details.
[6:5] TICONFIG	Timer Interrupt ConfigurationThis field configures timer interrupt definition. $0x = Timer$ interrupt occurs on all of the defined reload, compare and input events. $10 = Timer$ interrupt occurs only on defined input capture/deassertion events. $11 = Timer$ interrupt occurs only on defined reload/compare events.
[4]	<b>Reserved</b> This bit is reserved and must be programmed to 0.
[3:1] PWMD	<b>PWM Delay Value</b> This field is a programmable delay to control the number of system clock cycles delay         before the timer output and the timer output complement are forced to their Active state.         000 = No delay.         001 = 2 cycles delay.         010 = 4 cycles delay.         011 = 8 cycles delay.         100 = 16 cycles delay.         101 = 32 cycles delay.         110 = 64 cycles delay.         111 = 128 cycles delay.

# Comparator

The Z8 Encore! F0830 Series devices feature a general purpose comparator that compares two analog input signals. A GPIO (CINP) pin provides the positive comparator input. The negative input (CINN) can be taken from either an external GPIO pin or from an internal reference. The output is available as an interrupt source or can be routed to an external pin using the GPIO multiplex. The comparator includes the following features:

- Positive input is connected to a GPIO pin
- Negative input can be connected to either a GPIO pin or a programmable internal reference
- Output can be either an interrupt source or an output to an external pin

# Operation

One of the comparator inputs can be connected to an internal reference that is a user-selectable reference and is user-programmable with 200 mV resolution.

The comparator can be powered down to save supply current. For details, see the <u>Power</u> <u>Control Register 0</u> section on page 31.

**Caution:** As a result of the propagation delay of the comparator, Zilog does not recommend enabling the comparator without first disabling interrupts and waiting for the comparator output to settle. This delay prevents spurious interrupts after comparator enabling.

The following example shows how to safely enable the comparator:

```
di
ld cmp0,r0; load some new configuration
nop
nop ; wait for output to settle
clr irq0; clear any spurious interrupts pending
ei
```

Flash information area is mapped into program memory and overlays the 128 bytes in the address range FE00H to FE7FH. When the information area access is enabled, all reads from these program memory addresses return the information area data rather than the program memory data. Access to the Flash information area is read-only.

The trim bits are handled differently than the other Zilog Flash option bits. The trim bits are the hybrid of the user option bits and the standard Zilog option bits. These trim bits must be user-accessible for reading at all times using external registers regardless of the state of bit 7 in the Flash Page Select Register. Writes to the trim space change the value of the Option Bit Holding Register but do not affect the Flash bits, which remain as read-only.

Program Memory	
Address (Hex)	Function
FE00–FE3F	Zilog option bits
FE40–FE53	Part number 20-character ASCII alphanumeric code Left justified and filled with FH
FE54–FE5F	Reserved
FE60–FE7F	Reserved

Table 70. Z8F083 Flash Memory Area Map

## Operation

The Flash Controller programs and erases Flash memory. The Flash Controller provides the proper Flash controls and timing for byte programming, page erase and mass erase of Flash memory.

The Flash Controller contains several protection mechanisms to prevent accidental programming or erasure. These mechanism operate on the page, sector and full-memory levels.

The flowchart in Figure 19 display basic Flash Controller operation. The following subsections provide details about the various operations (Lock, Unlock, Byte Programming, Page Protect, Page Unprotect, Page Select Page Erase and Mass Erase) displayed in Figure 19. ory size and is approximately equal to the system clock period multiplied by the number of bytes in program memory.

```
DBG \leftarrow 0EH
DBG \rightarrow CRC[15:8]
DBG \rightarrow CRC[7:0]
```

**Step Instruction (10H).** The step instruction command, steps one assembly instruction at the current program counter (PC) location. If the device is not in DEBUG Mode or the Flash read protect option bit is enabled, the OCD ignores this command.

```
DBG \leftarrow 10H
```

**Stuff Instruction (11H).** The stuff instruction command, steps one assembly instruction and allows specification of the first byte of the instruction. The remaining 0–4 bytes of the instruction are read from program memory. This command is useful for stepping over instructions where the first byte of the instruction has been overwritten by a breakpoint. If the device is not in DEBUG Mode or the Flash read protect option bit is enabled, the OCD ignores this command.

```
DBG \leftarrow 11H
DBG \leftarrow opcode[7:0]
```

**Execute Instruction (12H).** The execute instruction command allows sending an entire instruction to be executed to the eZ8 CPU. This command can also step over breakpoints. The number of bytes to send for the instruction depends on the opcode. If the device is not in DEBUG Mode or the Flash read protect option bit is enabled, this command reads and discards one byte.

```
DBG \leftarrow 12H
DBG \leftarrow 1-5 byte opcode
```

# **On-Chip Debugger Control Register Definitions**

This section describes the features of the On-Chip Debugger Control and Status registers.

#### **OCD Control Register**

The OCD Control Register controls the state of the On-Chip Debugger. This register is used to enter or exit DEBUG Mode and to enable the BRK instruction. It can also reset the Z8 Encore! F0830 Series device.

A reset and stop function can be achieved by writing 81H to this register. A *reset and go* function can be achieved by writing 41H to this register. If the device is in DEBUG Mode, a run function can be implemented by writing 40H to this register.

# **OCD Status Register**

The OCD Status Register reports status information about the current state of the debugger and the system.

Table 97.	OCD	Status	Register	(OCDSTAT)
-----------	-----	--------	----------	-----------

Bit	7	6	5	4	3	2	1	0				
Field	DBG	HALT	FRPENB	Reserved								
RESET	0	0	0	0	0	0	0	0				
R/W	R	R	R	R	R	R	R	R				
Bit	Descriptio	n										

Bit	Description
[7] DBG	Debug Status 0 = NORMAL Mode. 1 = DEBUG Mode.
[6] HALT	HALT Mode 0 = Not in HALT Mode. 1 = In HALT Mode.
[5] FRPENB	Flash Read Protect Option Bit Enable 0 = FRP bit enabled, that allows disabling of many OCD commands. 1 = FRP bit has no effect.
[4:0]	Reserved These bits are reserved and must be programmed to 00000.

When selecting a new clock source, the primary oscillator failure detection circuitry and the Watchdog Timer Oscillator failure circuitry must be disabled. If POFEN and WOFEN are not disabled prior to a clock switch-over, it is possible to generate an interrupt for a failure of either oscillator. The failure detection circuitry can be enabled anytime after a successful write of OSCSEL in the Oscillator Control Register.

The Internal Precision Oscillator is enabled by default. If the user code changes to a different oscillator, it may be appropriate to disable the IPO for power savings. Disabling the IPO does not occur automatically.

#### **Clock Failure Detection and Recovery**

#### **Primary Oscillator Failure**

The Z8F04xA family devices can generate nonmaskable interrupt-like events when the primary oscillator fails. To maintain system function in this situation, the clock failure recovery circuitry automatically forces the Watchdog Timer Oscillator to drive the system clock. The Watchdog Timer Oscillator must be enabled to allow the recovery. Although this oscillator runs at a much slower speed than the original system clock, the CPU continues to operate, allowing execution of a clock failure vector and software routines that either remedy the oscillator failure or issue a failure alert. This automatic switch-over is not available if the Watchdog Timer is the primary oscillator. It is also unavailable if the Watchdog Timer reset function outlined in the Watchdog Timer chapter of this document.

The primary oscillator failure detection circuitry asserts if the system clock frequency drops below 1 KHz  $\pm$ 50%. If an external signal is selected as the system oscillator, it is possible that a very slow but nonfailing clock can generate a failure condition. Under these conditions, do not enable the clock failure circuitry (POFEN must be deasserted in the OSCCTL Register).

#### Watchdog Timer Failure

In the event of failure of a Watchdog Timer Oscillator, a similar nonmaskable interruptlike event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a primary oscillator failure. The failure detection circuitry does not function if the Watchdog Timer is used as the primary oscillator or if the Watchdog Timer Oscillator has been disabled. For either of these cases, it is necessary to disable the detection circuitry by deasserting the WDFEN bit of the OSCCTL Register.

The Watchdog Timer Oscillator failure detection circuit counts system clocks while looking for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which the Watchdog Timer failure is detected. A very slow system clock results in very slow detection times.

Assembly		Address Mode		Op Code(s)	Flags						Fetch	Instr.
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	Cycles	Cycles
DJNZ dst, RA	$dst \leftarrow dst - 1$ if $dst \neq 0$ PC $\leftarrow$ PC + X	r		0A–FA	_	-	-	-	-	_	2	3
EI	IRQCTL[7] ← 1			9F	_	_	_	_	_	_	1	2
HALT	HALT Mode			7F	-	-	_	-	_	-	1	2
INC dst	dst ← dst + 1	R		20	-	*	*	-	_	_	2	2
		IR		21	_						2	3
		r		0E-FE	_						1	2
INCW dst	dst ← dst + 1	RR		A0	-	*	*	*	-	-	2	5
		IRR		A1	_						2	6
IRET	$FLAGS \leftarrow @SP$ $SP \leftarrow SP + 1$ $PC \leftarrow @SP$ $SP \leftarrow SP + 2$ $IRQCTL[7] \leftarrow 1$			BF	*	*	*	*	*	*	1	5
JP dst	PC ← dst	DA		8D	_	_	_	_	_	_	3	2
		IRR		C4	_						2	3
JP cc, dst	if cc is true PC ← dst	DA		0D-FD	-	-	_	-	-	-	3	2
JR dst	$PC \leftarrow PC + X$	DA		8B	-	_	-	-	-	_	2	2
JR cc, dst	if cc is true PC $\leftarrow$ PC + X	DA		0B-FB	-	-	-	-	-	_	2	2

#### Table 113. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation:

\* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

					• •							
Assembly		Address Mode		Op Code(s)	Flags						Fetch	Instr
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	Cycles	Cycles
LD dst, rc	$dst \gets src$	r	IM	0C-FC	_	_	_	_	_	_	2	2
		r	X(r)	C7	_						3	3
		X(r)	r	D7	_						3	4
		r	lr	E3	_						2	3
		R	R	E4	_						3	2
		R	IR	E5	_						3	4
		R	IM	E6	_						3	2
		IR	IM	E7	_						3	3
		lr	r	F3	_						2	3
		IR	R	F5	_						3	3
LDC dst, src	dst ← src	r	Irr	C2	_	-	-	_	_	-	2	5
		lr	Irr	C5	_						2	9
		Irr	r	D2	_						2	5
LDCI dst, src	$dst \gets src$	lr	Irr	C3	_	-	_	_	—	_	2	9
	r ← r + 1 rr ← rr + 1	Irr	lr	D3							2	9
LDE dst, src	dst ← src	r	Irr	82	-	-	-	—	_	-	2	5
		Irr	r	92							2	5
LDEI dst, src	$dst \gets src$	lr	Irr	83	-	-	-	_	_	-	2	9
	r ← r + 1 rr ← rr + 1	Irr	lr	93							2	9
LDWX dst, src	dst $\leftarrow$ src	ER	ER	1FE8	-	_	_	_	_	_	5	4

#### Table 113. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation:

\* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

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Figure 30. Second Op Code Map after 1FH

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