



Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	-
Purchase URL	<a href="https://www.e-xfl.com/product-detail/zilog/z8f1233hh020eg">https://www.e-xfl.com/product-detail/zilog/z8f1233hh020eg</a>

## Nonvolatile Data Storage

The Nonvolatile Data Storage (NVDS) function uses a hybrid hardware/software scheme to implement a byte-programmable data memory and is capable of storing about 100,000 write cycles.

## Internal Precision Oscillator

The Internal Precision Oscillator (IPO) function, with an accuracy of  $\pm 4\%$  full voltage/temperature range, is a trimmable clock source that requires no external components.

## External Crystal Oscillator

The crystal oscillator circuit provides highly accurate clock frequencies using an external crystal, ceramic resonator or RC network.

## 10-Bit Analog-to-Digital Converter

The optional Analog-to-Digital Converter (ADC) converts an analog input signal to a 10-bit binary number. The ADC accepts inputs from eight different analog input pins.

## Analog Comparator

The analog comparator compares the signal at an input pin with either an internal programmable reference voltage or with a signal at the second input pin. The comparator output is used either to drive a logic output pin or to generate an interrupt.

## Timers

Two enhanced 16-bit reloadable timers can be used for timing/counting events or for motor control operations. These timers provide a 16-bit programmable reload counter and operate in ONE-SHOT, CONTINUOUS, GATED, CAPTURE, CAPTURE RESTART, COMPARE, CAPTURE and COMPARE, PWM SINGLE OUTPUT and PWM DUAL OUTPUT Modes.

## Interrupt Controller

The Z8 Encore! F0830 Series products support seventeen interrupt sources with sixteen interrupt vectors: up to five internal peripheral interrupts and up to twelve GPIO interrupts. These interrupts have three levels of programmable interrupt priority.

## ***Reset and Stop Mode Recovery***

The reset controller in the Z8 Encore! F0830 Series controls RESET and Stop Mode Recovery operations. In a typical operation, the following events can cause a reset:

- Power-On Reset (POR)
- Voltage Brown-Out (VBO)
- Watchdog Timer time-out (when configured by the WDT\_RES Flash option bit to initiate a reset)
- External  $\overline{\text{RESET}}$  pin assertion (when the alternate RESET function is enabled by the GPIO register)
- On-Chip Debugger initiated reset (OCDCTL[0] set to 1)

When the device is in STOP Mode, a Stop Mode Recovery event is initiated by either of the following occurrences:

- A Watchdog Timer time-out
- A GPIO port input pin transition on an enabled Stop Mode Recovery source

The VBO circuitry on the device generates a VBO reset when the supply voltage drops below a minimum safe level.

### **Reset Types**

The Z8 Encore! F0830 Series provides different types of Reset operations. Stop Mode Recovery is considered a form of reset. Table 9 lists the types of resets and their operating characteristics. The duration of a system reset is longer if the external crystal oscillator is enabled by the Flash option bits; the result is additional time for oscillator startup.

- Writing 1 to the IRQE bit in the Interrupt Control Register

Interrupts are globally disabled by any of the following actions:

- Execution of a `DI` (disable interrupt) instruction
- eZ8 CPU acknowledgement of an interrupt service request from the Interrupt Controller
- Writing a 0 to the IRQE bit in the Interrupt Control Register
- Reset
- Execution of a trap instruction
- Illegal instruction Trap
- Primary oscillator fail trap
- Watchdog Oscillator fail trap

## Interrupt Vectors and Priority

The Interrupt Controller supports three levels of interrupt priority. Level 3 is the highest priority, level 2 is the second highest priority and level 1 is the lowest priority. If all of the interrupts are enabled with identical interrupt priority (all as level 2 interrupts, for example), the interrupt priority is assigned from highest to lowest as specified in [Table 34](#) on page 54. Level 3 interrupts are always assigned higher priority than level 2 interrupts and level 2 interrupts are assigned higher priority than level 1 interrupts. Within each interrupt priority level (level 1, level 2 or level 3), priority is assigned as specified in [Table 34](#), above. Reset, Watchdog Timer interrupt (if enabled), primary oscillator fail trap, Watchdog Oscillator fail trap and illegal instruction trap always have highest (level 3) priority.

## Interrupt Assertion

Interrupt sources assert their interrupt requests for only a single system clock period (single pulse). When the interrupt request is acknowledged by the eZ8 CPU, the corresponding bit in the interrupt request register is cleared. Writing 0 to the corresponding bit in the interrupt request register clears the interrupt request.

---

**!** **Caution:** Zilog recommends not using a coding style that clears bits in the Interrupt Request registers. All incoming interrupts received between execution of the first LDX command and the final LDX command are lost. See Example 1, which follows.

---

**Example 1.** A poor coding style that can result in lost interrupt requests:

Table 45. IRQ2 Enable High Bit Register (IRQ2ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENH	C2ENH	C1ENH	C0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC7H							

Bit	Description
[7:4]	<b>Reserved</b> These registers are reserved and must be programmed to 0000.
[3] C3ENH	<b>Port C3 Interrupt Request Enable High Bit</b>
[2] C2ENH	<b>Port C2 Interrupt Request Enable High Bit</b>
[1] C1ENH	<b>Port C1 Interrupt Request Enable High Bit</b>
[0] C0ENH	<b>Port C0 Interrupt Request Enable High Bit</b>

Table 46. IRQ2 Enable Low Bit Register (IRQ2ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENL	C2ENL	C1ENL	C0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC8H							

Bit	Description
[7:4]	<b>Reserved</b> These registers are reserved and must be programmed to 0000.
[3] C3ENL	<b>Port C3 Interrupt Request Enable Low Bit</b>
[2] C2ENL	<b>Port C2 Interrupt Request Enable Low Bit</b>
[1] C1ENL	<b>Port C1 Interrupt Request Enable Low Bit</b>
[0] C0ENL	<b>Port C0 Interrupt Request Enable Low Bit</b>

6. Write to the Timer Control Register to enable the timer.
7. Counting begins on the first appropriate transition of the timer input signal. No interrupt is generated by the first edge.

In CAPTURE/COMPARE Mode, the elapsed time from timer start to capture event can be calculated using the following equation:

$$\text{Capture Elapsed Time (s)} = \frac{(\text{Capture Value} - \text{Start Value}) \times \text{Prescale}}{\text{System Clock Frequency (Hz)}}$$

## Reading the Timer Count Values

The current count value in the timers can be read while counting (enabled). This capability has no effect on Timer operation. When the timer is enabled and the Timer High Byte Register is read, the contents of the timer low byte register are placed in a holding register. A subsequent read from the timer low byte register returns the value in the holding register. This operation allows accurate reads of the full 16-bit timer count value when enabled. When the timers are not enabled, a read from the timer low byte register returns the actual value in the counter.

## Timer Pin Signal Operation

Timer output is a GPIO port pin alternate function. The timer output is toggled every time the counter is reloaded.

The timer input can be used as a selectable counting source. It shares the same pin as the complementary timer output. When selected by the GPIO alternate function registers, this pin functions as a timer input in all modes except for the DUAL PWM OUTPUT Mode. For this mode, no timer input is available.

## Timer Control Register Definitions

This section defines the features of the following Timer Control registers.

Timer 0–1 High and Low Byte Registers: see page 83

Timer Reload High and Low Byte Registers: see page 85

Timer 0–1 PWM High and Low Byte Registers: see page 86

Timer 0–1 Control Registers: see page 87

### Timer 0–1 High and Low Byte Registers

The Timer 0–1 High and Low Byte (TxH and TxL) registers, shown in Tables 50 and 51, contain the current 16-bit timer count value. When the timer is enabled, a read from TxH causes the value in TxL to be stored in a temporary holding register. A read from TxL always returns this temporary register content when the timer is enabled; however, when the timer is disabled, a read from the TxL reads the TxL Register content directly.

Writing to the Timer High and Low Byte registers while the timer is enabled is not recommended. There are no temporary holding registers available for write operations; therefore, simultaneous 16-bit writes are not possible. If either the timer High or Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low byte) at the next clock edge. The counter continues counting from the new value.

**Table 50. Timer 0–1 High Byte Register (TxH)**

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F00H, F08H							

**Table 51. Timer 0–1 Low Byte Register (TxL)**

Bit	7	6	5	4	3	2	1	0
Field	TL							
RESET	0	0	0	0	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F01H, F09H							

## ADC Interrupt

The ADC can generate an interrupt request when a conversion has been completed. An interrupt request that is pending when the ADC is disabled is not cleared automatically.

## Reference Buffer

The reference buffer, RBUF, supplies the reference voltage for the ADC. When enabled, the internal voltage reference generator supplies the ADC. When RBUF is disabled, the ADC must have the reference voltage supplied externally through the  $V_{REF}$  pin in 28-pin package. RBUF is controlled by the REFEN bit in the ADC Control Register.

## Internal Voltage Reference Generator

The internal voltage reference generator provides the voltage  $VR_2$ , for the RBUF.  $VR_2$  is 2V.

## Calibration and Compensation

A user can perform calibration and store the values into Flash or the user code can perform a manual offset calibration. There is no provision for manual gain calibration.

## ADC Control Register Definitions

The ADC Control registers are defined in this section.



## ADC Control Register 0

The ADC Control 0 Register, shown in Table 63, initiates an A/D conversion and provides ADC status information.

**Table 63. ADC Control Register 0 (ADCCTL0)**

Bit	7	6	5	4	3	2	1	0
Field	START	Reserved	REFEN	ADCEN	Reserved	ANAIN[2:0]		
RESET	0	0	0	0	0	0	0	0
R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F70h							

Bit	Description
[7] START	<b>ADC Start/Busy</b> 0 = Writing to 0 has no effect; reading a 0 indicates that the ADC is available to begin a conversion. 1 = Writing to 1 starts a conversion; reading a 1 indicates that a conversion is currently in progress.
[6]	<b>Reserved</b> This bit is reserved and must be programmed to 0.
[5] REFEN	<b>Reference Enable</b> 0 = Internal reference voltage is disabled allowing an external reference voltage to be used by the ADC. 1 = Internal reference voltage for the ADC is enabled. The internal reference voltage can be measured on the V <sub>REF</sub> pin.
[4] ADCEN	<b>ADC Enable</b> 0 = ADC is disabled for low power operation. 1 = ADC is enabled for normal use.
[3]	<b>Reserved</b> This bit is reserved and must be programmed to 0.
[2:0] ANAIN	<b>Analog Input Select</b> 000 = ANA0 input is selected for analog to digital conversion. 001 = ANA1 input is selected for analog to digital conversion. 010 = ANA2 input is selected for analog to digital conversion. 011 = ANA3 input is selected for analog to digital conversion. 100 = ANA4 input is selected for analog to digital conversion. 101 = ANA5 input is selected for analog to digital conversion. 110 = ANA6 input is selected for analog to digital conversion. 111 = ANA7 input is selected for analog to digital conversion.

## Option Bit Types

This section describes the two types of Flash option bits offered in the F0830 Series.

### User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits is provided because these locations contain application specific device configurations. The information contained here is lost when page 0 of program memory is erased.

### Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered by the user. Program memory can be erased without endangering these values. It is possible to alter working values of these bits by accessing the trim bit address and data registers, but these working values are lost after a power loss.

There are 32 bytes of trim data. To modify one of these values, the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data Register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data Register returns the working value of the target trim data byte.

---

► **Note:** The trim address range is from information address 20–3F only. The remaining information page is not accessible via the Trim Bit Address and Data registers.

---

During reset, the first 43 system clock cycles perform 43 Flash accesses. The six bits of the counter provide the lower six bits of the Flash memory address. All other address bits are set to 0. The option bit registers use the 6-bit address from the counter as an address and latch the data from the Flash on the positive edge of the IPO clock, allowing for a maximum of 344-bits (43 bytes) of option information to be read from Flash.

Because option information is stored in both the first two bytes of program memory and in the information area of Flash memory, the data must be placed in specific locations to be read correctly. In this case, the first two bytes at addresses 0 and 1 in program memory are read out and the remainder of the bytes are read out of the Flash information area.

## Byte Read

To read a byte from the NVDS array, user code must first push the address onto the stack. User code issues a `CALL` instruction to the address of the byte-read routine (`0x2000`). At the return from the subroutine, the read byte resides in working register R0 and the read status byte resides in working register R1. The bit fields of this status byte are defined in Table 92. Additionally, the user code should pop the address byte off the stack.

The read routine uses 16 bytes of stack space in addition to the one byte of address pushed by the user code. Sufficient memory must be available for this stack usage.

Due to the Flash memory architecture, NVDS reads exhibit a nonuniform execution time. A read operation takes between 71  $\mu$ s and 258  $\mu$ s (assuming a 20MHz system clock). Slower system clock speeds result in proportionally higher execution times.

NVDS byte reads from invalid addresses (those exceeding the NVDS array size) return `0xff`. Illegal read operations have a 6  $\mu$ s execution time.

The status byte returned by the NVDS read routine is zero for a successful read. If the status byte is nonzero, there is a corrupted value in the NVDS array at the location being read. In this case, the value returned in R0 is the byte most recently written to the array that does not have an error.

**Table 92. Read Status Byte**

Bit	7	6	5	4	3	2	1	0
Field	Reserved			DE	Reserved	FE	IGADDR	Reserved
Default Value	0	0	0	0	0	0	0	0

Bit	Description
[7:5]	<b>Reserved</b> These bits are reserved and must be programmed to 000.
[4] DE	<b>Data Error</b> When reading an NVDS address, if an error is found in the latest data corresponding to this NVDS address, this bit is set to 1. NVDS source code steps forward until it finds valid data at this address.
[3]	<b>Reserved</b> This bit is reserved and must be programmed to 0.
[2] FE	<b>Flash Error</b> If a Flash error is detected, this bit is set to 1.
[1] IGADDR	<b>Illegal Address</b> When NVDS byte reads from invalid addresses (those exceeding the NVDS array size) occur, this bit is set to 1.
[0]	<b>Reserved</b> This bit is reserved and must be programmed to 0.

## Operation

The following section describes the operation of the On-Chip Debugging function.

### OCD Interface

The On-Chip Debugger uses the DBG pin for communication with an external host. This one-pin interface is a bidirectional open-drain interface that transmits and receives data. Data transmission is half-duplex, which means that transmission and data retrieval cannot occur simultaneously. The serial data on the DBG pin is sent using the standard asynchronous data format defined in RS-232. This pin creates an interface between the Z8 Encore! F0830 Series products and the serial port of a host PC using minimal external hardware. Two different methods for connecting the DBG pin to an RS-232 interface are displayed in Figures 21 and 22. The recommended method is the buffered implementation depicted in Figure 22. The DBG pin must always be connected to  $V_{DD}$  through an external pull-up resistor.

---

**! Caution:** For proper operation of the On-Chip Debugger, all power pins ( $V_{DD}$  and  $AV_{DD}$ ) must be supplied with power and all ground pins ( $V_{SS}$  and  $AV_{SS}$ ) must be properly grounded. The DBG pin is open-drain and must always be connected to  $V_{DD}$  through an external pull-up resistor to ensure proper operation.

---

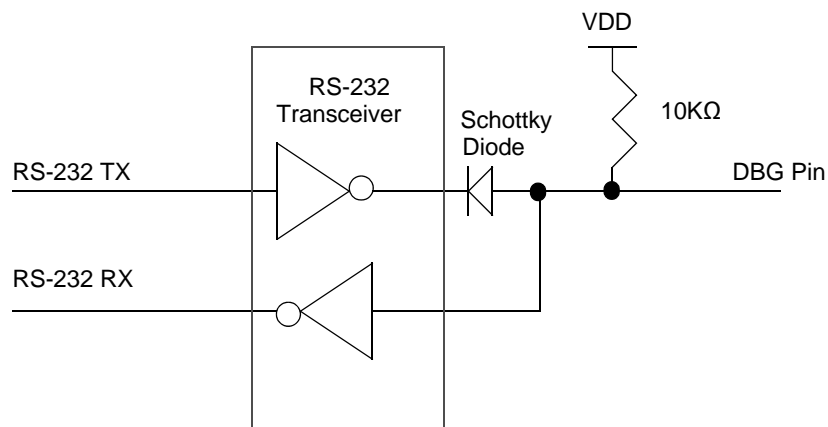


Figure 21. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #1 of 2

Table 96. OCD Control Register (OCDCTL)

Bit	7	6	5	4	3	2	1	0
Field	DBGMODE	BRKEN	DBGACK	Reserved				RST
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R	R	R/W

Bit	Description
[7] DBGMODE	<p><b>DEBUG Mode</b></p> <p>The device enters DEBUG Mode when this bit is 1. When in DEBUG Mode, the eZ8 CPU stops fetching new instructions. Clearing this bit causes the eZ8 CPU to restart. This bit is automatically set when a BRK instruction is decoded and breakpoints are enabled. If the Flash read protect option bit is enabled, this bit can only be cleared by resetting the device. It cannot be written to 0.</p> <p>0 = The Z8 Encore! F0830 Series device is operating in NORMAL Mode. 1 = The Z8 Encore! F0830 Series device is in DEBUG Mode.</p>
[6] BRKEN	<p><b>Breakpoint Enable</b></p> <p>This bit controls the behavior of the BRK instruction (opcode 00H). By default, breakpoints are disabled and the BRK instruction behaves similar to an NOP instruction. If this bit is 1 when a BRK instruction is decoded, the DBGMODE bit of the OCDCTL register is automatically set to 1.</p> <p>0 = Breakpoints are disabled. 1 = Breakpoints are enabled.</p>
[5] DBGACK	<p><b>Debug Acknowledge</b></p> <p>This bit enables the debug acknowledge feature. If this bit is set to 1, the OCD sends a Debug acknowledge character (FFH) to the host when a breakpoint occurs.</p> <p>0 = Debug acknowledge is disabled. 1 = Debug acknowledge is enabled.</p>
[4:1]	<p><b>Reserved</b></p> <p>These bits are reserved and must be programmed to 0000.</p>
[0] RST	<p><b>Reset</b></p> <p>Setting this bit to 1 resets the Z8F04xA family device. The device goes through a normal Power-On Reset sequence with the exception that the On-Chip Debugger is not reset. This bit is automatically cleared to 0 at the end of the reset sequence.</p> <p>0 = No effect. 1 = Reset the Flash read protect option bit device.</p>

# Internal Precision Oscillator

The Internal Precision Oscillator (IPO) is designed for use without external components. The user can either manually trim the oscillator for a nonstandard frequency or use the automatic factory-trimmed version to achieve a 5.53MHz frequency with  $\pm 4\%$  accuracy and 45%~55% duty cycle over the operating temperature and supply voltage of the device. The maximum start-up time of the IPO is 25 $\mu$ s. IPO features include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53MHz or 32.8kHz (contains both a FAST and a SLOW mode)
- Trimming possible through Flash option bits, with user override
- Elimination of crystals or ceramic resonators in applications where high timing accuracy is not required

## Operation

The internal oscillator is an RC relaxation oscillator with a minimized sensitivity to power supply variations. By using ratio-tracking thresholds, the effect of power supply voltage is cancelled out. The dominant source of oscillator error is the absolute variance of chip-level fabricated components, such as capacitors. An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed, the oscillator frequency is stable and does not require subsequent calibration. Trimming was performed during manufacturing and is not necessary for the user to repeat unless a frequency other than 5.53MHz (FAST mode) or 32.8kHz (SLOW mode) is required.

---

► **Note:** The user can power down the IPO block for minimum system power.

---

By default, the oscillator is configured through the Flash option bits. However, the user code can override these trim values, as described in the [Trim Bit Address Space](#) section on page 129.

Select one of two frequencies for the oscillator: 5.53MHz or 32.8 kHz, using the OSCSEL bits described in the [Oscillator Control](#) chapter on page 151.

Table 108. CPU Control Instructions

Mnemonic	Operands	Instruction
ATM	—	Atomic Execution
CCF	—	Complement Carry Flag
DI	—	Disable Interrupts
EI	—	Enable Interrupts
HALT	—	HALT Mode
NOP	—	No Operation
RCF	—	Reset Carry Flag
SCF	—	Set Carry Flag
SRP	src	Set Register Pointer
STOP	—	STOP Mode
WDT	—	Watchdog Timer Refresh

Table 109. Load Instructions

Mnemonic	Operands	Instruction
CLR	dst	Clear
LD	dst, src	Load
LDC	dst, src	Load Constant to/from Program Memory
LDCI	dst, src	Load Constant to/from Program Memory and Auto-Increment Addresses
LDE	dst, src	Load External Data to/from Data Memory
LDEI	dst, src	Load External Data to/from Data Memory and Auto-Increment Addresses
LDWX	dst, src	Load Word using Extended Addressing
LDX	dst, src	Load using Extended Addressing
LEA	dst, X(src)	Load Effective Address
POP	dst	Pop
POPX	dst	Pop using Extended Addressing
PUSH	src	Push
PUSHX	src	Push using Extended Addressing

Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
DJNZ dst, RA	$\text{dst} \leftarrow \text{dst} - 1$ if $\text{dst} \neq 0$ $\text{PC} \leftarrow \text{PC} + X$	r		0A–FA	–	–	–	–	–	–	2	3
EI	$\text{IRQCTL}[7] \leftarrow 1$			9F	–	–	–	–	–	–	1	2
HALT	HALT Mode			7F	–	–	–	–	–	–	1	2
INC dst	$\text{dst} \leftarrow \text{dst} + 1$	R		20	–	*	*	–	–	–	2	2
		IR		21							2	3
		r		0E–FE							1	2
INCW dst	$\text{dst} \leftarrow \text{dst} + 1$	RR		A0	–	*	*	*	–	–	2	5
		IRR		A1							2	6
IRET	$\text{FLAGS} \leftarrow @\text{SP}$ $\text{SP} \leftarrow \text{SP} + 1$ $\text{PC} \leftarrow @\text{SP}$ $\text{SP} \leftarrow \text{SP} + 2$ $\text{IRQCTL}[7] \leftarrow 1$			BF	*	*	*	*	*	*	1	5
JP dst	$\text{PC} \leftarrow \text{dst}$	DA		8D	–	–	–	–	–	–	3	2
		IRR		C4							2	3
JP cc, dst	if cc is true $\text{PC} \leftarrow \text{dst}$	DA		0D–FD	–	–	–	–	–	–	3	2
JR dst	$\text{PC} \leftarrow \text{PC} + X$	DA		8B	–	–	–	–	–	–	2	2
JR cc, dst	if cc is true $\text{PC} \leftarrow \text{PC} + X$	DA		0B–FB	–	–	–	–	–	–	2	2

Note: Flags Notation:

\* = Value is a function of the result of the operation.

– = Unaffected.

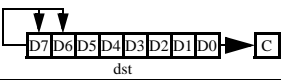

X = Undefined.

0 = Reset to 0.

1 = Set to 1.



Table 113. eZ8 CPU Instruction Summary (Continued)

Assembly Mnemonic	Symbolic Operation	Address Mode		Op Code(s) (Hex)	Flags						Fetch Cycles	Instr. Cycles
		dst	src		C	Z	S	V	D	H		
SRA dst		R		D0	*	*	*	0	-	-	2	2
		IR		D1							2	3
SRL dst		R		1F C0	*	*	0	*	-	-	3	2
		IR		1F C1							3	3
SRP src	RP ← src		IM	01	-	-	-	-	-	-	2	2
STOP	STOP Mode			6F	-	-	-	-	-	-	1	2
SUB dst, src	dst ← dst - src	r	r	22	*	*	*	*	1	*	2	3
		r	lr	23							2	4
		R	R	24							3	3
		R	IR	25							3	4
		R	IM	26							3	3
		IR	IM	27							3	4
SUBX dst, src	dst ← dst - src	ER	ER	28	*	*	*	*	1	*	4	3
		ER	IM	29							4	3
SWAP dst	dst[7:4] ↔ dst[3:0]	R		F0	X	*	*	X	-	-	2	2
		IR		F1							2	3
TCM dst, src	(NOT dst) AND src	r	r	62	-	*	*	0	-	-	2	3
		r	lr	63							2	4
		R	R	64							3	3
		R	IR	65							3	4
		R	IM	66							3	3
		IR	IM	67							3	4
TCMX dst, src	(NOT dst) AND src	ER	ER	68	-	*	*	0	-	-	4	3
		ER	IM	69							4	3

Note: Flags Notation:

\* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.

		Lower Nibble (Hex)															
		0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Upper Nibble (Hex)	0																
	1																
	2																
	3																
	4																
	5																
	6																
	7	3.2 PUS															
	8																
	9																
	A			3.3 CPC r1,r2	3.4 CPC r1,lr2	4.3 CPC R2,R1	4.4 CPC IR2,R1	4.3 CPC R1,IM	4.4 CPC IR1,IM	5.3 CPCX ER2,ER1	5.3 CPCX IM,ER1						
	B																
	C	3.2 SRL R1	3.3 SRL IR1														
	D																
	E									5, 4 LDWX ER2,ER1							
	F																

Figure 30. Second Op Code Map after 1FH

## DC Characteristics

Table 116 lists the DC characteristics of the Z8 Encore! F0830 Series products. All voltages are referenced to  $V_{SS}$ , the primary system ground.

**Table 116. DC Characteristics**

Symbol	Parameter	$T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$			$T_A = -40^{\circ}\text{C to } +105^{\circ}\text{C}$			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
$V_{DD}$	Supply Voltage				2.7	–	3.6	V	Power supply noise not to exceed 100mV peak to peak
$V_{IL1}$	Low Level Input Voltage				–0.3	–	$0.3 \cdot V_{DD}$	V	For all input pins except RESET.
$V_{IL2}$	Low Level Input Voltage				–0.3	–	0.8	V	For RESET.
$V_{IH1}$	High Level Input Voltage				2.0	–	5.5	V	For all input pins without analog or oscillator function.
$V_{IH2}$	High Level Input Voltage				2.0	–	$V_{DD} + 0.3$	V	For those pins with analog or oscillator function.
$V_{OL1}$	Low Level Output Voltage				–	–	0.4	V	$I_{OL} = 2\text{mA}$ ; $V_{DD} = 3.0\text{V}$ High Output Drive disabled.
$V_{OH1}$	High Level Output Voltage				2.4	–	–	V	$I_{OH} = -2\text{mA}$ ; $V_{DD} = 3.0\text{V}$ High Output Drive disabled.
$V_{OL2}$	Low Level Output Voltage				–	–	0.6	V	$I_{OL} = 20\text{mA}$ ; $V_{DD} = 3.3\text{V}$ High Output Drive enabled.
$V_{OH2}$	High Level Output Voltage				2.4	–	–	V	$I_{OH} = -20\text{mA}$ ; $V_{DD} = 3.3\text{V}$ High Output Drive enabled.
$I_{IL}$	Input Leakage Current				–5	–	+5	$\mu\text{A}$	$V_{DD} = 3.6\text{V}$ ; $V_{IN} = V_{DD}$ or $V_{SS}$ <sup>1</sup>
$I_{TL}$	Tristate Leakage Current				–5	–	+5	$\mu\text{A}$	$V_{DD} = 3.6\text{V}$

**Notes:**

1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.
3. See Figure 31 for HALT Mode current.

## General Purpose I/O Port Input Data Sample Timing

Figure 33 displays timing of the GPIO port input sampling. The input value on a GPIO port pin is sampled on the rising edge of the system clock. The port value is available to the eZ8 CPU on the second rising clock edge following the change of the port value.

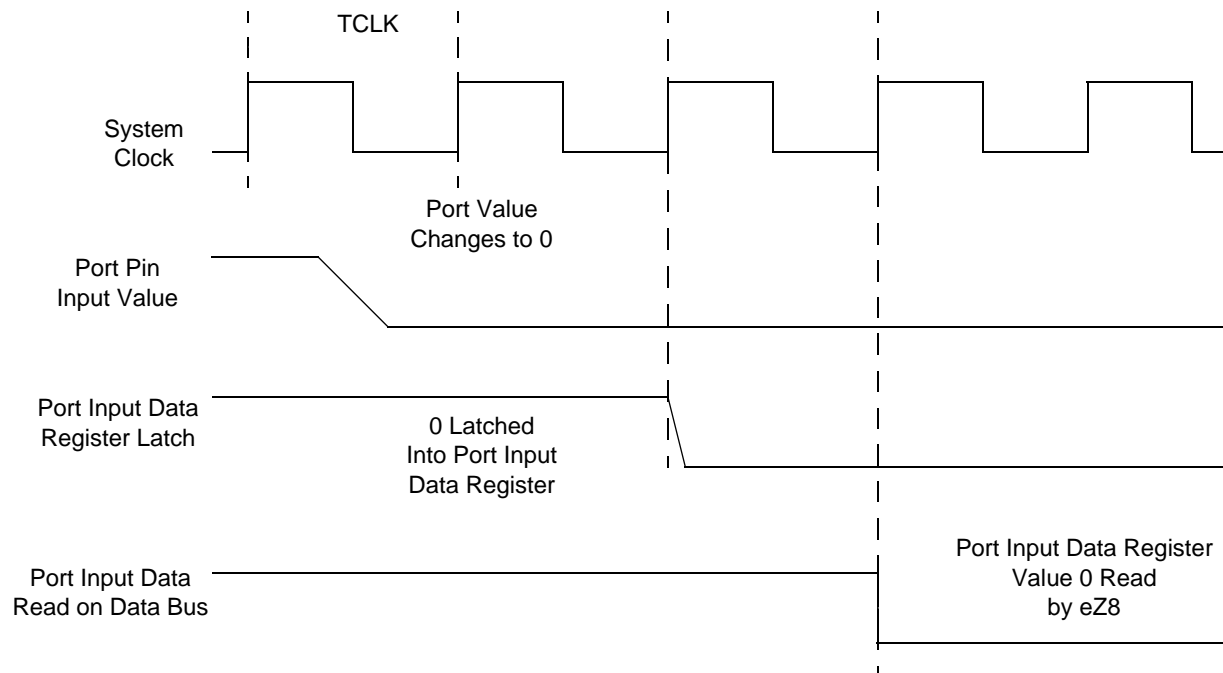


Figure 33. Port Input Sample Timing

Table 124. GPIO Port Input Timing

Parameter	Abbreviation	Delay (ns)	
		Minimum	Maximum
$T_{S\_PORT}$	Port Input Transition to $X_{IN}$ Rise Setup Time (not pictured)	5	–
$T_{H\_PORT}$	$X_{IN}$ Rise to Port Input Transition Hold Time (not pictured)	0	–
$T_{SMR}$	GPIO port pin pulse width to ensure Stop Mode Recovery (for GPIO port pins enabled as SMR sources)	1 $\mu$ s	

- reload high and low byte registers 85
- timer control register definitions 83
- timer output signal operation 82
- timers 0-3
  - control registers 87, 88
  - high and low byte registers 83, 86
- TM 167
- TMX 167
- TRAP 169

## **V**

- vector 165
- voltage brown-out reset (VBR) 24
- voltage measurement timing diagram 100

## **W**

- watch-dog timer
  - approximate time-out delay 92
  - approximate time-out delays 92, 106, 134, 151, 161
  - CNTL 24
  - control register 95, 154
  - electrical characteristics and timing 194
  - interrupt in normal operation 93
  - interrupt in stop mode 93
  - operation 92, 106, 134, 151, 161
  - refresh 93
  - reload unlock sequence 94
  - reload upper, high and low registers 96
  - reset 25
  - reset in normal operation 94
  - reset in Stop mode 94
  - time-out response 93
- watchdog timer
  - refresh 168
- WDTCTL register 29, 95, 107, 154, 217, 218, 226
- WDTH register 96, 227
- WDTL register 97, 227
- working register 164
- working register pair 165
- WTDU register 96, 227

## **X**

- X 165
- XOR 169
- XORX 169

## **Z**

- Z8 Encore!
  - block diagram 3
  - features 1
  - part selection guide 2