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Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	25
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.173", 4.40mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f1233hj020sg

Revision History

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

Date	Revision Level	Chapter/Section	Description	Page No.
Dec 2012	13	GPIO	Modified GPIO Port D0 language in Shared Reset Pin section and Port Alternate Function Mapping table.	<u>35</u> , <u>36</u>
Sep 2011	12	LED Drive Enable Register	Clarified statement surrounding the Alternate Function Register as it relates to the LED function; revised Sector Based Flash Protection description; revised Packaging chapter.	<u>51</u> , <u>115</u> , <u>199</u>
Dec 2007	11	n/a	Updated all instances of <i>Z8 Encore! XP F0830</i> to <i>Z8 Encore! F0830</i> .	All
Nov 2007	10	DC Characteristics, On-Chip Peripheral AC and DC Electrical Characteristics	Updated Tables 116 and 122.	<u>185</u> , <u>193</u>
Sep 2007	09	Timers, PWM SINGLE OUTPUT Mode, PWM DUAL OUTPUT Mode, Analog-to-Digital Converter, Reference Buffer.	Updated Figures 2 and 4, Table 4.	<u>8</u> , <u>9</u> , <u>11</u> , <u>68</u> , <u>74</u> , <u>75</u> , <u>98</u> , <u>101</u>
Apr 2007	08	Optimizing NVDS Memory Usage for Execution Speed, On-Chip Peripheral AC and DC Electrical Characteristics	Added a note under Table 93 in Nonvolatile Data Storage chapter. Updated Table 121 and Table 122 in Electrical Characteristics chapter. Other style updates.	<u>137</u> , <u>193</u> , <u>193</u>
Dec 2006	07	General Purpose Input/Output	Added PD0 in Table 16.	<u>38</u>
		Overview, Interrupt Controller	Changed the number of interrupts to 17.	<u>1.5</u> , <u>53</u>
		Nonvolatile Data Storage	Updated chapter.	<u>136</u>
		Oscillator Control Register Definitions, AC Characteristics, On-Chip Peripheral AC and DC Electrical Characteristics	Updated Tables 117 and 122. Added Figure 24.	<u>156</u> , <u>189</u> , <u>193</u>
		Ordering Information	Updated Part Number Suffix Designations.	<u>205</u>
		n/a	Removed <i>Preliminary</i> stamp from footer.	All

Electrical Characteristics	184
Absolute Maximum Ratings	184
DC Characteristics	185
AC Characteristics	189
On-Chip Peripheral AC and DC Electrical Characteristics	190
General Purpose I/O Port Input Data Sample Timing	195
General Purpose I/O Port Output Timing	196
On-Chip Debugger Timing	197
Packaging	199
Ordering Information	200
Part Number Suffix Designations	205
Appendix A. Register Tables	208
General Purpose RAM	208
Timer 0	208
Analog-to-Digital Converter	213
Low Power Control	216
LED Controller	216
Oscillator Control	217
Comparator 0	218
Interrupt Controller	218
GPIO Port A	222
Watchdog Timer	226
Trim Bit Control	228
Flash Memory Controller	228
Index	231
Customer Support	239

List of Figures

Figure 1.	Z8 Encore! F0830 Series Block Diagram	3
Figure 2.	Z8F0830 Series in 20-Pin SOIC, SSOP, PDIP Package	8
Figure 3.	Z8F0830 Series in 28-Pin SOIC, SSOP, PDIP Package	8
Figure 4.	Z8F0830 Series in 20-Pin QFN Package	9
Figure 5.	Z8F0830 Series in 28-Pin QFN Package	10
Figure 6.	Power-On Reset Operation	24
Figure 7.	Voltage Brown-Out Reset Operation	25
Figure 8.	GPIO Port Pin Block Diagram	34
Figure 9.	Interrupt Controller Block Diagram	55
Figure 10.	Timer Block Diagram	69
Figure 11.	Analog-to-Digital Converter Block Diagram	99
Figure 12.	ADC Timing Diagram	100
Figure 13.	ADC Convert Timing	100
Figure 14.	1K Flash with NVDS	108
Figure 15.	2K Flash with NVDS	109
Figure 16.	4K Flash with NVDS	109
Figure 17.	8K Flash with NVDS	110
Figure 18.	12K Flash without NVDS	111
Figure 19.	Flash Controller Operation Flow Chart	113
Figure 20.	On-Chip Debugger Block Diagram	139
Figure 21.	Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #1 of 2	140
Figure 22.	Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, #2 of 2	141
Figure 23.	OCD Data Format	142
Figure 24.	Oscillator Control Clock Switching Flow Chart	156
Figure 25.	Recommended 20MHz Crystal Oscillator Configuration	158
Figure 26.	Connecting the On-Chip Oscillator to an External RC Network	159

Table 29.	Port A–C Input Data Registers (PxIN)	49
Table 30.	Port A–D Output Data Register (PxOUT)	50
Table 31.	LED Drive Enable (LEDEN)	51
Table 32.	LED Drive Level High Register (LEDLVLH)	51
Table 33.	LED Drive Level Low Register (LEDLVLL)	52
Table 34.	Trap and Interrupt Vectors in Order of Priority	54
Table 35.	Interrupt Request 0 Register (IRQ0)	58
Table 36.	Interrupt Request 1 Register (IRQ1)	59
Table 37.	Interrupt Request 2 Register (IRQ2)	60
Table 38.	IRQ0 Enable and Priority Encoding	60
Table 39.	IRQ0 Enable Low Bit Register (IRQ0ENL)	61
Table 40.	IRQ0 Enable High Bit Register (IRQ0ENH)	61
Table 41.	IRQ1 Enable and Priority Encoding	62
Table 42.	IRQ1 Enable High Bit Register (IRQ1ENH)	62
Table 43.	IRQ2 Enable and Priority Encoding	63
Table 44.	IRQ1 Enable Low Bit Register (IRQ1ENL)	63
Table 45.	IRQ2 Enable Low Bit Register (IRQ2ENL)	64
Table 46.	IRQ2 Enable High Bit Register (IRQ2ENH)	64
Table 47.	Interrupt Edge Select Register (IRQES)	65
Table 48.	Shared Interrupt Select Register (IRQSS)	66
Table 49.	Interrupt Control Register (IRQCTL)	67
Table 50.	Timer 0–1 High Byte Register (TxH)	83
Table 51.	Timer 0–1 Low Byte Register (TxL)	83
Table 52.	Timer 0–1 Reload High Byte Register (TxRH)	85
Table 53.	Timer 0–1 Reload Low Byte Register (TxRL)	85
Table 54.	Timer 0–1 PWM High Byte Register (TxPWMH)	86
Table 55.	Timer 0–1 PWM Low Byte Register (TxPWML)	86
Table 56.	Timer 0–1 Control Register 0 (TxCTL0)	87
Table 57.	Timer 0–1 Control Register 1 (TxCTL1)	88
Table 58.	Watchdog Timer Approximate Time-Out Delays	92

Table 149. ADC Sample Settling Time (ADCSST)	215
Table 150. ADC Sample Time (ADCST)	215
Table 151. Power Control Register 0 (PWRCTL0)	216
Table 152. LED Drive Enable (LEDEN)	216
Table 153. LED Drive Level High Register (LEDLVLH)	217
Table 154. LED Drive Level Low Register (LEDLVLL)	217
Table 155. Oscillator Control Register (OSCCTL)	217
Table 156. Comparator Control Register (CMP0)	218
Table 157. Interrupt Request 0 Register (IRQ0)	218
Table 158. IRQ0 Enable High Bit Register (IRQ0ENH)	219
Table 159. IRQ0 Enable Low Bit Register (IRQ0ENL)	219
Table 160. Interrupt Request 1 Register (IRQ1)	219
Table 161. IRQ1 Enable High Bit Register (IRQ1ENH)	219
Table 162. IRQ1 Enable Low Bit Register (IRQ1ENL)	220
Table 163. Interrupt Request 2 Register (IRQ2)	220
Table 164. IRQ2 Enable High Bit Register (IRQ2ENH)	220
Table 165. IRQ2 Enable Low Bit Register (IRQ2ENL)	220
Table 166. Interrupt Edge Select Register (IRQES)	221
Table 167. Shared Interrupt Select Register (IRQSS)	221
Table 168. Interrupt Control Register (IRQCTL)	221
Table 169. Port A GPIO Address Register (PAADDR)	222
Table 170. Port A Control Registers (PACTL)	222
Table 171. Port A Input Data Registers (PAIN)	222
Table 172. Port A Output Data Register (PAOUT)	223
Table 173. Port B GPIO Address Register (PBADDR)	223
Table 174. Port B Control Registers (PBCTL)	223
Table 175. Port B Input Data Registers (PBIN)	223
Table 176. Port B Output Data Register (PBOUT)	224
Table 177. Port C GPIO Address Register (PCADDR)	224
Table 178. Port C Control Registers (PCCTL)	224

Part Selection Guide

Table 1 lists the basic features available for each device within the Z8 Encore! F0830 Series product line. See the [Ordering Information](#) chapter on page 200 for details.

Table 1. Z8 Encore! F0830 Series Family Part Selection Guide

Part Number	Flash (KB)	RAM (B)	NVDS (64B)	ADC
Z8F1232	12	256	No	Yes
Z8F1233	12	256	No	No
Z8F0830	8	256	Yes	Yes
Z8F0831	8	256	Yes	No
Z8F0430	4	256	Yes	Yes
Z8F0431	4	256	Yes	No
Z8F0230	2	256	Yes	Yes
Z8F0231	2	256	Yes	No
Z8F0130	1	256	Yes	Yes
Z8F0131	1	256	Yes	No

Table 16. Port Alternate Function Mapping (Continued)

Port	Pin	Mnemonic	Alternate Function Description	Alternate Function Set Register AFS1
Port C³	PC0	Reserved		AFS1[0]: 0
		ANA4/CINP	ADC or comparator input	AFS1[0]: 1
	PC1	Reserved		AFS1[1]: 0
		ANA5/CINN	ADC or comparator input	AFS1[1]: 1
	PC2	Reserved		AFS1[2]: 0
		ANA6	ADC analog input	AFS1[2]: 1
	PC3	COUT	Comparator output	AFS1[3]: 0
		Reserved		AFS1[3]: 1
	PC4	Reserved		AFS1[4]: 0
				AFS1[4]: 1
	PC5	Reserved		AFS1[5]: 0
				AFS1[5]: 1
	PC6	Reserved		AFS1[6]: 0
				AFS1[6]: 1
	PC7	Reserved		AFS1[7]: 0
				AFS1[7]: 1
Port D¹	PD0	RESET	Default to be Reset function	N/A

Notes:

1. Because there is only a single alternate function for each Port A and Port D (PD0) pin, the Alternate Function Set registers are not implemented for Port A and Port D (PD0). Enabling alternate function selections (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) automatically enables the associated alternate function.
2. Because there are at most two choices of alternate functions for any Port B pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) must also be enabled.
3. Because there are at most two choices of alternate functions for any Port C pin, the AFS2 Alternate Function Set Register is implemented but is not used to select the function. Additionally, alternate function selection (as described in the [Port A–D Alternate Function Subregisters](#) section on page 42) must also be enabled.

Architecture

Figure 9 displays the Interrupt Controller block diagram.

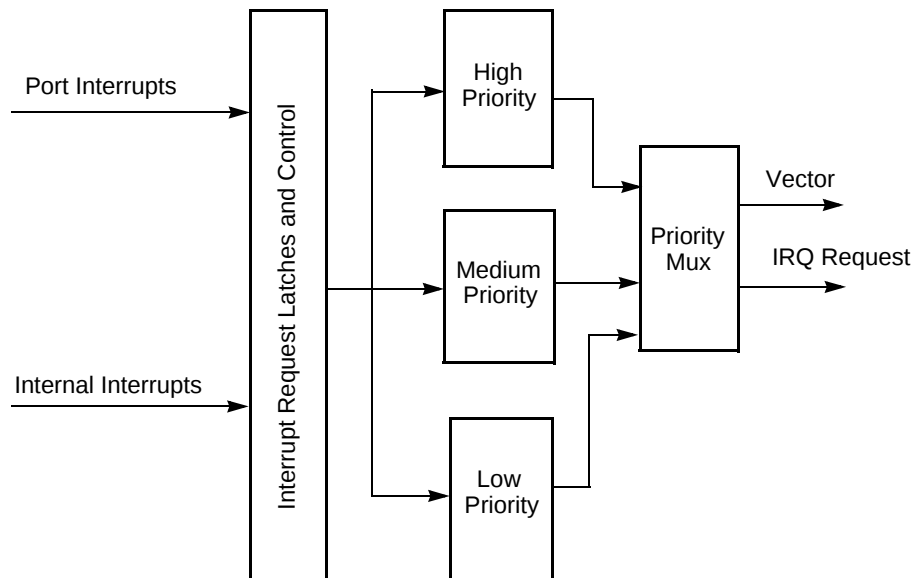


Figure 9. Interrupt Controller Block Diagram

Operation

This section describes the operational aspects of the following functions.

Master Interrupt Enable: see page 55

Interrupt Vectors and Priority: see page 56

Interrupt Assertion: see page 56

Software Interrupt Assertion: see page 57

Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control Register globally enables and disables the interrupts.

Interrupts are globally enabled by any of the following actions:

- Execution of an EI (enable interrupt) instruction
- Execution of an IRET (return from interrupt) instruction

Interrupt Request 1 Register

The Interrupt Request 1 (IRQ1) Register, shown in Table 36, stores interrupt requests for both vectored and polled interrupts. When a request is sent to the Interrupt Controller, the corresponding bit in the IRQ1 Register becomes 1. If interrupts are globally enabled (vectored interrupts), the Interrupt Controller passes an interrupt request to the eZ8 CPU. If interrupts are globally disabled (polled interrupts), the eZ8 CPU can read the Interrupt Request 1 Register to determine if any interrupt requests are pending.

Table 36. Interrupt Request 1 Register (IRQ1)

Bit	7	6	5	4	3	2	1	0
Field	PA7I	PA6CI	PA5I	PA4I	PA3I	PA2I	PA1I	PA0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC3H							

Bit	Description
[7] PA7I	Port A7 0 = No interrupt request is pending for GPIO Port A. 1 = An interrupt request from GPIO Port A.
[6] PA6CI	Port A6 or Comparator Interrupt Request 0 = No interrupt request is pending for GPIO Port A or comparator. 1 = An interrupt request from GPIO Port A or comparator.
[5] PAxI	Port A Pin x Interrupt Request 0 = No interrupt request is pending for GPIO Port A pin x. 1 = An interrupt request from GPIO Port A pin x is awaiting service.
Note: x indicates the specific GPIO port pin number (5–0).	

IRQ1 Enable High and Low Bit Registers

Table 41 describes the priority control for IRQ1. The IRQ1 Enable High and Low Bit registers, shown in Tables 42 and 43, form a priority-encoded enabling service for interrupts in the Interrupt Request 1 Register. Priority is generated by setting the bits in each register.

Table 41. IRQ1 Enable and Priority Encoding

IRQ1ENH[x]	IRQ1ENL[x]	Priority	Description
0	0	Disabled	Disabled
0	1	Level 1	Low
1	0	Level 2	Nominal
1	1	Level 3	High

Note: x indicates register bits in the address range 7–0.

Table 42. IRQ1 Enable High Bit Register (IRQ1ENH)

Bit	7	6	5	4	3	2	1	0
Field	PA7ENH	PA6CENH	PA5ENH	PA4ENH	PA3ENH	PA2ENH	PA1ENH	PA0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC4H							

Bit	Description
[7] PA7ENH	Port A Bit[7] Interrupt Request Enable High Bit
[6] PA6CENH	Port A Bit[7] or Comparator Interrupt Request Enable High Bit
[5:0] PAxENH	Port A Bit[x] Interrupt Request Enable High Bit See the interrupt port select register for selection of either Port A or Port D as the interrupt source.

Note: x indicates register bits in the address range 5–0.

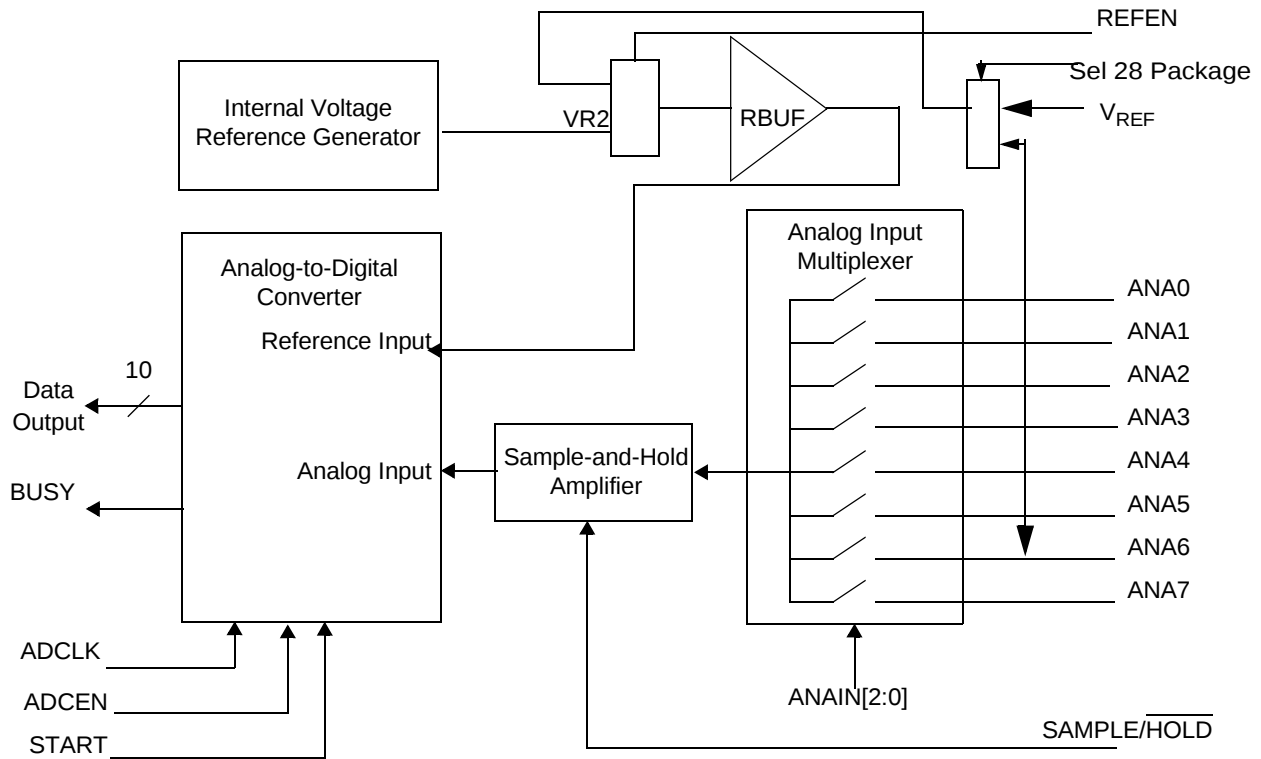


Figure 11. Analog-to-Digital Converter Block Diagram

Operation

The ADC converts the analog input, ANA_X , to a 10-bit digital representation. The equation for calculating the digital value is represented by:

$$ADCOutput = 1024 \times (ANA_X \div V_{REF})$$

Assuming zero gain and offset errors, any voltage outside the ADC input limits of AV_{SS} and V_{REF} returns all 0s or 1s, respectively. A new conversion can be initiated by a software to the ADC Control Register's start bit.

Initiating a new conversion, stops any conversion currently in progress and begins a new conversion. To avoid disrupting a conversion already in progress, the START bit can be read to determine ADC operation status (busy or available).

Flash Memory

The products in the Z8 Encore! F0830 Series features either 1KB (1024 bytes with NVDS), 2KB (2048 bytes with NVDS), 4KB (4096 bytes with NVDS), 8KB (8192 bytes with NVDS) or 12KB (12288 bytes with no NVDS) of nonvolatile Flash memory with read/write/erase capability. Flash memory can be programmed and erased in-circuit by either user code or through the On-Chip Debugger.

The Flash memory array is arranged in pages with 512 bytes per page. The 512-byte page is the minimum Flash block size that can be erased. Each page is divided into eight rows of 64 bytes.

For program/data protection, Flash memory is also divided into sectors. In the Z8 Encore! F0830 Series, each sector maps to one page (for 1KB, 2KB and 4KB devices), two pages (8KB device) or three pages (12KB device).

The first two bytes of Flash program memory is used as Flash option bits. For more information, see the [Flash Option Bits](#) chapter on page 124.

Table 69 lists the Flash memory configuration for each device in the Z8 Encore! F0830 Series. Figures 14 through 18 display the memory arrangements for each Flash memory size.

Table 69. Z8 Encore! F0830 Series Flash Memory Configuration

Part Number	Flash Size KB (Bytes)	Flash Pages	Program Memory Addresses	Flash Sector Size (bytes)
Z8F123x	12 (12,288)	24	0000H–2FFFH	1536
Z8F083x	8 (8196)	16	0000H–1FFFH	1024
Z8F043x	4 (4096)	8	0000H–0FFFH	512
Z8F023x	2 (2048)	4	0000H–07FFH	512
Z8F013x	1 (1024)	2	0000H–03FFH	512

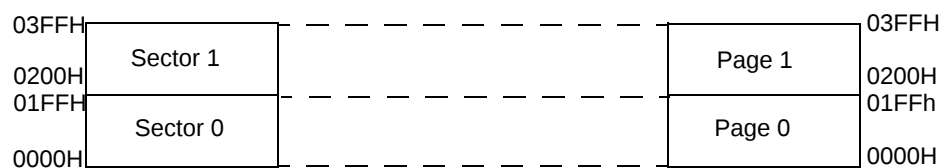


Figure 14. 1K Flash with NVDS

Internal Precision Oscillator

The Internal Precision Oscillator (IPO) is designed for use without external components. The user can either manually trim the oscillator for a nonstandard frequency or use the automatic factory-trimmed version to achieve a 5.53MHz frequency with $\pm 4\%$ accuracy and 45%~55% duty cycle over the operating temperature and supply voltage of the device. The maximum start-up time of the IPO is 25 μ s. IPO features include:

- On-chip RC oscillator that does not require external components
- Output frequency of either 5.53MHz or 32.8kHz (contains both a FAST and a SLOW mode)
- Trimming possible through Flash option bits, with user override
- Elimination of crystals or ceramic resonators in applications where high timing accuracy is not required

Operation

The internal oscillator is an RC relaxation oscillator with a minimized sensitivity to power supply variations. By using ratio-tracking thresholds, the effect of power supply voltage is cancelled out. The dominant source of oscillator error is the absolute variance of chip-level fabricated components, such as capacitors. An 8-bit trimming register, incorporated into the design, compensates for absolute variation of oscillator frequency. Once trimmed, the oscillator frequency is stable and does not require subsequent calibration. Trimming was performed during manufacturing and is not necessary for the user to repeat unless a frequency other than 5.53MHz (FAST mode) or 32.8kHz (SLOW mode) is required.

► **Note:** The user can power down the IPO block for minimum system power.

By default, the oscillator is configured through the Flash option bits. However, the user code can override these trim values, as described in the [Trim Bit Address Space](#) section on page 129.

Select one of two frequencies for the oscillator: 5.53MHz or 32.8 kHz, using the OSCSEL bits described in the [Oscillator Control](#) chapter on page 151.

eZ8 CPU Instruction Set

This chapter describes the following features of the eZ8 CPU instruction set:

Assembly Language Programming Introduction: see page 162

Assembly Language Syntax: see page 163

eZ8 CPU Instruction Notation: see page 164

eZ8 CPU Instruction Classes: see page 166

eZ8 CPU Instruction Summary: see page 171

Assembly Language Programming Introduction

The eZ8 CPU assembly language provides a means for writing an application program without concern for actual memory addresses or machine instruction formats. A program written in assembly language is called a source program. Assembly language allows the use of symbolic addresses to identify memory locations. It also allows mnemonic codes (op codes and operands) to represent the instructions themselves. The op codes identify the instruction while the operands represent memory locations, registers or immediate data values.

Each assembly language program consists of a series of symbolic commands called statements. Each statement contains labels, operations, operands and comments.

Labels can be assigned to a particular instruction step in a source program. The label identifies that step in the program as an entry point for use by other instructions.

The assembly language also includes assembler directives that supplement the machine instruction. The assembler directives, or pseudo-ops, are not translated into a machine instruction. Rather, these pseudo-ops are interpreted as directives that control or assist the assembly process.

The source program is processed (assembled) by the assembler to obtain a machine language program called the object code. The object code is executed by the eZ8 CPU. An example segment of an assembly language program is provided in the following example.

Op Code Maps

A description of the opcode map data and the abbreviations are provided in Figure 28. Table 114 on page 181 lists opcode map abbreviations.

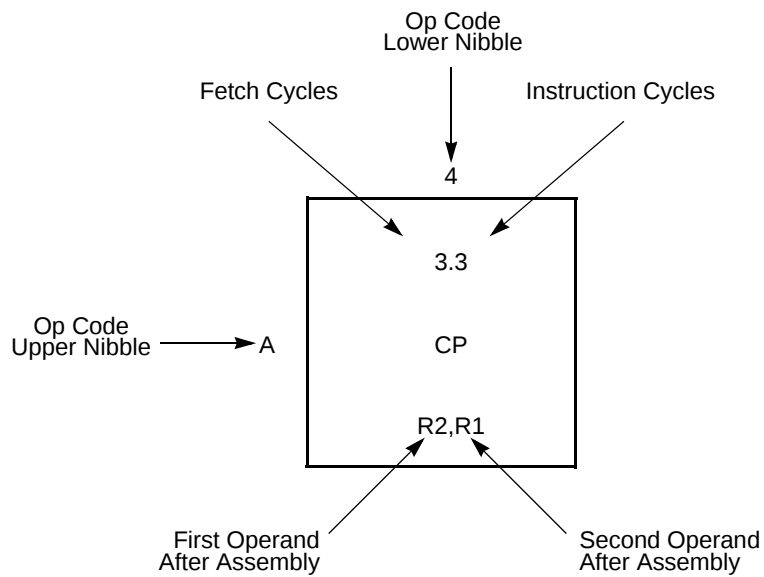


Figure 28. Op Code Map Cell Description

Figures 29 and 30 provide information about each of the eZ8 CPU instructions.

		Lower Nibble (Hex)										A	B	C	D	E	F	
		0	1	2	3	4	5	6	7	8	9							
Upper Nibble (Hex)	0	1.1 BRK	2.2 SRP IM	2.3 ADD r1,r2	2.4 ADD r1,lr2	3.3 ADD R2,R1	3.4 ADD IR2,R1	3.3 ADD R1,IM	3.4 ADD IR1,IM	4.3 ADDX ER2,ER1	4.3 ADDX IM,ER1	2.3 DJNZ r1,X	2.2 JR cc,X	2.2 LD r1,IM	3.2 JP cc,DA	1.2 INC r1	1.2 NOP	
	1	2.2 RLC R1	2.3 RLC IR1	2.3 ADC r1,r2	2.4 ADC r1,lr2	3.3 ADC R2,R1	3.4 ADC IR2,R1	3.3 ADC R1,IM	3.4 ADC IR1,IM	4.3 ADCX ER2,ER1	4.3 ADCX IM,ER1							See 2nd Op Code Map
	2	2.2 INC R1	2.3 INC IR1	2.3 SUB r1,r2	2.4 SUB r1,lr2	3.3 SUB R2,R1	3.4 SUB IR2,R1	3.3 SUB R1,IM	3.4 SUB IR1,IM	4.3 SUBX ER2,ER1	4.3 SUBX IM,ER1							
	3	2.2 DEC R1	2.3 DEC IR1	2.3 SBC r1,r2	2.4 SBC r1,lr2	3.3 SBC R2,R1	3.4 SBC IR2,R1	3.3 SBC R1,IM	3.4 SBC IR1,IM	4.3 SBCX ER2,ER1	4.3 SBCX IM,ER1							
	4	2.2 DA R1	2.3 DA IR1	2.3 OR r1,r2	2.4 OR r1,lr2	3.3 OR R2,R1	3.4 OR IR2,R1	3.3 OR R1,IM	3.4 OR IR1,IM	4.3 ORX ER2,ER1	4.3 ORX IM,ER1							
	5	2.2 POP R1	2.3 POP IR1	2.3 AND r1,r2	2.4 AND r1,lr2	3.3 AND R2,R1	3.4 AND IR2,R1	3.3 AND R1,IM	3.4 AND IR1,IM	4.3 ANDX ER2,ER1	4.3 ANDX IM,ER1							1.2 WDT
	6	2.2 COM R1	2.3 COM IR1	2.3 TCM r1,r2	2.4 TCM r1,lr2	3.3 TCM R2,R1	3.4 TCM IR2,R1	3.3 TCM R1,IM	3.4 TCM IR1,IM	4.3 TCMX ER2,ER1	4.3 TCMX IM,ER1							1.2 STOP
	7	2.2 PUSH R2	2.3 PUSH IR2	2.3 TM r1,r2	2.4 TM r1,lr2	3.3 TM R2,R1	3.4 TM IR2,R1	3.3 TM R1,IM	3.4 TM IR1,IM	4.3 TMX ER2,ER1	4.3 TMX IM,ER1							1.2 HALT
	8	2.5 DECW RR1	2.6 DECW IRR1	2.5 LDE r1,lr2	2.9 LDEI lr1,lr2	3.2 LDX r1,ER2	3.3 LDX lr1,ER2	3.4 LDX IRR2,R1	3.5 LDX IRR2,IR1	3.4 LDX r1,r2,X	3.4 LDX rr1,r2,X							1.2 DI
	9	2.2 RL R1	2.3 RL IR1	2.5 LDE r2,lr1	2.9 LDEI lr2,lr1	3.2 LDX r2,ER1	3.3 LDX lr2,ER1	3.4 LDX R2,IRR1	3.5 LDX IR2,IRR1	3.3 LEA r1,r2,X	3.5 LEA rr1,r2,X							1.2 EI
	A	2.5 INCW RR1	2.6 INCW IRR1	2.3 CP r1,r2	2.4 CP r1,lr2	3.3 CP R2,R1	3.4 CP IR2,R1	3.3 CP R1,IM	3.4 CP IR1,IM	4.3 CPX ER2,ER1	4.3 CPX IM,ER1							1.4 RET
	B	2.2 CLR R1	2.3 CLR IR1	2.3 XOR r1,r2	2.4 XOR r1,lr2	3.3 XOR R2,R1	3.4 XOR IR2,R1	3.3 XOR R1,IM	3.4 XOR IR1,IM	4.3 XORX ER2,ER1	4.3 XORX IM,ER1							1.5 IRET
	C	2.2 RRC R1	2.3 RRC IR1	2.5 LDC r1,lr2	2.9 LDCI lr1,lr2	2.3 JP IRR1	2.9 LDC lr1,lr2		3.4 LD r1,r2,X	3.2 PUSHX ER2								1.2 RCF
	D	2.2 SRA R1	2.3 SRA IR1	2.5 LDC r2,lr1	2.9 LDCI lr2,lr1	2.6 CALL IRR1	2.2 BSWAP R1	3.3 CALL DA	3.4 LD r2,r1,X	3.2 POPX ER1								1.2 SCF
	E	2.2 RR R1	2.3 RR IR1	2.2 BIT p,b,r1	2.3 LD r1,lr2	3.2 LD R2,R1	3.3 LD IR2,R1	3.2 LD R1,IM	3.3 LD IR1,IM	4.2 LDX ER2,ER1	4.2 LDX IM,ER1							1.2 CCF
	F	2.2 SWAP R1	2.3 SWAP IR1	2.6 TRAP Vector	2.3 LD lr1,r2	2.8 MULT RR1	3.3 LD R2,IR1	3.3 BTJ p,b,r1,X	3.4 BTJ p,b,lr1,X									

Figure 29. First Op Code Map

Ordering Information

Order your F0830 Series products from Zilog using the part numbers shown in Table 128. For more information about ordering, please consult your local Zilog sales office. The [Sales Location](#) page on the Zilog website lists all regional offices.

Table 128. Z8 Encore! XP F0830 Series Ordering Matrix

Part Number	Flash	RAM	NVDS	ADC Channels	Description
Z8 Encore! F0830 Series MCUs with 12KB Flash					
Standard Temperature: 0°C to 70°C					
Z8F1232SH020SG	12KB	256	No	7	SOIC 20-pin
Z8F1232HH020SG	12KB	256	No	7	SSOP 20-pin
Z8F1232PH020SG	12KB	256	No	7	PDIP 20-pin
Z8F1232QH020SG	12KB	256	No	7	QFN 20-pin
Z8F1233SH020SG	12KB	256	No	0	SOIC 20-pin
Z8F1233HH020SG	12KB	256	No	0	SSOP 20-pin
Z8F1233PH020SG	12KB	256	No	0	PDIP 20-pin
Z8F1233QH020SG	12KB	256	No	0	QFN 20-pin
Z8F1232SJ020SG	12KB	256	No	8	SOIC 28-pin
Z8F1232HJ020SG	12KB	256	No	8	SSOP 28-pin
Z8F1232PJ020SG	12KB	256	No	8	PDIP 28-pin
Z8F1232QJ020SG	12KB	256	No	8	QFN 28-pin
Z8F1233SJ020SG	12KB	256	No	0	SOIC 28-pin
Z8F1233HJ020SG	12KB	256	No	0	SSOP 28-pin
Z8F1233PJ020SG	12KB	256	No	0	PDIP 28-pin
Z8F1233QJ020SG	12KB	256	No	0	QFN 28-pin
Extended Temperature: –40°C to 105°C					
Z8F1232SH020EG	12KB	256	No	7	SOIC 20-pin
Z8F1232HH020EG	12KB	256	No	7	SSOP 20-pin
Z8F1232PH020EG	12KB	256	No	7	PDIP 20-pin
Z8F1232QH020EG	12KB	256	No	7	QFN 20-pin
Z8F1233SH020EG	12KB	256	No	0	SOIC 20-pin
Z8F1233HH020EG	12KB	256	No	0	SSOP 20-pin
Z8F1233PH020EG	12KB	256	No	0	PDIP 20-pin

Hex Address: F05

Table 135. Timer 0 PWM Low Byte Register (T0PWML)

Bit	7	6	5	4	3	2	1	0
Field	PWML							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F05H							

Hex Address: F06

Table 136. Timer 0 Control Register 0 (T0CTL0)

Bit	7	6	5	4	3	2	1	0
Field	TMODEHI	TICONFIG		Reserved	PWMD			INPCAP
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F06H							

Hex Address: F07

Table 137. Timer 0 Control Register 1 (T0CTL1)

Bit	7	6	5	4	3	2	1	0
Field	TEN	TPOL	PRES			TMODE		
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F07H							

Hex Address: F08

Table 138. Timer 1 High Byte Register (T1H)

Bit	7	6	5	4	3	2	1	0
Field	TH							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F08H							

Hex Address: FC5

Table 162. IRQ1 Enable Low Bit Register (IRQ1ENL)

Bit	7	6	5	4	3	2	1	0
Field	PA7ENL	PA6CENL	PA5ENL	PA4ENL	PA3ENL	PA2ENL	PA1ENL	PA0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC5H							

Hex Address: FC6

Table 163. Interrupt Request 2 Register (IRQ2)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				PC3I	PC2I	PC1I	PC0I
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC6H							

Hex Address: FC7

Table 164. IRQ2 Enable High Bit Register (IRQ2ENH)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENH	C2ENH	C1ENH	C0ENH
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC7H							

Hex Address: FC8

Table 165. IRQ2 Enable Low Bit Register (IRQ2ENL)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				C3ENL	C2ENL	C1ENL	C0ENL
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FC8H							

JP 169
 LD 168
 LDC 168
 LDCI 167, 168
 LDE 168
 LDEI 167
 LDX 168
 LEA 168
 load 168
 logical 169
 MULT 167
 NOP 168
 OR 169
 ORX 169
 POP 168
 POPX 168
 program control 169
 PUSH 168
 PUSHX 168
 RCF 167, 168
 RET 169
 RL 169
 RLC 169
 rotate and shift 169
 RR 170
 RRC 170
 SBC 167
 SCF 167, 168
 SRA 170
 SRL 170
 SRP 168
 STOP 168
 SUB 167
 SUBX 167
 SWAP 170
 TCM 167
 TCMX 167
 TM 167
 TMX 167
 TRAP 169
 watch-dog timer refresh 168
 XOR 169
 XORX 169
 instructions, eZ8 classes of 166

interrupt control register 67
 interrupt controller 53
 architecture 53
 interrupt assertion types 56
 interrupt vectors and priority 56
 operation 55
 register definitions 57
 software interrupt assertion 57
 interrupt edge select register 65
 interrupt request 0 register 58
 interrupt request 1 register 59
 interrupt request 2 register 60
 interrupt return 169
 interrupt vector listing 53
 IR 164
 Ir 164
 IRET 169
 IRQ0 enable high and low bit registers 60
 IRQ1 enable high and low bit registers 62
 IRQ2 enable high and low bit registers 63
 IRR 164
 Irr 164

J

JP 169
 jump, conditional, relative, and relative conditional 169

L

LD 168
 LDC 168
 LDCI 167, 168
 LDE 168
 LDEI 167, 168
 LDX 168
 LEA 168
 load 168
 load constant 167
 load constant to/from program memory 168
 load constant with auto-increment addresses 168
 load effective address 168
 load external data 168