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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	17
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f1233ph020sg

Part Selection Guide

Table 1 lists the basic features available for each device within the Z8 Encore! F0830 Series product line. See the <u>Ordering Information</u> chapter on page 200 for details.

Table 1. Z8 Encore! F0830 Series Family Part Selection Guide

Part Number	Flash (KB)	RAM (B)	NVDS (64B)	ADC
Z8F1232	12	256	No	Yes
Z8F1233	12	256	No	No
Z8F0830	8	256	Yes	Yes
Z8F0831	8	256	Yes	No
Z8F0430	4	256	Yes	Yes
Z8F0431	4	256	Yes	No
Z8F0230	2	256	Yes	Yes
Z8F0231	2	256	Yes	No
Z8F0130	1	256	Yes	Yes
Z8F0131	1	256	Yes	No
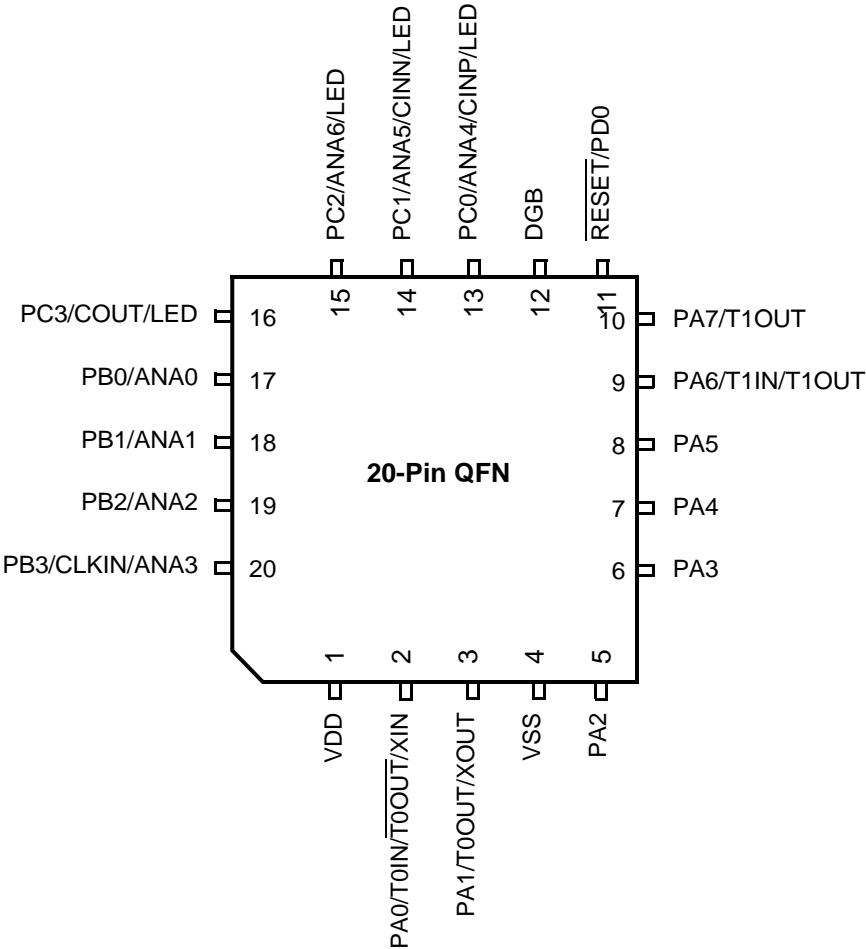
Figure 4. Z8F0830 Series in 20-Pin QFN Package

Signal Descriptions

Table 4 describes the Z8 Encore! F0830 Series signals. See the Pin Configurations section on page 7 to determine the signals available for each specific package style.

Table 4. Signal Descriptions

Signal Mnemonic	I/O	Description
General-Purpose I/O Ports A–D		
PA[7:0]	I/O	Port A. These pins are used for general purpose I/O.
PB[7:0]	I/O	Port B. These pins are used for general purpose I/O. PB6 and PB7 are available only in those devices without an ADC.
PC[7:0]	I/O	Port C. These pins are used for general purpose I/O.
PD[0]	I/O	Port D. This pin is used for general purpose output only.
Note: PB6 and PB7 are only available in 28-pin packages without ADC. In 28-pin packages with ADC, they are replaced by AV_{DD} and AV_{SS}.		
Timers		
T0OUT/T1OUT	O	Timer output 0–1. These signals are the output from the timers.
$\overline{T0OUT}/\overline{T1OUT}$	O	Timer complement output 0–1. These signals are output from the timers in PWM DUAL OUTPUT Mode.
T0IN/T1IN	I	Timer Input 0–1. These signals are used as the capture, gating and counter inputs. The T0IN signal is multiplexed T0OUT signals.
Comparator		
CINP/CINN	I	Comparator inputs. These signals are the positive and negative inputs to the comparator.
COUT	O	Comparator output. This is the output of the comparator.
Analog		
ANA[7:0]	I	Analog port. These signals are used as inputs to the analog-to-digital converter (ADC).
V_{REF}	I/O	Analog-to-digital converter reference voltage input. **Note:** When configuring ADC using external V_{REF}, PB5 is used as V_{REF} in 28-pin package.
Note: The AV_{DD} and AV_{SS} signals are available only in the 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.		

Table 8. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No.
Trim Bit Control				
FF6	Trim bit address	TRMADR	00	126
FF7	Trim data	TRMDR	XX	127
Flash Memory Controller				
FF8	Flash control	FCTL	00	119
FF8	Flash status	FSTAT	00	120
FF9	Flash page select	FPS	00	121
	Flash sector protect	FPROT	00	122
FFA	Flash programming frequency high byte	FFREQH	00	123
FFB	Flash programming frequency low byte	FFREQL	00	123
eZ8 CPU				
FFC	Flags	—	XX	Refer to the eZ8 CPU Core User Manual (UM0128)
FFD	Register pointer	RP	XX	
FFE	Stack pointer high byte	SPH	XX	
FFF	Stack pointer low byte	SPL	XX	
Note: XX = Undefined.				

Port A–D Stop Mode Recovery Source Enable Subregisters

The Port A–D Stop Mode Recovery Source Enable Subregister, shown in Table 25, is accessed through the Port A–D Control Register by writing 05H to the Port A–D Address Register. Setting the bits in the Port A–D Stop Mode Recovery Source Enable subregisters to 1 configures the specified port pins as a Stop Mode Recovery source. During STOP Mode, any logic transition on a port pin enabled as a Stop Mode Recovery source initiates a Stop Mode Recovery event.

Table 25. Port A–D Stop Mode Recovery Source Enable Subregisters (PxSMRE)

Bit	7	6	5	4	3	2	1	0
Field	PSMRE7	PSMRE6	PSMRE5	PSMRE4	PSMRE3	PSMRE2	PSMRE1	PSMRE0
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	If 05H in Port A–D Address Register, accessible through the Port A–D Control Register							

Bit	Description
[7:0] PSMREx	**Port Stop Mode Recovery Source Enable** 0 = The port pin is not configured as a Stop Mode Recovery source. Transitions on this pin during STOP Mode do not initiate Stop Mode Recovery. 1 = The port pin is configured as a Stop Mode Recovery source. Any logic transition on this pin during STOP Mode initiates Stop Mode Recovery.

Note: x indicates the specific GPIO port pin number (7–0).

LED Drive Enable Register

The LED Drive Enable Register, shown in Table 31, activates the controlled current drive. The Alternate Function Register has no control over the LED function; therefore, setting the Alternate Function Register to select the LED function is not required. LEDEN bits [7:0] correspond to Port C bits [7:0], respectively.

Table 31. LED Drive Enable (LEDEN)

Bit	7	6	5	4	3	2	1	0
Field	LEDEN[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F82H							

Bit	Description
[7:0] LEDEN	**LED Drive Enable** These bits determine which Port C pins are connected to an internal current sink. 0 = Tristate the Port C pin. 1= Connect controlled current sink to the Port C pin.

LED Drive Level High Register

The LED Drive Level High Register, shown in Table 32, contains two control bits for each Port C pin. These two bits select one of four programmable current drive levels for each Port C pin. Each pin is individually programmable.

Table 32. LED Drive Level High Register (LEDLVLH)

Bit	7	6	5	4	3	2	1	0
Field	LEDLVLH[7:0]							
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	F83H							

Bit	Description
[7:0] LEDLVLH	**LED Level High Bits** {LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin. 00 = 3mA. 01= 7mA. 10= 13mA. 11= 20mA.

PWM SINGLE OUTPUT Mode

In PWM SINGLE OUTPUT Mode, the timer outputs a pulse width modulated (PWM) output signal through a GPIO port pin. The timer input is the system clock. The timer first counts up to 16-bit PWM match value stored in the timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the timer output toggles. The timer continues counting until it reaches the reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to `0001H` and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the timer output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The timer output signal returns to a High (1) after the timer reaches the reload value and is reset to `0001H`.

If the TPOL bit in the Timer Control Register is set to 0, the timer output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The timer output signal returns to a Low (0) after the timer reaches the reload value and is reset to `0001H`.

Observe the following steps for configuring a timer for PWM SINGLE OUTPUT Mode and for initiating PWM operation:

1. Write to the Timer Control Register to:
   - Disable the timer
   - Configure the timer for PWM Mode
   - Set the prescale value
   - Set the initial logic level (High or Low) and PWM High/Low transition for the timer output alternate function

2. Write to the Timer High and Low Byte registers to set the starting count value (typically `0001H`). This value only affects the first pass in PWM Mode. After the first timer reset in PWM Mode, counting always begins at the reset value of `0001H`.

3. Write to the PWM High and Low Byte registers to set the PWM value.

4. Write to the Timer Reload High and Low Byte registers to set the reload value (PWM period). The reload value must be greater than the PWM value.

5. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.

6. Configure the associated GPIO port pin for the timer output alternate function.

7. Write to the Timer Control Register to enable the timer and initiate counting.

The PWM period is represented by the following equation:

Bit	Description
[7:0] TH, TL	**Timer High and Low Bytes** These 2 bytes, {TH[7:0], TL[7:0]}, contain the current 16-bit timer count value.

Watchdog Timer Control Register Definitions

This section defines the features of the following Watchdog Timer Control registers.

Watchdog Timer Control Register (WDTCTL): see page 95

Watchdog Timer Reload Low Byte Register (WDTL): see page 97

Watchdog Timer Reload Upper Byte Register (WDTU): see page 96

Watchdog Timer Reload High Byte Register (WDTH): see page 96

Watchdog Timer Control Register

The Watchdog Timer Control (WDTCTL) Register is a write-only control register. Writing the unlock sequence: 55H, AAH to the WDTCTL Register address unlocks the three Watchdog Timer Reload Byte registers (WDTU, WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTCTL Register address have no effect on the bits in the WDTCTL Register. The locking mechanism prevents spurious writes to the reload registers.

This register address is shared with the read-only Reset Status Register.

Table 59. Watchdog Timer Control Register (WDTCTL)

Bit	7	6	5	4	3	2	1	0
Field	WDTUNLK							
RESET	X	X	X	X	X	X	X	X
R/W	W	W	W	W	W	W	W	W
Address	FF0H							

Bit	Description
[7:0] WDTUNLK	**Watchdog Timer Unlock** The user software must write the correct unlocking sequence to this register before it is allowed to modify the contents of the Watchdog Timer Reload registers.

Sample Settling Time Register

The Sample Settling Time Register, shown in Table 66, is used to program a delay after the SAMPLE/HOLD signal is asserted and before the START signal is asserted; an ADC conversion then begins. The number of clock cycles required for settling will vary from system to system depending on the system clock period used. The system designer should program this register to contain the number of clocks required to meet a 0.5 µs minimum settling time.

Table 66. Sample Settling Time (ADCSST)

Bit	7	6	5	4	3	2	1	0
Field	Reserved				SST			
RESET	0				1	1	1	1
R/W	R				R/W			
Address	F74H							

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3:0] SST	0h–Fh = Sample settling time in number of system clock periods to meet 0.5 µs minimum.

Option Bit Types

This section describes the two types of Flash option bits offered in the F0830 Series.

User Option Bits

The user option bits are contained in the first two bytes of program memory. User access to these bits is provided because these locations contain application specific device configurations. The information contained here is lost when page 0 of program memory is erased.

Trim Option Bits

The trim option bits are contained in the information page of the Flash memory. These bits are factory programmed values required to optimize the operation of onboard analog circuitry and cannot be permanently altered by the user. Program memory can be erased without endangering these values. It is possible to alter working values of these bits by accessing the trim bit address and data registers, but these working values are lost after a power loss.

There are 32 bytes of trim data. To modify one of these values, the user code must first write a value between 00H and 1FH into the Trim Bit Address Register. The next write to the Trim Bit Data Register changes the working value of the target trim data byte.

Reading the trim data requires the user code to write a value between 00H and 1FH into the Trim Bit Address Register. The next read from the Trim Bit Data Register returns the working value of the target trim data byte.

> **Note:** The trim address range is from information address 20–3F only. The remaining information page is not accessible via the Trim Bit Address and Data registers.

During reset, the first 43 system clock cycles perform 43 Flash accesses. The six bits of the counter provide the lower six bits of the Flash memory address. All other address bits are set to 0. The option bit registers use the 6-bit address from the counter as an address and latch the data from the Flash on the positive edge of the IPO clock, allowing for a maximum of 344-bits (43 bytes) of option information to be read from Flash.

Because option information is stored in both the first two bytes of program memory and in the information area of Flash memory, the data must be placed in specific locations to be read correctly. In this case, the first two bytes at addresses 0 and 1 in program memory are read out and the remainder of the bytes are read out of the Flash information area.

Table 80. Trim Bit Data Register (TRMDR)

Bit	7	6	5	4	3	2	1	0
Field	TRMDR: Trim Bit Data
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	FF7H

Flash Option Bit Address Space

The first two bytes of Flash program memory at addresses `0000H` and `0001H` are reserved for the user-programmable Flash option bits. See Tables 81 and 82.

Table 81. Flash Option Bits at Program Memory Address 0000H

Bit	7	6	5	4	3	2	1	0
Field	WDT_RES	WDT_AO	OSC_SEL[1:0]		VBO_AO	FRP	Reserved	FWP
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Program Memory 0000H							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7] WDT_RES	**Watchdog Timer Reset** 0 = Watchdog Timer time-out generates an interrupt request. Interrupts must be globally enabled for the eZ8 CPU to acknowledge the interrupt request. 1 = Watchdog Timer time-out causes a system reset. This is the default setting for unprogrammed (erased) Flash.
[6] WDT_AO	**Watchdog Timer Always On** 0 = On application of system power, Watchdog Timer is automatically enabled. Watchdog Timer cannot be disabled. 1 = Watchdog Timer is enabled on execution of the WDT instruction. Once enabled, the Watchdog Timer can only be disabled by a reset. This is the default setting for unprogrammed (erased) Flash.
[5:4] OSC_SEL	**OSCILLATOR Mode Selection** 00 = On-chip oscillator configured for use with external RC networks (<4 MHz). 01 = Minimum power for use with very low frequency crystals (32 kHz to 1.0 MHz). 10 = Medium power for use with medium frequency crystals or ceramic resonators (0.5 MHz to 5.0 MHz). 11 = Maximum power for use with high frequency crystals (5.0 MHz to 20.0 MHz). This is the default setting for unprogrammed (erased) Flash.

Bit	Description (Continued)
[1:0] FilterSel*y*	**Filter Select** 2-bit selection for the clock filter mode. 00 = No filter. 01 = Filter low level noise on high level signal. 10 = Filter high level noise on low level signal. 11 = Filter both.

Notes: x indicates bit values 3–1; y indicates bit values 1–0.

> **Note:** The bit values used in Table 89 are set at factory and no calibration is required.

Table 90. ClkFlt Delay Control Definition

DlyCtl3, DlyCtl2, DlyCtl1	Low Noise Pulse on High Signal (ns)	High Noise Pulse on Low Signal (ns)
000	5	5
001	7	7
010	9	9
011	11	11
100	13	13
101	17	17
110	20	20
111	25	25

Note: The variation is about 30%.

Nonvolatile Data Storage

Z8 Encore! F0830 Series devices contain a Nonvolatile Data Storage (NVDS) element of up to 64 bytes (except when in Flash 12 KB mode). This type of memory can perform over 100,000 write cycles.

Operation

NVDS is implemented by special-purpose Zilog software stored in areas of program memory that are not user-accessible. These special-purpose routines use Flash memory to store the data, and incorporate a dynamic addressing scheme to maximize the write/erase endurance of the Flash.

> **Note:** The products in the Z8 Encore! F0830 Series feature multiple NVDS array sizes. See the Z8 Encore! F0830 Series Family Part Selection Guide section on page 2 for details.

NVDS Code Interface

Two routines are required to access the NVDS: a write routine and a read routine. Both of these routines are accessed with a CALL instruction to a predefined address outside of program memory that is accessible to the user. Both the NVDS address and data are single-byte values. In order to not disturb the user code, these routines save the working register set before using it so that 16 bytes of stack space are required to preserve the site. After finishing the call to these routines, the working register set of the user code is recovered.

During both read and write accesses to the NVDS, interrupt service is not disabled. Any interrupts that occur during NVDS execution must not disturb the working register and existing stack contents; otherwise, the array can become corrupted. Zilog recommends the user disable interrupts before executing NVDS operations.

Use of the NVDS requires 16 bytes of available stack space. The contents of the working register set are saved before calling NVDS read or write routines.

For correct NVDS operation, the Flash Frequency registers must be programmed based on the system clock frequency. See *the* Flash Operation Timing Using the Flash Frequency Registers *section on page 114*.

Crystal Oscillator

The products in the Z8 Encore! F0830 Series contain an on-chip crystal oscillator for use with external crystals with 32 kHz to 20 MHz frequencies. In addition, the oscillator supports external RC networks with oscillation frequencies up to 4 MHz or ceramic resonators with frequencies up to 8 MHz. The on-chip crystal oscillator can be used to generate the primary system clock for the internal eZ8 CPU and the majority of its on-chip peripherals. Alternatively, the X_{IN} input pin can also accept a CMOS-level clock input signal (32 kHz–20 MHz). If an external clock generator is used, the X_{OUT} pin must remain unconnected. The on-chip crystal oscillator also contains a clock filter function. To see the settings for this clock filter, see Table 90 on page 133. By default, however, this clock filter is disabled; therefore, no divide to the input clock (namely, the frequency of the signal on the X_{IN} input pin) can determine the frequency of the system clock when using the default settings.

▶ **Note:** Although the X_{IN} pin can be used as an input for an external clock generator, the CLKIN pin is better suited for such use. See *the* System Clock Selection *section on page 151* for more information.

Operating Modes

The Z8 Encore! F0830 Series products support the following four OSCILLATOR Modes:

- Minimum power for use with very low frequency crystals (32 kHz to 1 MHz)

- Medium power for use with medium frequency crystals or ceramic resonators (0.5 MHz to 8 MHz)

- Maximum power for use with high frequency crystals (8 MHz to 20 MHz)

- On-chip oscillator configured for use with external RC networks (<4 MHz)

The OSCILLATOR Mode is selected using user-programmable Flash option bits. See the Flash Option Bits chapter on page 124 for more information.

Crystal Oscillator Operation

The XTLDIS Flash option bit controls whether the crystal oscillator is enabled during reset. The crystal may later be disabled after reset if a new oscillator has been selected as the system clock. If the crystal is manually enabled after reset through the OSCCTL Reg-

ister, the user code must wait at least 5000 IPO cycles for the crystal to stabilize. After this period, the crystal oscillator may be selected as the system clock.

Figure 25 displays a recommended configuration for connection with an external fundamental-mode, parallel-resonant crystal operating at 20 MHz. Recommended 20 MHz crystal specifications are provided in Table 100. Resistor R_1 is optional and limits total power dissipation by the crystal. Printed circuit board layout must add no more than 4 pF of stray capacitance to either the X_{IN} or X_{OUT} pins. If oscillation does not occur, reduce the values of capacitors C_1 and C_2 to decrease loading.
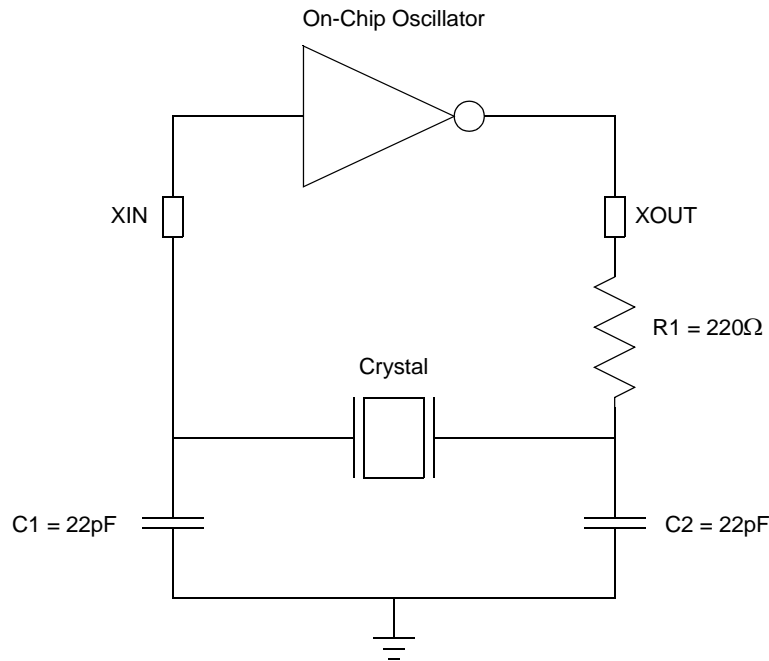

Figure 25. Recommended 20 MHz Crystal Oscillator Configuration

Table 100. Recommended Crystal Oscillator Specifications

Parameter	Value	Units	Comments
Frequency	20	MHz	
Resonance	Parallel		
Mode	Fundamental		
Series Resistance (R_S)	60	Ω	Maximum
Load Capacitance (C_L)	30	pF	Maximum
Shunt Capacitance (C_0)	7	pF	Maximum
Drive Level	1	mW	Maximum

eZ8 CPU Instruction Summary

Table 113 summarizes the eZ8 CPU instructions. The table identifies the addressing modes employed by the instruction, the effect upon the Flags register, the number of CPU clock cycles required for the instruction fetch and the number of CPU clock cycles required for the instruction execution.

Table 113. eZ8 CPU Instruction Summary

| Assembly Mnemonic | Symbolic Operation | Address Mode | | Op Code(s) (Hex) | Flags | | | | | | Fetch Cycles | Instr. Cycles |
		dst	src		C	Z	S	V	D	H		
ADC dst, src	dst ← dst + src + C	r	r	12	*	*	*	*	0	*	2	3
		r	Ir	13							2	4
		R	R	14							3	3
		R	IR	15							3	4
		R	IM	16							3	3
		IR	IM	17							3	4
ADCX dst, src	dst ← dst + src + C	ER	ER	18	*	*	*	*	0	*	4	3
		ER	IM	19							4	3
ADD dst, src	dst ← dst + src	r	r	02	*	*	*	*	0	*	2	3
		r	Ir	03							2	4
		R	R	04							3	3
		R	IR	05							3	4
		R	IM	06							3	3
		IR	IM	07							3	4
ADDX dst, src	dst ← dst + src	ER	ER	08	*	*	*	*	0	*	4	3
		ER	IM	09							4	3

Note: Flags Notation:
* = Value is a function of the result of the operation.
– = Unaffected.
X = Undefined.
0 = Reset to 0.
1 = Set to 1.

Z8   F   08   30   S   H   020   S   G

Environmental Flow
G = Green Plastic Packaging Compound

Temperature Range
S = Standard, 0°C to 70°C
E = Extended, –40°C to +105°C

Speed
020 = 20 MHz

Pin Count*
H = 20
J = 28

Package*
P = PDIP
Q = QFN
S = SOIC
H = SSOP

Device Type
30 = Equipped with ADC and with NVDS.
31 = Equipped without ADC and with NVDS.
32 = Equipped with ADC and without NVDS (12 K version only).
33 = Equipped without ADC and without NVDS (12 K version only).

Memory Size
12 = 12 KB Flash
08 = 8 KB Flash
04 = 4 KB Flash
02 = 2 KB Flash
01 = 1 KB Flash

Memory Type
F = Flash

Device Family
Z8 = Zilog's 8-bit microcontroller