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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908mr8cdw

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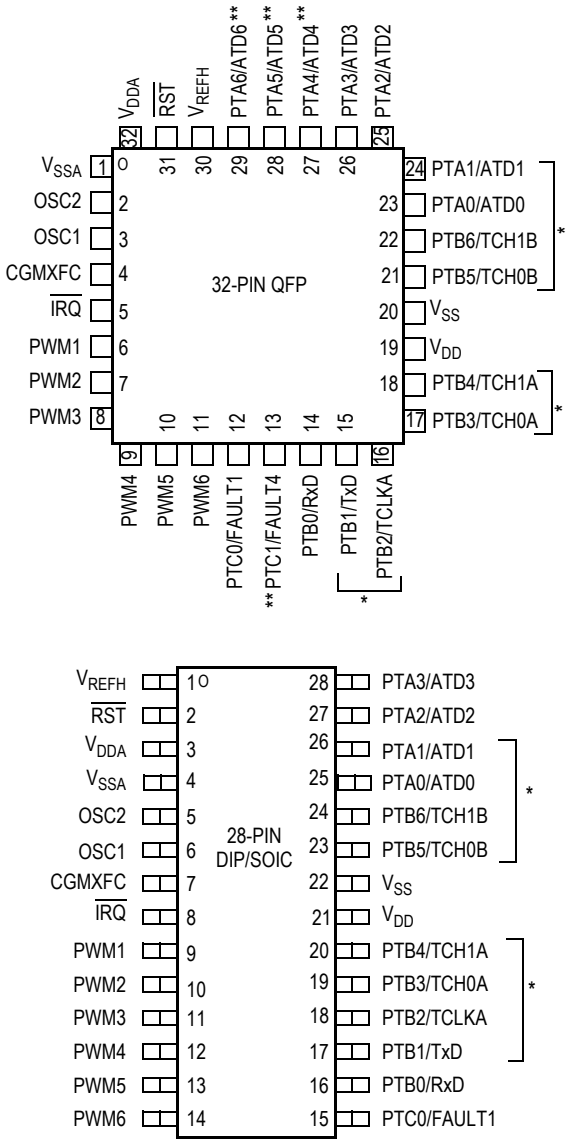
1.5 Pin Assignments

Figure 1-2 shows 32-pin QFP and 28-pin DIP/SOIC pin assignments.



* High current pins
** These pins are not bonded on the 28-pin package.

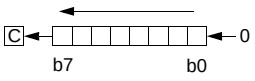
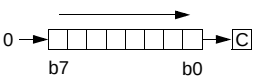
Figure 1-2. QFP and DIP/SOIC Pin Assignments

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0014	TIMA Channel 0 Register High (TACH0H) See page **222.**	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	Indeterminate after reset							
$0015	TIMA Channel 0 Register Low (TACH0L) See page **218.**	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	Indeterminate after reset							
$0016	TIMA Channel 1 Status/Control Register (TASC1) See page **222.**	Read: Write:	CH1F 0	CH1IE	0 R	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Reset:	0	0	0	0	0	0	0	0
$0017	TIMA Channel 1 Register High (TACH1H) See page **222.**	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	Indeterminate after reset							
$0018	TIMA Channel 1 Register Low (TACH1L) See page **222.**	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	Indeterminate after reset							
$0019			Unimplemented							
↓										
$001E			Unimplemented							
$001F	Configuration Register (CONFIG) See page **68.**	Read: Write:	EDGE	BOTNEG	TOPNEG	INDEP	LVIRST	LVIPWR	STOPE	COPD
		Reset:	0	0	0	0	1	1	0	0
$0020	PWM Control Register 1 (PCTL1) See page **175.**	Read: Write:	DISX	DISY	PWMINT	PWMF			LDOK	PWMEN
		Reset:	0	0	0	0	0	0	0	0
$0021	PWM Control Register 2 (PCTL2) See page **177.**	Read: Write:	**LDFQ1**	**LDFQ0**	0	**SEL12**	**SEL34**	**SEL56**	**PRSC1**	**PRSC0**
		Reset:	0	0	0	0	0	0	0	0

U = Unaffected X = Indeterminate R = Reserved **Bold** = Buffered = Unimplemented

Figure 2-2. Control, Status, and Data Registers (Sheet 3 of 10)

Table 6-1. Instruction Set Summary (Sheet 5 of 8)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
INC *opr* INCA INCX INC *opr*,X INC ,X INC *opr*,SP	Increment	M ← M) + 1 A ← (A) + 1 X ← X) + 1 M ← (M) + 1 M ← (M) + 1 M ← (M) + 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd ff ff	4 1 1 4 3 5
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Jump	PC ← Jump Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + *n* (*n* = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Unconditional Address	–	–	–	–	–	–	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	4 5 6 5 4
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X LDA *opr*,SP LDA *opr*,SP	Load A from M	A ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A6 B6 C6 D6 E6 F6 9EE6 9ED6	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
LDHX #*opr* LDHX *opr*	Load H:X from M	H:X ← (M:M + 1)	0	–	–	↕	↕	–	IMM DIR	45 55	ii jj dd	3 4
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X LDX *opr*,SP LDX *opr*,SP	Load X from M	X ← (M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	AE BE CE DE EE FE 9EEE 9EDE	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X LSL *opr*,SP	Logical Shift Left (Same as ASL)		↕	–	–	↕	↕	↕	DIR INH INH IX1 IX SP1	38 48 58 68 78 9E68	dd ff ff	4 1 1 4 3 5
LSR *opr* LSRA LSR*X* LSR *opr*,X LSR ,X LSR *opr*,SP	Logical Shift Right		↕	–	–	0	↕	↕	DIR INH INH IX1 IX SP1	34 44 54 64 74 9E64	dd ff ff	4 1 1 4 3 5
MOV *opr*,*opr* MOV *opr*,X+ MOV #*opr*,*opr* MOV X+,*opr*	Move	$(M)_{Destination}$ ← $(M)_{Source}$ H:X ← (H:X) + 1 (IX+D, DIX+)	0	–	–	↕	↕	–	DD DIX+ IMD IX+D	4E 5E 6E 7E	dd dd dd ii dd dd	5 4 4 4
MUL	Unsigned multiply	X:A ¨ (X) ¥ (A)	–	0	–	–	–	0	INH	42		5

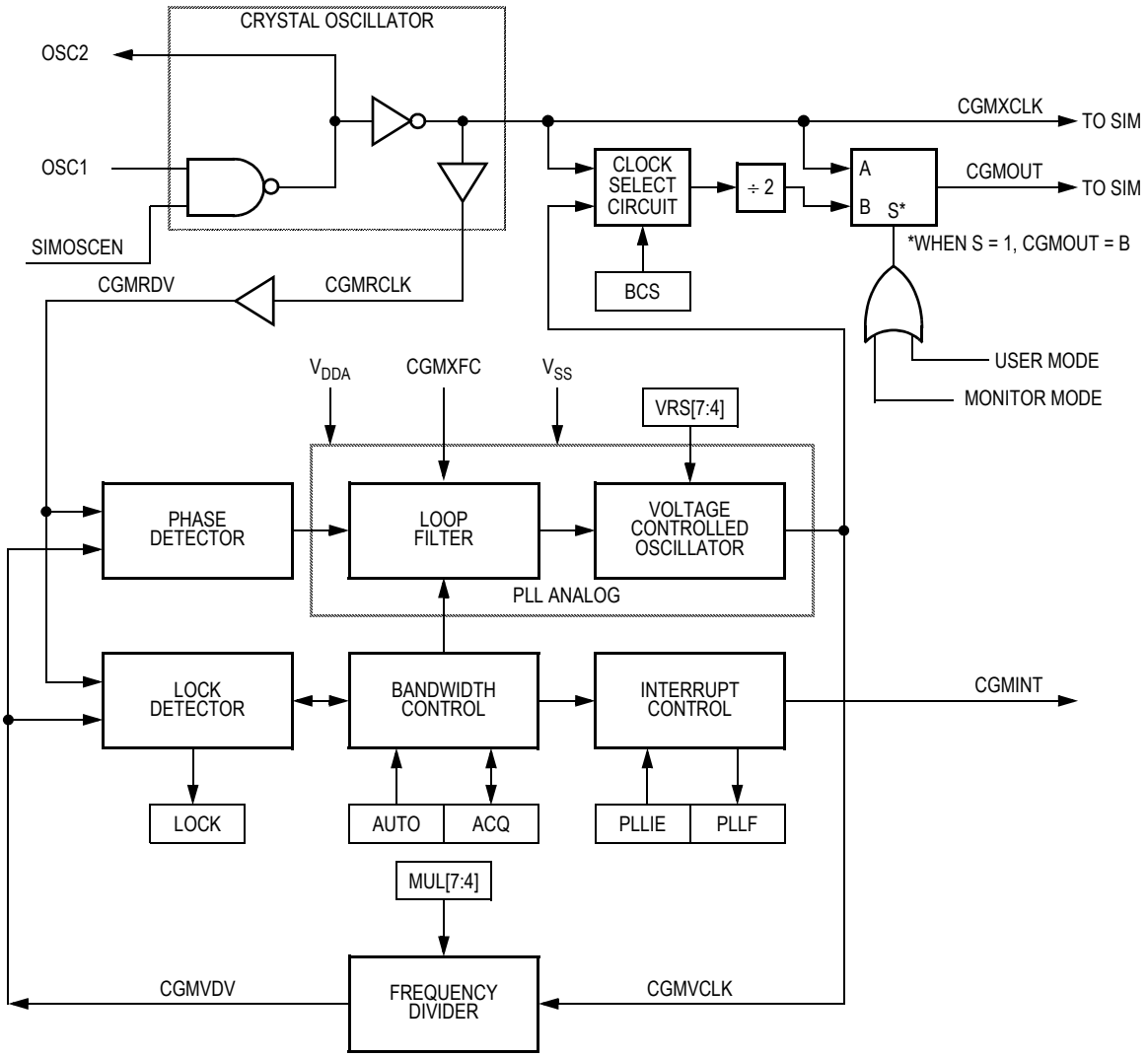


Figure 8-1. CGM Block Diagram

- Phase detector
- Loop filter
- Lock detector

certain number of clock cycles, n_{TRK}, is required to ascertain that the PLL is within the lock mode entry tolerance, Δ_{Lock}. Therefore, the acquisition time, t_{ACQ}, is an integer multiple of n_{ACQ}/f_{RDV}, and the acquisition to lock time, t_{AL}, is an integer multiple of n_{TRK}/f_{RDV}. Also, since the average frequency over the entire measurement period must be within the specified tolerance, the total time usually is longer than t_{Lock} as calculated above.

In manual mode, it is usually necessary to wait considerably longer than t_{Lock} before selecting the PLL clock (see **8.4.3 Base Clock Selector Circuit**) because the factors described in **8.11.2 Parametric Influences on Reaction Time** may slow the lock time considerably.

9.2 Introduction

This section describes the pulse-width modulator for motor control (PWMMC, version A). The MC68HC908MR8 PWM module can generate three complementary PWM pairs or six independent PWM signals. These PWM signals can be center-aligned or edge-aligned. A block diagram of the PWM module is shown in **Figure 9-1**.

A 12-bit timer PWM counter is common to all six channels. PWM resolution is one clock period for edge-aligned operation and two clock periods for center-aligned operation. The clock period is dependent on the internal operating frequency (f_{OP}) and a programmable prescaler. The highest resolution for edge-aligned operation is 125 ns (f_{OP} = 8 MHz). The highest resolution for center-aligned operation is 250 ns (f_{OP} = 8 MHz).

When generating complementary PWM signals, the module features automatic dead-time insertion to the PWM output pairs.

A summary of the PWM registers is shown in **Figure 9-2**.

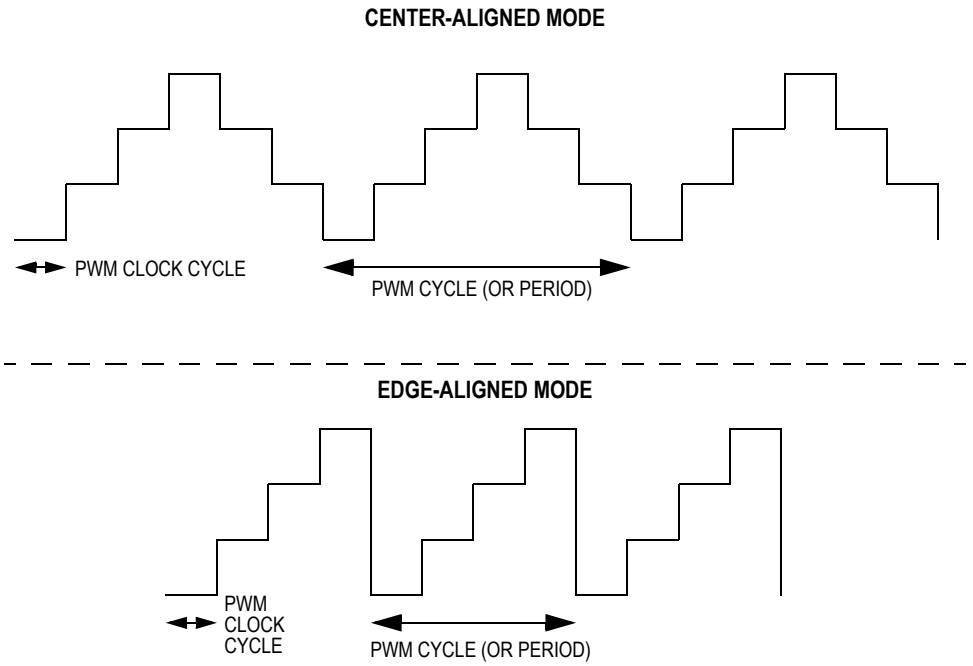


Figure 9-43. PWM Clock Cycle and PWM Cycle Definitions

PWM Load Frequency — The frequency at which new PWM parameters get loaded into the PWM. See **Figure 9-44**.

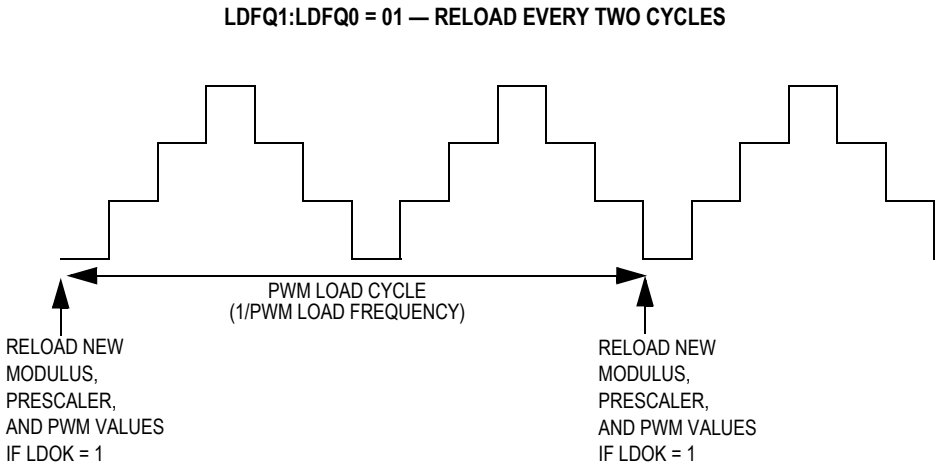


Figure 9-44. PWM Load Cycle/Frequency Definition

10.4 Functional Description

The monitor ROM receives and executes commands from a host computer. **Figure 10-1** shows a sample circuit used to enter monitor mode and communicate with a host computer via a standard RS-232 interface.

Simple monitor commands can access any memory address. In monitor mode, the MCU can execute host-computer code in RAM while all MCU pins retain normal operating mode functions. All communication between the host computer and the MCU is through the serial communications interface (SCI). A level-shifting RS-232 interface is required between the SCI and the host computer. PTB1 requires a pulldown resistor to ensure proper entry into monitor mode.

10.4.1 Entering Monitor Mode

Table 10-1 shows the pin conditions for entering monitor mode.

Table 10-1. Mode Selection

$\overline{\text{IRQ}}$ Pin	RESET	$FFFE/ $FFFF	PLL	PTB0	PTB1	External Clock	CGMOUT	f_{op}	COP	Baud Rate	Comment
X	V_{SS}	X	X	X	X	X	0	0	Disabled	0	No operation until reset = V_{DD}
V_{HI}	V_{DD} or V_{HI}	X	ON	V_{DD}	V_{SS}	4.0 MHz	16.0 MHz	8.0 MHz	Disabled	9600	PLL configured with BCS set by monitor code
V_{DD}	V_{DD}	Blank (FF)	ON	X	X	4.0 MHz	16.0 MHz	8.0 MHz	Disabled	9600	PLL configured with BCS set by monitor code
V_{SS}	V_{DD}	Blank (FF)	OFF	X	X	f_{OSC}	$f_{OSC}/2$	$f_{OSC}/4$	Disabled	f_{OSC} /1024	Enters monitor mode with any external clock rate within operating spec
V_{DD}	V_{DD}	Non-blank	X	X	X	X	X	X	Enabled	X	Enters user mode

X = Don't care
PTB0 = V_{DD} and PTB1 = V_{SS} to enter monitor mode
PTB0 (RXD) and PTB1 (TXD) used for serial communications (all monitor mode)

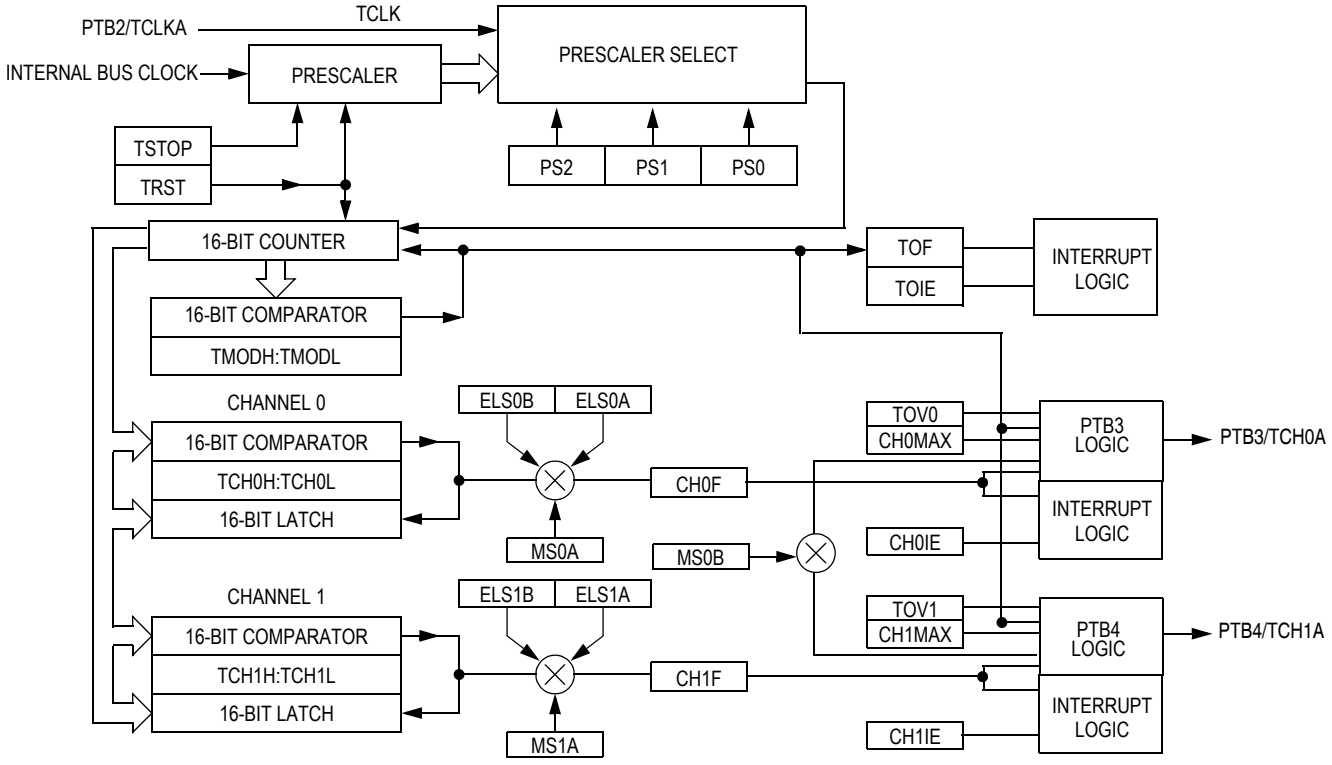


Figure 11-1. TIMA Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000E	TIMA Status/Control Register (TASC) See page **214.**	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST	R			
		Reset:	0	0	1	0	0	0	0	0
$000F	TIMA Counter Register High (TACNTH) See page **216.**	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 11-2. TIMA I/O Register Summary

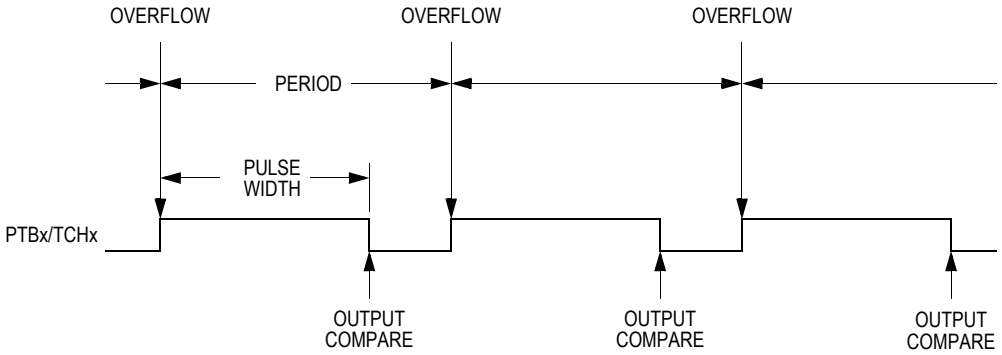


Figure 12-3. PWM Period and Pulse Width

The value in the TIMB counter modulo registers and the selected prescaler output determines the frequency of the PWM output. The frequency of an 8-bit PWM signal is variable in 256 increments. Writing $00FF (255) to the TIMB counter modulo registers produces a PWM period of 256 times the internal bus clock period if the prescaler select value is $000 (see **12.10.1 TIMB Status and Control Register**).

The value in the TIMB channel registers determines the pulse width of the PWM output. The pulse width of an 8-bit PWM signal is variable in 256 increments. Writing $0080 (128) to the TIMB channel registers produces a duty cycle of 128/256 or 50 percent.

12.4.4.1 Unbuffered PWM Signal Generation

Any output compare channel can generate unbuffered PWM pulses as described in **12.4.4 Pulse-Width Modulation (PWM)**. The pulses are unbuffered because changing the pulse width requires writing the new pulse width value over the value currently in the TIMB channel registers.

An unsynchronized write to the TIMB channel registers to change a pulse width value could cause incorrect operation for up to two PWM periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that PWM period. Also, using a TIMB overflow interrupt routine to write a new, smaller pulse width value may cause the compare to be missed. The TIMB may pass the new value before it is written to the TIMB channel registers.

- Interrupt-driven operation with eight interrupt flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

13.4 Functional Description

The SCI allows full-duplex, asynchronous, NRZ serial communication among the MCU and remote devices, including other MCUs. The transmitter and receiver of the SCI operate independently, although they use the same baud rate generator. During normal operation, the CPU monitors the status of the SCI, writes the data to be transmitted, and processes received data.

Figure 13-1 shows the structure of the SCI module. **Figure 13-2** provides a summary of the input/output (I/O) registers.

13.8 I/O Signals

Port B shares two of its pins with the SCI module. The two SCI I/O pins are:

- PTB1/TxD — Transmit data
- PTB0/RxD — Receive data

13.8.1 PTE2/TxD (Transmit Data)

The PTB1/TxD pin is the serial data output from the SCI transmitter. The SCI shares the PTB1/TxD pin with port B. When the SCI is enabled, the PTB1/TxD pin is an output regardless of the state of the DDRF1 bit in data direction register B (DDRB).

13.8.2 PTB0/RxD (Receive Data)

The PTB0/RxD pin is the serial data input to the SCI receiver. The SCI shares the PTB0/RxD pin with port B. When the SCI is enabled, the PTB0/RxD pin is an input regardless of the state of the DDRB0 bit in data direction register B (DDRB).

13.9 I/O Registers

These I/O registers control and monitor SCI operation:

- SCI control register 1 (SCC1)
- SCI control register 2 (SCC2)
- SCI control register 3 (SCC3)
- SCI status register 1 (SCS1)
- SCI status register 2 (SCS2)
- SCI data register (SCDR)
- SCI baud rate register (SCBR)

PEN — Parity Enable Bit

This read/write bit enables the SCI parity function (see **Table 13-4**). When enabled, the parity function inserts a parity bit in the most significant bit position (see **Figure 13-3**). Reset clears the PEN bit.

1 = Parity function enabled
0 = Parity function disabled

PTY — Parity Bit

This read/write bit determines whether the SCI generates and checks for odd parity or even parity (see **Table 13-4**). Reset clears the PTY bit.

1 = Odd parity
0 = Even parity

NOTE: *Changing the PTY bit in the middle of a transmission or reception can generate a parity error.*

Table 13-4. Character Format Selection

Control Bits		Character Format				
M	**PEN:PTY**	**Start Bits**	**Data Bits**	**Parity**	**Stop Bits**	**Character Length (Bits)**
0	0X	1	8	None	1	10
1	0X	1	9	None	1	11
0	10	1	7	Even	1	10
0	11	1	7	Odd	1	10
1	10	1	8	Even	1	11
1	11	1	8	Odd	1	11

SCTE — SCI Transmitter Empty Bit

This clearable, read-only bit is set when the SCDR transfers a character to the transmit shift register. SCTE can generate an SCI transmitter CPU interrupt request. When the SCTIE bit in SCC2 is set, SCTE generates an SCI transmitter CPU interrupt request. In normal operation, clear the SCTE bit by reading SCS1 with SCTE set and then writing to SCDR. Reset sets the SCTE bit.

1 = SCDR data transferred to transmit shift register
0 = SCDR data not transferred to transmit shift register

TC — Transmission Complete Bit

This read-only bit is set when the SCTE bit is set, and no data, preamble, or break character is being transmitted. TC generates an SCI transmitter CPU interrupt request if the TCIE bit in SCC2 is also set. TC is cleared automatically when data, preamble, or break is queued and ready to be sent. There may be up to 1.5 transmitter clocks of latency between queueing data, preamble, and break and the transmission actually starting. Reset sets the TC bit.

1 = No transmission in progress
0 = Transmission in progress

SCRF — SCI Receiver Full Bit

This clearable, read-only bit is set when the data in the receive shift register transfers to the SCI data register. SCRF can generate an SCI receiver CPU interrupt request. When the SCRIE bit in SCC2 is set, SCRF generates a CPU interrupt request. In normal operation, clear the SCRF bit by reading SCS1 with SCRF set and then reading the SCDR. Reset clears SCRF.

1 = Received data available in SCDR
0 = Data not available in SCDR

IDLE — Receiver Idle Bit

This clearable, read-only bit is set when 10 or 11 consecutive logic 1s appear on the receiver input. IDLE generates an SCI error CPU interrupt request if the ILIE bit in SCC2 is also set. Clear the IDLE bit by reading SCS1 with IDLE set and then reading the SCDR. After the receiver is enabled, it must receive a valid character that sets the SCRF bit before an idle condition can set the IDLE bit. Also, after the

Section 15. Computer Operating Properly (COP)

15.1 Contents

15.2 Introduction

This section describes the computer operating properly module (COP, version B), a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by periodically clearing the COP counter.

18.6 Wait Mode

The WAIT instruction can put the MCU in low power-consumption standby mode.

The ADC continues normal operation during wait mode. Any enabled CPU interrupt request from the ADC can bring the MCU out of wait mode. If the ADC is not required to bring the MCU out of wait mode, power down the ADC by setting ADCH[4:0] in the ADC status and control register before executing the WAIT instruction.

18.7 Stop Mode

The STOP instruction can put the MCU in low power-consumption standby mode.

The ADC module becomes inactive after the execution of a STOP instruction. Any pending conversion is aborted. ADC conversions resume when the MCU exits stop mode after an external interrupt. Allow one conversion cycle to stabilize the analog circuitry after exiting stop mode.

18.8 I/O Signals

The ADC module has seven input signals that are shared with port A.

18.8.1 ADC Voltage Reference Pin (V_{REFH})

V_{REFH} is the power supply for setting the reference voltage. Connect the V_{REFH} pin to the same voltage potential as V_{DDA}. There will be a finite current associated with V_{REFH}.

NOTE: *Route V_{REFH} carefully for maximum noise immunity and place bypass capacitors as close as possible to the package.*

21.3 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***21.6 DC Electrical Characteristics*** *for guaranteed operating conditions.*

Characteristic[1]	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +6.0	V
Input voltage	V_{In}	V_{SS} – 0.3 to V_{DD} + 0.3	V
Input high voltage	V_{HI}	V_{DD} + 4	V
Maximum current per pin excluding V_{DD} and V_{SS}	I	± 25	mA
Storage temperature	t_{STG}	–55 to +150	°C
Maximum current out of V_{SS}	I_{MVSS}	100	mA
Maximum current Into V_{DD}	I_{MVDD}	100	mA

1. Voltages are referenced to V_{SS}.

NOTE: *This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{In} and V_{Out} be constrained to the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}).*

Ordering Information