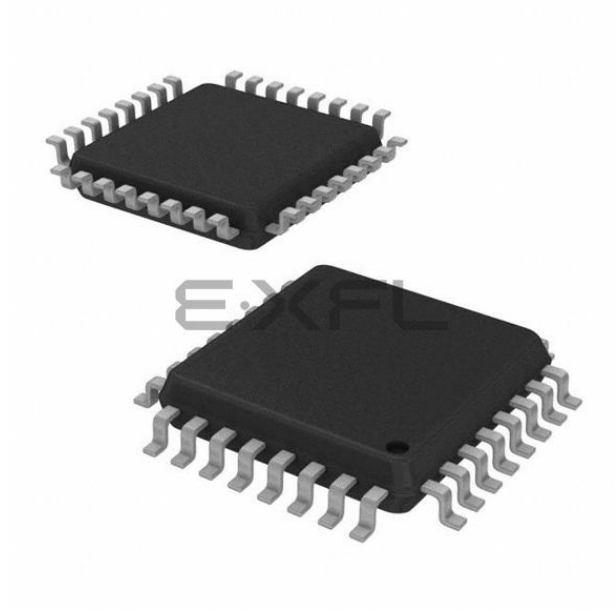

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM
Number of I/O	16
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 7x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc68hc908mr8cfa

- Available packages:
  - 32-pin low-profile quad flat pack (LQFP)
  - 28-pin dual in-line package (PDIP)
  - 28-pin small outline package (SOIC)
- Low-power design, fully static with stop and wait modes
- Break (BRK) module allows single breakpoint setting during in-circuit debugging
- Master reset pin and power-on reset (POR)

Features of the CPU08 include:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the M68HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 u8 multiply instruction
- Fast 16 y8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- C language support

1.4 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908MR8.

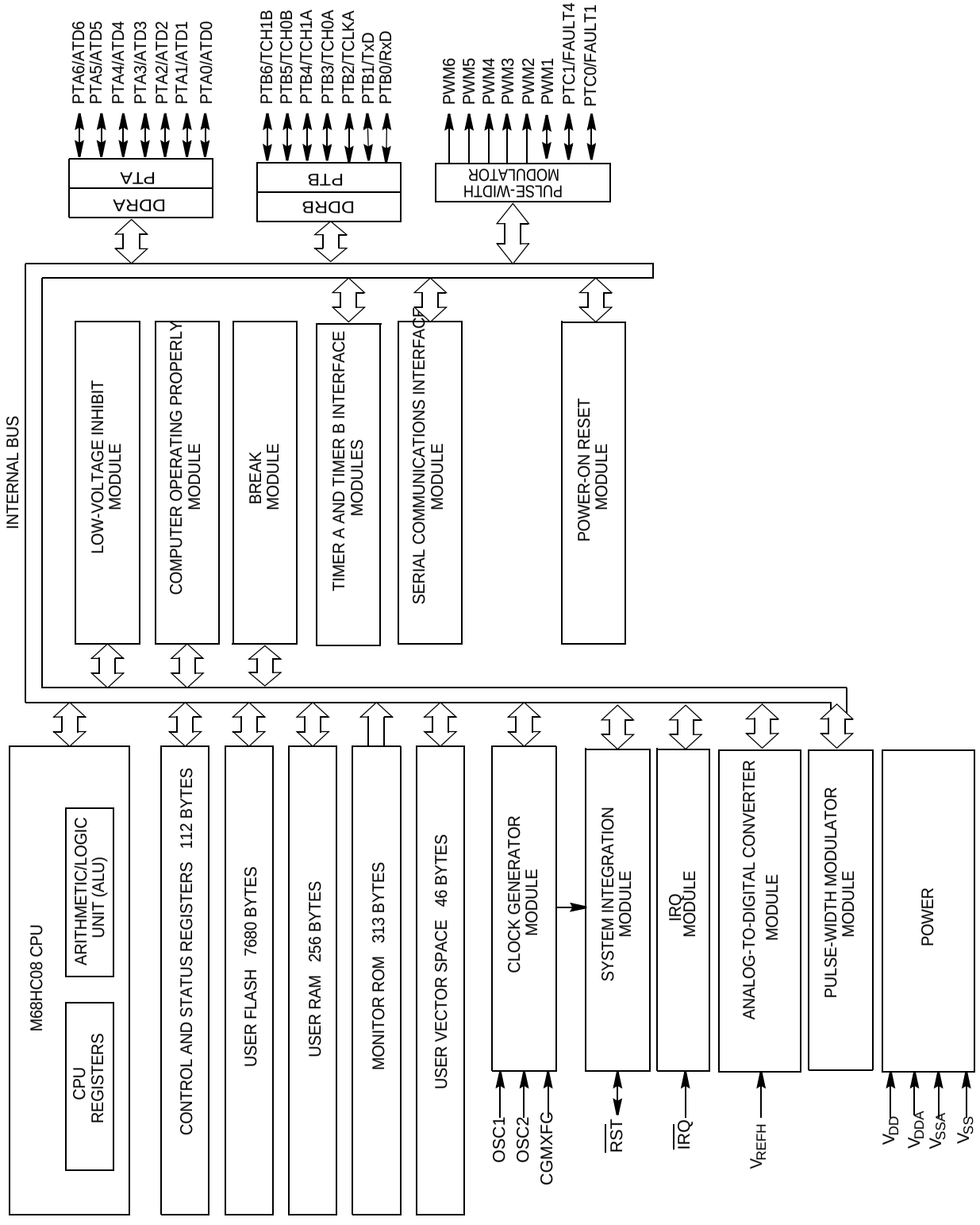

Figure 1-1. MCU Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$005F	Reserved		R	R	R	R	R	R	R	R
$FE00	SIM Break Status Register (SBSR) See page **336.**	Read:	R	R	R	R	R	R	SBSW	R
		Write:							Note(1)	
		Reset:							0	
$FE01	SIM Reset Status Register (SRSR) See page **108.**	Read:	POR	PIN	COP	ILOP	ILAD	0	LVI	0
		Write:	R	R	R	R	R	R	R	R
		Reset:	1	0	0	0	0	0	0	0
$FE03	SIM Break Flag Control Register (SBFCR) See page **109.**	Read:	BCFE	R	R	R	R	R	R	R
		Write:								
		Reset:	0							
$FE08	FLASH Control Register (FLCR) See page **57.**	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0A	Reserved		R	R	R	R	R	R	R	R
$FE0B			Unimplemented							
$FE0C	Break Address Register High (BRKH) See page **334.**	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0D	Break Address Register Low (BRKL) See page **334.**	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE0E	Break Status and Control Register (BRKSCR) See page **333.**	Read:	BRKE	BRKA	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

U = Unaffected X = Indeterminate R = Reserved **Bold** = Buffered = Unimplemented

Figure 2-2. Control, Status, and Data Registers (Sheet 9 of 10)

Note 1. Writing a logic 0 clears SBSW.

address range desired.

4. Wait for a time, t_{NVS} (minimum of 10 μs).
5. Set the HVEN bit.
6. Wait for a time, t_{PGS} (minimum of 5 μs).
7. Write data to the FLASH address to be programmed.
8. Wait for a time, t_{PROG} (minimum of 30 μs).
9. Repeat step 7 and step 8 until all the bytes within the row are programmed.
10. Clear the PGM bit.
11. Wait for a time, t_{NVH} (minimum of 5 μs).
12. Clear the HVEN bit.
13. After a time, t_{RCV} (typically 1 μs), the memory can be accessed in read mode again.

NOTE: The time between each FLASH address change, or the time between the last FLASH address programmed to clear the PGM bit, must not exceed the maximum programming time, t_{PROG}.

Programming and erasing of FLASH locations cannot be performed by code being executed from the FLASH memory. While these operations must be performed in the order shown, other unrelated operations may occur between the steps. Do not exceed t_{PROG} maximum. See 21.7 Memory Characteristics .

4.3 FLASH Programming Algorithm

Refer to **Figure 4-2** for an algorithm for programming a row (32 bytes) of FLASH memory.

9.11 PWM Operation in Break Mode

If the microcontroller goes into break mode (or background mode), the clocks to the PWM generator and output control blocks will freeze. This allows the user to set a breakpoint on a development system and examine the register contents and PWM outputs at that point. It also allows the user to single-step through the code.

The clocks to the fault block will continue to run. Therefore, if a fault occurs while the microcontroller is in break mode, the PWM outputs will immediately be driven to their inactive state(s).

During break mode, the system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the SIM break flag control register (SBFCR) enables software to clear status bits during the break state. Refer to 7.7.5 SIM Break Flag Control Register .

To allow software to clear status bits during a break interrupt, write a logic 1 to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect the PWMF and FFLAGx bits during the break state, make sure BCFE is a logic 0. With BCFE at logic 0 (its default state), software can read and write the status and control registers during the break state without affecting the PWMF and FFLAGx bits.

FFLAG4 Fault Event Flag 4

The FFLAG4 event bit is set within two CPU cycles after a rising edge on fault pin 4. To clear the FFLAG4 bit, the user must write a 1 to the FTACK4 bit in the fault acknowledge register.

1 = A fault has occurred on fault pin 4
0 = No new fault on fault pin 4

FPIN4 State of Fault Pin 4 Bit

This read-only bit allows the user to read the current state of fault pin 4.

1 = Fault pin 4 is at logic 1.
0 = Fault pin 4 is at logic 0.

9.12.10 Fault Ac knowledge Register

The fault acknowledge register (FTACK) is used to acknowledge and clear the FFLAGs. In addition, it is used to monitor the current sensing bits to test proper operation.

Address: $0024

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0
Write:		FTACK 4						FTACK 1
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-41. Fault Acknow ledge Register (FTACK)

If TIMA functions are not required during wait mode, reduce power consumption by stopping the TIMA before executing the WAIT instruction.

11.7 Stop Mode

TIMA is inactive after execution of a STOP instruction. The STOP instruction does not affect register conditions or the state of the TIMA counter. TIMA operation resumes when the MCU exits stop mode after an external interrupt.

11.8 TIMA During Break Interrupts

A break interrupt stops the TIMA counter and inhibits input captures.

The system integration module (SIM) controls whether status bits in other modules can be cleared during the break state. The BCFE bit in the SIM break flag control register (SBFCR) enables software to clear status bits during the break state. See 7.7.5 SIM Break Flag Control Register .

To allow software to clear status bits during a break interrupt, write a logic 1 to the BCFE bit. If a status bit is cleared during the break state, it remains cleared when the MCU exits the break state.

To protect status bits during the break state, write a logic 0 to the BCFE bit. With BCFE at logic 0 (its default state), software can read and write I/O registers during the break state without affecting status bits. Some status bits have a 2-step read/write clearing procedure. If software does the first step on such a bit before the break, the bit cannot change during the break state as long as BCFE is at logic 0. After the break, doing the second step clears the status bit.

11.9 I/O Signals

Port B shares three of its pins with the TIMA. PTB2/TCLKA is an external clock input to the TIMA prescaler. The two TIMA channel I/O pins are PTB3/TCH0A and PTB4/TCH1A.

TRST TIMB Reset Bit

Setting this write-only bit resets the TIMB counter and the TIMB prescaler. Setting TRST has no effect on any other registers. Counting resumes from $0000. TRST is cleared automatically after the TIMB counter is reset and always reads as logic 0. Reset clears the TRST bit.

1 = Prescaler and TIMB counter cleared
0 = No effect

NOTE: *Setting the TSTOP and TRST bits simultaneously stops the TIMB counter at a value of $0000.*

PS[2:0] Prescaler Select Bits

These read/write bits select one of the seven prescaler outputs as the input to the TIMB counter as Table 12-1 shows. Reset clears the PS[2:0] bits.

Table 12-1. Pres caler Selection

PS[2:0]	TIMB Clock Source
000	Internal Bus Clock y1
001	Internal Bus Clock y2
010	Internal Bus Clock y4
011	Internal Bus Clock y8
100	Internal Bus Clock y16
101	Internal Bus Clock y32
110	Internal Bus Clock y64
111	Invalid: do not use this value

21.4 Functional Operating Range

Characteristic	Symbol	Value	Unit
Operating temperature range[1] MC68HC908MR8CP MC68HC908MR8CFA MC68HC908MR8CDW MC68HC908MR8VFA MC68HC908MR8VP MC68HC908MR8VDW MC68HC908MR8MFA MC68HC908MR8MP MC68HC908MR8MDW	T_A	 –40 to +85 –40 to +85 –40 to +85 –40 to +105 –40 to +105 –40 to +105 –40 to +125 –40 to +125 –40 to +125	°C
Operating voltage range	V_{DD}	5.0 r 10%	V

1. Contact a Freescale representative for temperature availability.
   C = Extended temperature range (–40 to +85 °C)
   V = Industrial temperature range (–40 to +105 °C)
   M = Automotive temperature range (–40 to +125 °C)

M68HC08