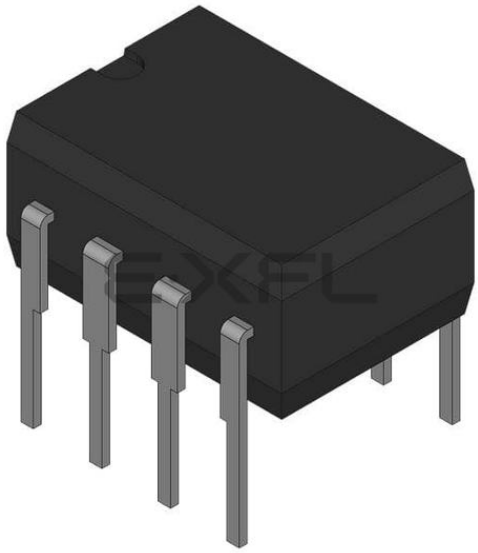

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc908mr8cpe

Section 8. Clock Generator Module (CGM)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0014	TIMA Channel 0 Register High (TACH0H) See page **222.**	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	Indeterminate after reset							
$0015	TIMA Channel 0 Register Low (TACH0L) See page **218.**	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	Indeterminate after reset							
$0016	TIMA Channel 1 Status/Control Register (TASC1) See page **222.**	Read: Write:	CH1F 0	CH1IE	0 R	MS1A	ELS1B	ELS1A	TOV1	CH1MAX
		Reset:	0	0	0	0	0	0	0	0
$0017	TIMA Channel 1 Register High (TACH1H) See page **222.**	Read: Write:	Bit 15	14	13	12	11	10	9	Bit 8
		Reset:	Indeterminate after reset							
$0018	TIMA Channel 1 Register Low (TACH1L) See page **222.**	Read: Write:	Bit 7	6	5	4	3	2	1	Bit 0
		Reset:	Indeterminate after reset							
$0019			Unimplemented							
↓										
$001E			Unimplemented							
$001F	Configuration Register (CONFIG) See page **68.**	Read: Write:	EDGE	BOTNEG	TOPNEG	INDEP	LVIRST	LVIPWR	STOPE	COPD
		Reset:	0	0	0	0	1	1	0	0
$0020	PWM Control Register 1 (PCTL1) See page **175.**	Read: Write:	DISX	DISY	PWMINT	PWMF			LDOK	PWMEN
		Reset:	0	0	0	0	0	0	0	0
$0021	PWM Control Register 2 (PCTL2) See page **177.**	Read: Write:	**LDFQ1**	**LDFQ0**	0	**SEL12**	**SEL34**	**SEL56**	**PRSC1**	**PRSC0**
		Reset:	0	0	0	0	0	0	0	0

U = Unaffected X = Indeterminate R = Reserved **Bold** = Buffered = Unimplemented

Figure 2-2. Control, Status, and Data Registers (Sheet 3 of 10)

TOPNEG — Top-Side PWM Polarity Bit

TOPNEG determines if the top-side PWMs will have positive or negative polarity. See **Section 9. Pulse-Width Modulator for Motor Control (PWMMC)**.

1 = Negative polarity
0 = Positive polarity

INDEP — Independent Mode Enable Bit

INDEP determines if the motor control PWMs will be six independent PWMs or three complementary PWM pairs. See **Section 9. Pulse-Width Modulator for Motor Control (PWMMC)**.

1 = Six independent PWMs
0 = Three complementary PWM pairs

LVIPWR — LVI Power Enable Bit

LVIPWR enables the LVI module. See **Section 17. Low-Voltage Inhibit (LVI)**.

1 = LVI module power enabled
0 = LVI module power disabled

LVIRST — LVI Reset Enable Bit

LVIRST enables the reset signal from the LVI module. See **Section 17. Low-Voltage Inhibit (LVI)**.

1 = LVI module resets enabled
0 = LVI module resets disabled

STOPE — STOP Enable Bit

STOPE enables the STOP instruction. See **Section 6. Central Processor Unit (CPU)**.

1 = STOP instruction is enabled.
0 = STOP instruction is disabled and executes as an illegal instruction.

COPD — COP Disable Bit

COPD disables the COP module. See **Section 15. Computer Operating Properly (COP)**.

1 = COP module disabled
0 = COP module enabled

6.4.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.

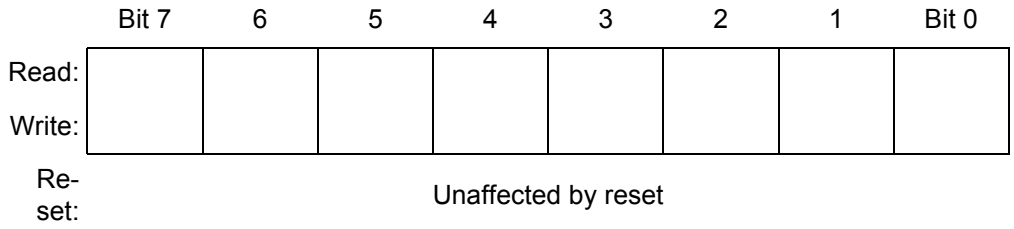


Figure 6-2. Accumulator (A)

6.4.2 Index Register

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

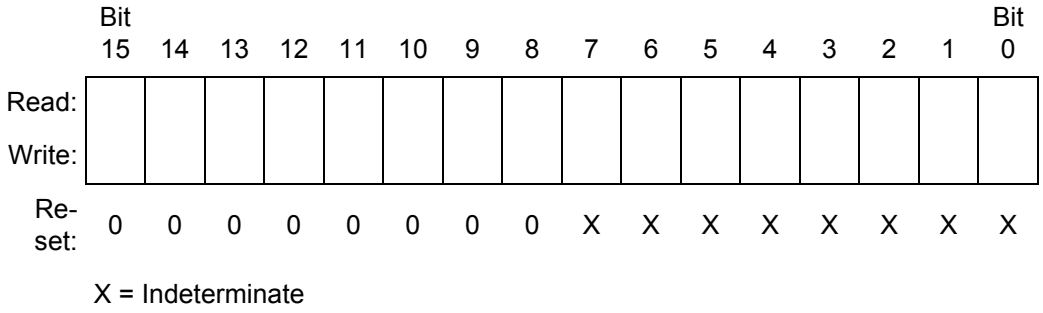


Figure 6-3. Index Register (H:X)

The index register can serve also as a temporary data storage location.

Table 6-1. Instruction Set Summary (Sheet 3 of 8)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? (Z) = 0	–	–	–	–	–	–	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? (N) = 0	–	–	–	–	–	–	REL	2A	rr	3
BRA *rel*	Branch Always	PC ¨ (PC) + 2 + *rel*	–	–	–	–	–	–	REL	20	rr	3
BRCLR *n,opr,rel*	Branch if Bit *n* in M Clear	PC ← (PC) + 3 + *rel* ? (Mn) = 0	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2	–	–	–	–	–	–	REL	21	rr	3
BRSET *n,opr,rel*	Branch if Bit *n* in M Set	PC ← (PC) + 3 + *rel* ? (Mn) = 1	–	–	–	–	–	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n,opr*	Set Bit *n* in M	Mn ← 1	–	–	–	–	–	–	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	4 4 4 4 4 4 4 4
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	–	–	–	–	–	–	REL	AD	rr	4
CBEQ *opr,rel* CBEQA #*opr,rel* CBEQX #*opr,rel* CBEQ *opr*,X+,*rel* CBEQ X+,*rel* CBEQ *opr*,SP,*rel*	Compare and Branch if Equal	PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 3 + rel ? (X) – (M) = $00 PC ← (PC) + 3 + rel ? (A) – (M) = $00 PC ← (PC) + 2 + rel ? (A) – (M) = $00 PC ← (PC) + 4 + rel ? (A) – (M) = $00	–	–	–	–	–	–	DIR IMM IMM IX1+ IX+ SP1	31 41 51 61 71 9E61	dd rr ii rr ii rr ff rr rr ff rr	5 4 4 5 4 6
CLC	Clear Carry Bit	C ← 0	–	–	–	–	–	0	INH	98		1
CLI	Clear Interrupt Mask	I ← 0	–	–	0	–	–	–	INH	9A		2
CLR *opr* CLRA CLRX CLRH CLR *opr*,X CLR ,X CLR *opr*,SP	Clear	M ← $00 A ← $00 X ← $00 H ← $00 M ← $00 M ← $00 M ← $00	0	–	–	0	1	–	DIR INH INH INH IX1 IX SP1	3F 4F 5F 8C 6F 7F 9E6F	dd ff ff	3 1 1 1 3 2 4

7.3.3 Clocks in Wait Mode

In wait mode, the CPU clocks are inactive. The SIM also produces two sets of clocks for other modules. Refer to the wait mode subsection of each module to see if the module is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

7.4 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{\text{RST}}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector $FFFE–FFFF ($FEFE–FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see **7.5 SIM Counter**), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). See **7.7.4 SIM Reset Status Register**.

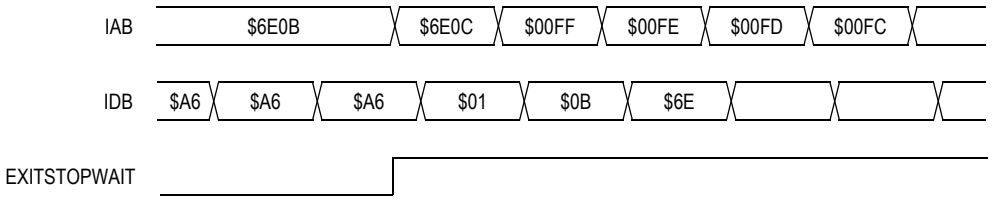
7.4.1 External Pin Reset

Pulling the asynchronous $\overline{\text{RST}}$ pin low halts all processing. The PIN bit of the SIM reset status register (SRSR) is set as long as $\overline{\text{RST}}$ is held low for a minimum of 67 CGMXCLK cycles, assuming that neither the POR nor the LVI was the source of the reset. See **Table 7-2** for details. **Figure 7-4** shows the relative timing.

is active or inactive in wait mode. Some modules can be programmed to be active in wait mode.

Wait mode can also be exited by a reset or break. A break interrupt during wait mode sets the SIM break stop/wait bit, SBSW, in the SIM break status register (SBSR). If the COP disable bit, COPD, in the configuration register is logic 0, then the computer operating properly module (COP) is enabled and remains active in wait mode.

Figure 7-13 and **Figure 7-14** show the timing for wait recovery.



Note: EXITSTOPWAIT = $\overline{\text{RST}}$ pin or CPU interrupt or break interrupt

Figure 7-13. Wait Recovery from Interrupt or Break

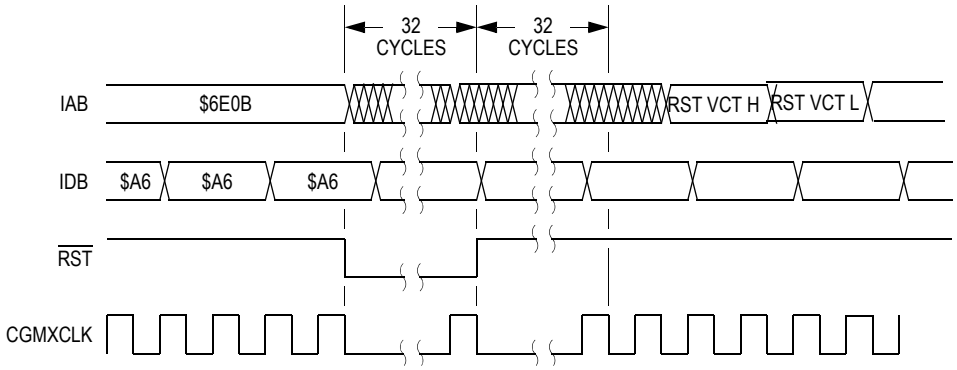


Figure 7-14. Wait Recovery from Internal Reset

7.7.2 Stop Mode

In stop mode, the SIM counter is reset and the system clock is disabled. An external interrupt request will cause an exit from stop mode. Stacking for interrupts begins after the stop recovery delay time of 4096 CGMXCLK cycles has elapsed. Reset or break also cause an exit from stop mode.

The SIM disables the clock generator module outputs in stop mode, stopping the CPU and all peripherals.

NOTE: *It is important to note that when using the PWM generator Its outputs will stop toggling when stop mode is entered. The PWM module must be disabled before entering stop mode to prevent external inverter failure.*

7.7.3 SIM Break Status Register

The SIM break status register (SBSR) contains a flag to indicate that a break caused an exit from wait mode.

Address: $FE00

	Blt 7	6	5	4	3	2	1	Bit 0
Read:	R	R	R	R	R	R	SBSW	R
Write:							Note(1)	
Reset:							0	

R = Reserved

1. Writing a logic 0 clears SBSW.

Figure 7-15. SIM Break Status Register (SBSR)

SBSW — SIM Break Stop/Wait Bit

This status bit is useful in applications requiring a return to wait mode after exiting from a break interrupt. Clear SBSW by writing a logic 0 to it. Reset clears SBSW.

1 = Wait mode was exited by break interrupt.
0 = Wait mode was not exited by break interrupt.

8.6.3 PLL Programming Register

The PLL programming register (PPG) contains the programming information for the modulo feedback divider and the programming information for the hardware configuration of the VCO.

Address: $005E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MUL7	MUL6	MUL5	MUL4	VRS7	VRS6	VRS5	VRS4
Reset:	0	1	1	0	0	1	1	0

Figure 8-7. PLL Programming Register (PPG)

MUL[7:4] — Multiplier Select Bits

These read/write bits control the modulo feedback divider that selects the VCO frequency multiplier, N. See **8.4.2.1 PLL Circuits** and **8.4.2.4 Programming the PLL**. A value of $0 in the multiplier select bits configures the modulo feedback divider the same as a value of $1. Reset initializes these bits to $6 to give a default multiply value of 6.

Table 8-1. VCO Frequency Multiplier (N) Selection

MUL7:MUL6:MUL5:MUL4	VCO Frequency Multiplier (N)
0000	1
0001	1
0010	2
0011	3
↓	↓
1101	13
1110	14
1111	15

NOTE: *The multiplier select bits have built-in protection that prevents them from being written when the PLL is on (PLLON = 1).*

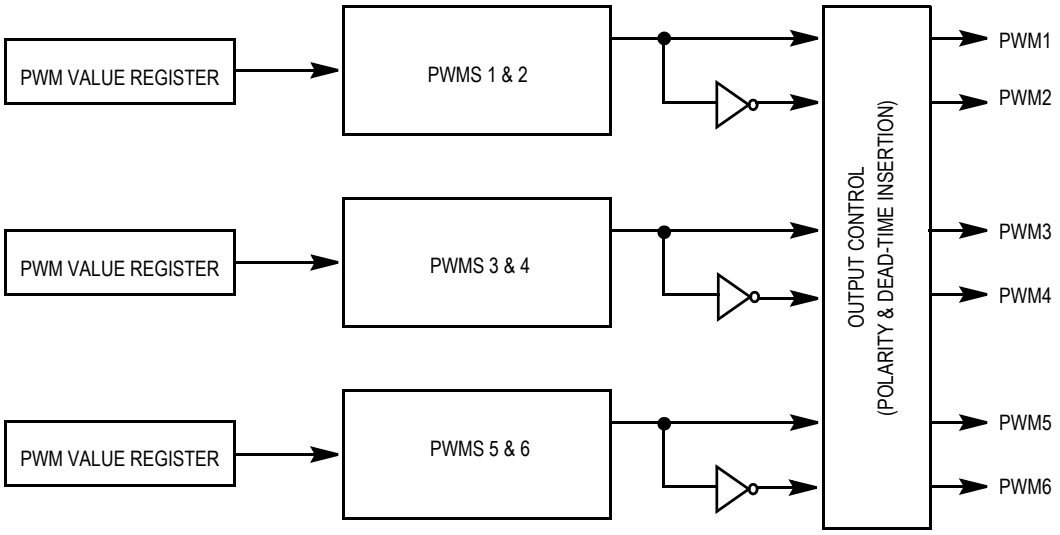


Figure 9-11. Complementary Pairing

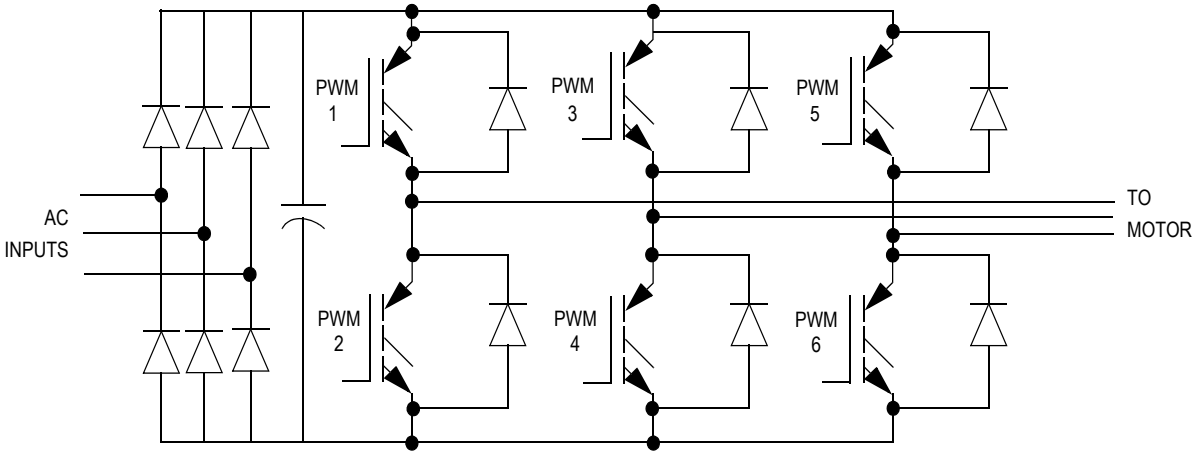


Figure 9-12. Typical AC Motor Drive

When complementary operation is used, two additional features are provided:

- Dead-time insertion
- Separate top/bottom pulse width correction to correct for distortions caused by the motor drive characteristics.

If independent operation is chosen, each PWM has its own PWM value register.

10.4 Functional Description

The monitor ROM receives and executes commands from a host computer. **Figure 10-1** shows a sample circuit used to enter monitor mode and communicate with a host computer via a standard RS-232 interface.

Simple monitor commands can access any memory address. In monitor mode, the MCU can execute host-computer code in RAM while all MCU pins retain normal operating mode functions. All communication between the host computer and the MCU is through the serial communications interface (SCI). A level-shifting RS-232 interface is required between the SCI and the host computer. PTB1 requires a pulldown resistor to ensure proper entry into monitor mode.

10.4.1 Entering Monitor Mode

Table 10-1 shows the pin conditions for entering monitor mode.

Table 10-1. Mode Selection

$\overline{\text{IRQ}}$ Pin	RESET	$FFFE/ $FFFF	PLL	PTB0	PTB1	External Clock	CGMOUT	f_{op}	COP	Baud Rate	Comment
X	V_{SS}	X	X	X	X	X	0	0	Disabled	0	No operation until reset = V_{DD}
V_{HI}	V_{DD} or V_{HI}	X	ON	V_{DD}	V_{SS}	4.0 MHz	16.0 MHz	8.0 MHz	Disabled	9600	PLL configured with BCS set by monitor code
V_{DD}	V_{DD}	Blank (FF)	ON	X	X	4.0 MHz	16.0 MHz	8.0 MHz	Disabled	9600	PLL configured with BCS set by monitor code
V_{SS}	V_{DD}	Blank (FF)	OFF	X	X	f_{OSC}	$f_{OSC}/2$	$f_{OSC}/4$	Disabled	f_{OSC} /1024	Enters monitor mode with any external clock rate within operating spec
V_{DD}	V_{DD}	Non-blank	X	X	X	X	X	X	Enabled	X	Enters user mode

X = Don't care
PTB0 = V_{DD} and PTB1 = V_{SS} to enter monitor mode
PTB0 (RXD) and PTB1 (TXD) used for serial communications (all monitor mode)

11.10.2 TIMA Counter Registers

The two read-only TIMA counter registers contain the high and low bytes of the value in the TIMA counter. Reading the high byte (TACNTH) latches the contents of the low byte (TACNTL) into a buffer. Subsequent reads of TACNTH do not affect the latched TACNTL value until TACNTL is read. Reset clears the TIMA counter registers. Setting the TIMA reset bit (TRST) also clears the TIMA counter registers.

NOTE: *If TACNTH is read during a break interrupt, be sure to unlatch TACNTL by reading TACNTL before exiting the break interrupt. Otherwise, TACNTL retains the value latched during the break.*

Register Name and Address: TACNTH — $000F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

Register Name and Address: TACNTL — $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Write:	R	R	R	R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 11-5. TIMA Counter Registers (TACNTH and TACNTL)

17.4.4 LVI Trip Selection

The TRPSEL bit allows the user to choose between 5 percent and 10 percent tolerance when monitoring the supply voltage. The 10 percent option is enabled out of reset. Writing a logic 1 to TRPSEL will enable the 5 percent option.

NOTE: *The MCU is guaranteed to operate at a minimum supply voltage. The trip point (V_{LVR1} or V_{LVR2}) may be lower than this.*

17.5 LVI Status and Control Register

The LVI status register flags V_{DD} voltages below the V_{LVRX} level.

Address: $FE0F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	TRPSEL	0	0	0	0	0
Write:	R	R		R	R	R	R	R
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 17-3. LVI Status and Control Register (LVISCR)

LVIOUT — LVI Output Bit

This read-only flag becomes set when the V_{DD} voltage falls below the V_{LVRX} voltage for 32 to 40 CGMXCLK cycles. See **Table 17-1**. Reset clears the LVIOUT bit.

Table 17-1. LVIOUT Bit Indication

V_{DD}		LVIOUT
At level:	**For number of CGMXCLK cycles:**	
$V_{DD} > V_{LVRX} + V_{LVHX}$	Any	0
$V_{DD} < V_{LVRX}$	< 32 CGMXCLK CYCLES	0
$V_{DD} < V_{LVRX}$	Between 32 and 40 CGMXCLK cycles	0 or 1
$V_{DD} < V_{LVRX}$	> 40 CGMXCLK cycles	1

18.9 I/O Registers

These I/O registers control and monitor operation of the ADC:

- ADC status and control register (ADSCR)
- ADC data registers (ADRH and ARDL)
- ADC control register (ADCR)
- ADC clock register (ADCLK)

18.9.1 ADC Status and Control Register

These paragraphs describe the function of the ADC status and control register (ADSCR). Writing ADSCR aborts the current conversion and initiates a new conversion.

Address: $0040

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Reset:	0	0	0	1	1	1	1	1

Figure 18-3. ADC Status and Control Register (ADSCR)

COCO — Conversions Complete Bit

When AIEN bit is a logic 0, the COCO is a read-only bit which is set each time a conversion is completed except in the continuous conversion mode where it is set after the first conversion. This bit is cleared whenever the ADC status and control register is written or whenever the ADC data register is read.

If AIEN bit is a logic 1, the COCO is a read/write bit which selects the CPU to service the ADC interrupt request. Reset clears this bit.

1 = Conversion completed (AIEN = 0) interrupt (AIEN = 1)
0 = Conversion not completed (AIEN = 0)/CPU interrupt (AIEN = 1)

18.9.2 ADC Data Register High

In left justified mode, this 8-bit result register holds the eight MSBs of the 10-bit result. This register is updated each time an ADC single channel conversion completes. Reading ADRH latches the contents of ADRL until ADRL is read. Until ADRL is read, all subsequent ADC results will be lost.

Address: $0041

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2
Write:	R	R	R	R	R	R	R	R
Reset:	Unaffected by Reset							

R = Reserved

Figure 18-4. ADC Data Register High (ADRH) Left Justified Mode

In right justified mode, this 8-bit result register holds the two MSBs of the 10-bit result. All other bits read as 0. This register is updated each time a single channel ADC conversion completes. Reading ADRH latches the contents of ADRL until ADRL is read. Until ADRL is read, all subsequent ADC results will be lost.

Address: $0041

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	AD9	AD8
Write:	R	R	R	R	R	R	R	R
Reset:	Unaffected by Reset							

R = Reserved

Figure 18-5. ADC Data Register High (ADRH) Right Justified Mode

Section 19. Power-On Reset (POR)

19.1 Contents

19.2 Introduction

This section describes the power-on reset (POR) module.

19.3 Functional Description

The POR module provides a known, stable signal to the MCU at power-on. This signal tracks V_{DD} until the MCU generates a feedback signal to indicate that it is properly initialized. At this time, the POR drives its output low. The POR is not a brown-out detector, low-voltage detector, or glitch detector. V_{DD} at the POR must go completely to 0 to reset the MCU. To detect power-loss conditions, use a low-voltage inhibit module (LVI) or other suitable circuit.

Break (BRK)

pointer — Pointer register. An index register is sometimes called a pointer register because its contents are used in the calculation of the address of an operand and, therefore, points to the operand.

polarity — The two opposite logic levels, logic 1 and logic 0, which correspond to two different voltage levels, V_{DD} and V_{SS}.

polling — Periodically reading a status bit to monitor the condition of a peripheral device.

port — A set of wires for communicating with off-chip devices.

prescaler — A circuit that generates an output signal related to the input signal by a fractional scale factor such as 1/2, 1/8, 1/10, etc.

program — A set of computer instructions that causes a computer to perform a desired operation or operations.

program counter (PC) — A 16-bit register in the CPU08. The PC register holds the address of the next instruction or operand that the CPU will use.

pull — An instruction that copies into the accumulator the contents of a stack RAM location. The stack RAM address is in the stack pointer.

pullup — A transistor in the output of a logic gate that connects the output to the logic 1 voltage of the power supply.

pulse-width — The amount of time a signal is on as opposed to being in its off state.

pulse-width modulation (PWM) — Controlled variation (modulation) of the pulse width of a signal with a constant frequency.

push — An instruction that copies the contents of the accumulator to the stack RAM. The stack RAM address is in the stack pointer.

PWM period — The time required for one complete cycle of a PWM waveform.

PMC — Pulse width modulated motor control module

RAM — Random access memory. All RAM locations can be read or written by the CPU. The contents of a RAM memory location remain valid until the CPU writes a different value or until power is turned off.

RC circuit — A circuit consisting of capacitors and resistors having a defined time constant.

read — To copy the contents of a memory location to the accumulator.