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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI
Peripherals	LVD, POR, PWM
Number of I/O	12
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.600", 15.24mm)
Supplier Device Package	28-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908mr8mpe

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1.2 Introduction

The MC68HC908MR8 is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCU). The M68HC08 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

2.3 Unimplemented Memory Locations

Some addresses are unimplemented. Accessing an unimplemented address will cause an illegal address reset. In the memory map and in the input/output (I/O) register summary, unimplemented addresses are shaded.

Some I/O bits are read-only; the write function is unimplemented. Writing to a read-only I/O bit has no effect on MCU operation. In register figures, the write function of read-only bits is shaded. Similarly, some I/O bits are write-only; the read function is unimplemented. Reading of write-only I/O bits has no effect on microcontroller unit (MCU) operation. In register figures, the read function of write-only bits is shaded.

2.4 Reserved Memory Locations

Some addresses are reserved. Writing to a reserved address can have unpredictable effects on MCU operation. In the memory map and in the I/O register summary, reserved addresses are marked with the word reserved.

Some I/O bits are reserved. Writing to a reserved bit can have unpredictable effects on MCU operation. In register figures, reserved bits are marked with the letter R.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
\$003F	IRQ Status/Control Register (ISCR) See page 303.	Read:	0	0	0	0	IRQF	0	IMASK1	MODE1
		Write:	R	R	R	R		ACK1		
		Reset:	0	0	0	0	0	0	0	0
\$0040	ADC Status and Control Register (ADSCR) See page 319.	Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
		Write:								
		Reset:	0	0	0	1	1	1	1	1
\$0041	ADC Data Register High (ADRH) See page 322.	Read:	0	0	0	0	0	0	AD9	AD8
		Write:	R	R	R	R	R	R	R	R
		Reset:	Unaffected by reset							
\$0042	ADC Data Register Low (ADRL) See page 323.	Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Write:	R	R	R	R	R	R	R	R
		Reset:	Unaffected by reset							
\$0043	ADC Clock Register (ADCLK) See page 324.	Read:	ADIV2	ADIV1	ADIV0	ADICLK	MODE1	MODE0	0	0
		Write:							0	R
		Reset:	0	0	0	0	0	1	0	0
\$0044			Unimplemented							
↓										
\$0050			Unimplemented							
\$0051	TIMB Status/Control Register (TBSC) See page 238.	Read:	TOF	TOIE	TSTOP	0	0	PS2	PS1	PS0
		Write:	0			TRST	R			
		Reset:	0	0	1	0	0	0	0	0
\$0052	TIMB Counter Register High (TBCNTH) See page 240.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
\$0053	TIMB Counter Register Low (TBCNTL) See page 240.	Read:	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		Write:	R	R	R	R	R	R	R	R
		Reset:	0	0	0	0	0	0	0	0
\$0054	TIMB Counter Modulo Register High (TBMODH) See page 241.	Read:	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
		Write:								
		Reset:	1	1	1	1	1	1	1	1
U = Unaffected X = Indeterminate			R	= Reserved		Bold	= Buffered		= Unimplemented	

Figure 2-2. Control, Status, and Data Registers (Sheet 7 of 10)

Section 5. Configuration Register (CONFIG)

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5.2 Introduction

This section describes the configuration register (CONFIG).

The CONFIG registers contain bits that configure these options:

- Resets caused by the low-voltage inhibit (LVI) module
- Power to the LVI module
- Computer operating properly (COP) module
- Top-side pulse-width modulator (PWM) polarity
- Bottom-side PWM polarity
- Edge-aligned versus center-aligned PWMs
- Six independent PWMs versus three complementary PWM pairs
- STOP instruction enable

7.6.1 Interrupts

At the beginning of an interrupt, the CPU saves the CPU register contents on the stack and sets the interrupt mask (I bit) to prevent additional interrupts. At the end of an interrupt, the return from interrupt (RTI) instruction recovers the CPU register contents from the stack so that normal processing can resume. [Figure 7-8](#) shows interrupt entry timing. [Figure 7-10](#) shows interrupt recovery timing.

Interrupts are latched, and arbitration is performed in the SIM at the start of interrupt processing. The arbitration result is a constant that the CPU uses to determine which vector to fetch. Once an interrupt is latched by the SIM, no other interrupt can take precedence, regardless of priority, until the latched interrupt is serviced (or the I bit is cleared). See [Figure 7-9](#).

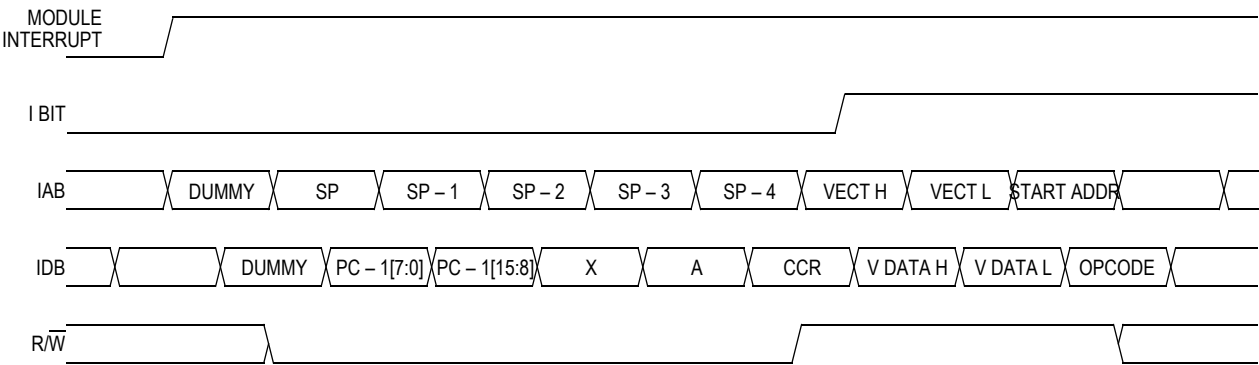


Figure 7-8. Interrupt Entry

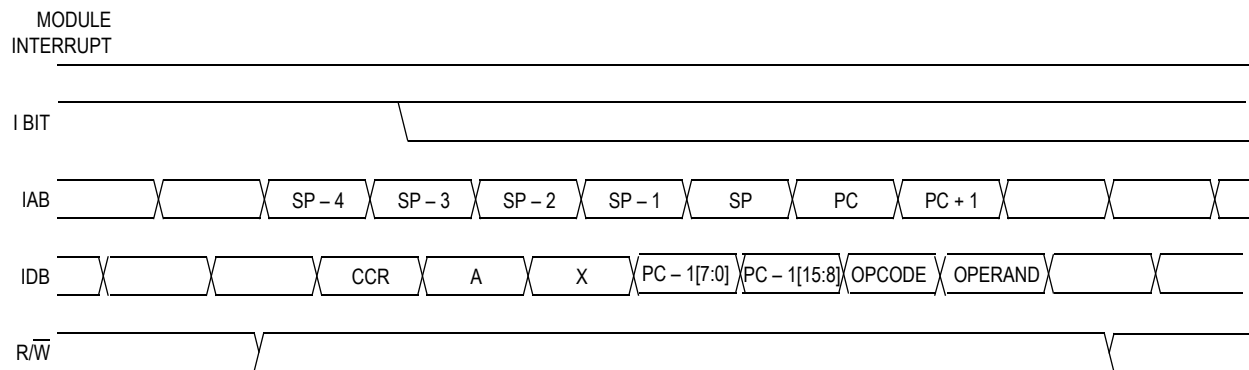


Figure 7-10. Interrupt Recovery

7.6.1.1 Hardware Interrupts

A hardware interrupt does not stop the current instruction. Processing of a hardware interrupt begins after completion of the current instruction. When the current instruction is complete, the SIM checks all pending hardware interrupts. If interrupts are not masked (I bit clear in the condition code register), and if the corresponding interrupt enable bit is set, the SIM proceeds with interrupt processing; otherwise, the next instruction is fetched and executed.

If more than one interrupt is pending at the end of an instruction execution, the highest priority interrupt is serviced first. [Figure 7-11](#) demonstrates what happens when two interrupts are pending. If an interrupt is pending upon exit from the original interrupt service routine, the pending interrupt is serviced before the LDA instruction is executed.

The LDA opcode is prefetched by both the INT1 and INT2 RTI instructions. However, in the case of the INT1 RTI prefetch, this is a redundant operation.

NOTE: *To maintain compatibility with the M6805 Family, the H register is not pushed on the stack during interrupt entry. If the interrupt service routine modifies the H register or uses the indexed addressing mode, software should save the H register and then restore it prior to exiting the routine.*

8.6.3 PLL Programming Register

The PLL programming register (PPG) contains the programming information for the modulo feedback divider and the programming information for the hardware configuration of the VCO.

Address: \$005E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	MUL7	MUL6	MUL5	MUL4	VRS7	VRS6	VRS5	VRS4
Write:								
Reset:	0	1	1	0	0	1	1	0

Figure 8-7. PLL Programming Register (PPG)

MUL[7:4] — Multiplier Select Bits

These read/write bits control the modulo feedback divider that selects the VCO frequency multiplier, N. See [8.4.2.1 PLL Circuits](#) and [8.4.2.4 Programming the PLL](#). A value of \$0 in the multiplier select bits configures the modulo feedback divider the same as a value of \$1. Reset initializes these bits to \$6 to give a default multiply value of 6.

Table 8-1. VCO Frequency Multiplier (N) Selection

MUL7:MUL6:MUL5:MUL4	VCO Frequency Multiplier (N)
0000	1
0001	1
0010	2
0011	3
↓	↓
1101	13
1110	14
1111	15

NOTE: The multiplier select bits have built-in protection that prevents them from being written when the PLL is on (PLLON = 1).

This equation does not always yield a commonly available capacitor size, so round to the nearest available size. If the value is between two different sizes, choose the higher value for better stability. Choosing the lower size may seem attractive for acquisition time improvement, but the PLL can become unstable. Also, always choose a capacitor with a tight tolerance (± 20 percent or better) and low dissipation.

8.11.4 Reaction Time Calculation

The actual acquisition and lock times can be calculated using the equations here. These equations yield nominal values under these conditions:

- Correct selection of filter capacitor, C_F ; see [8.11.3 Choosing a Filter Capacitor](#)
- Room temperature operation
- Negligible external leakage on CGMXFC
- Negligible noise

The K factor in the equations is derived from internal PLL parameters. K_{ACQ} is the K factor when the PLL is configured in acquisition mode, and K_{TRK} is the K factor when the PLL is configured in tracking mode. See [8.4.2.2 Acquisition and Tracking Modes](#).

$$t_{ACQ} = \left(\frac{V_{DDA}}{f_{RDV}} \right) \left(\frac{8}{K_{ACQ}} \right)$$

$$t_{AL} = \left(\frac{V_{DDA}}{f_{RDV}} \right) \left(\frac{4}{K_{TRK}} \right)$$

$$t_{Lock} = t_{ACQ} + t_{AL}$$

NOTE: *Inverse proportionality between the lock time and the reference frequency*

In automatic bandwidth control mode, the acquisition and lock times are quantized into units based on the reference frequency, see [8.4.2.3 Manual and Automatic PLL Bandwidth Modes](#). A certain number of clock cycles, n_{ACQ} , is required to ascertain that the PLL is within the tracking mode entry tolerance, Δ_{TRK} , before exiting acquisition mode. A

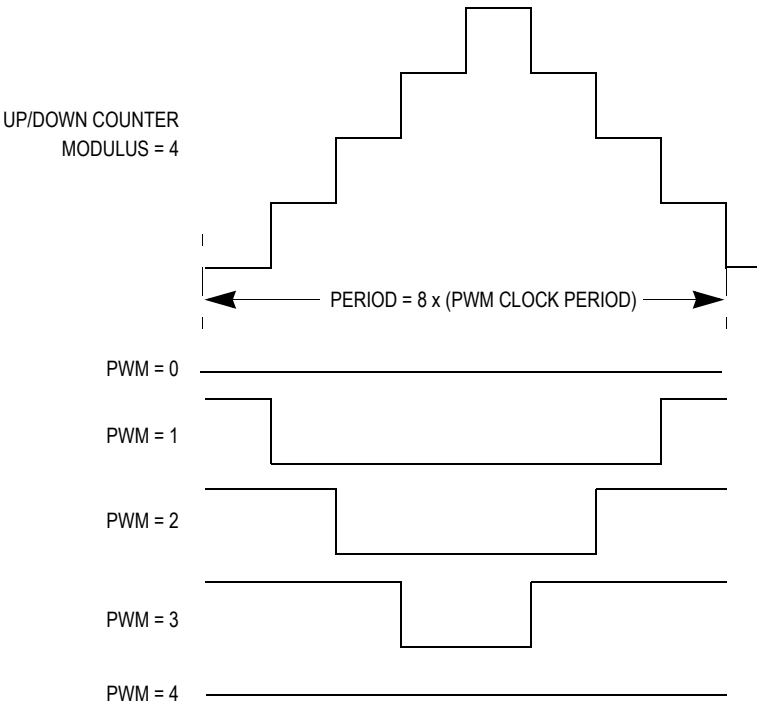


Figure 9-3. Center-Aligned PWM (Positive Polarity)

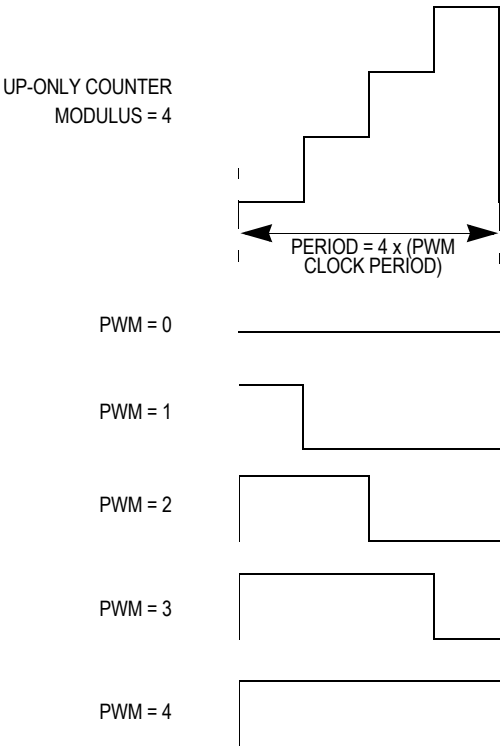


Figure 9-4. Edge-Aligned PWM (Positive Polarity)

9.12 Control Logic Block

This subsection provides a description of the control logic block.

9.12.1 PWM Counter Registers

The PWM counter registers (PCNTH and PCNTL) display the 12-bit up/down or up-only counter. When the high byte of the counter is read, the lower byte is latched. PCNTL will hold this latched value until it is read.

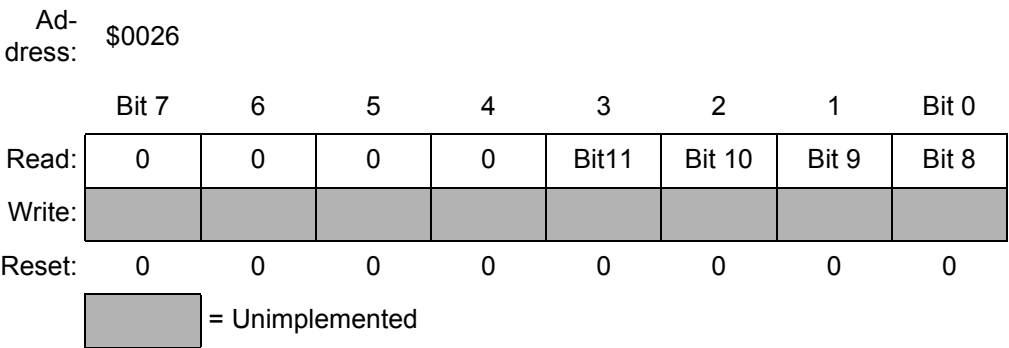


Figure 9-29. PWM Counter Register High (PCNTH)

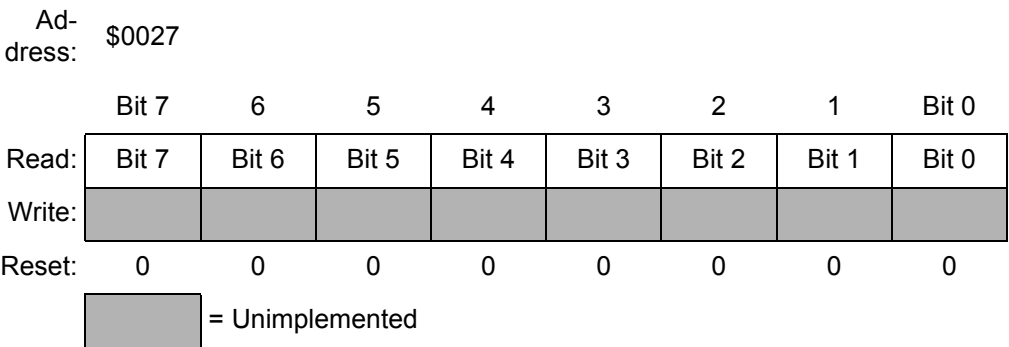


Figure 9-30. PWM Counter Register Low (PCNTL)

12.4.3.2 Buffered Output Compare

Channels 0 and 1 can be linked to form a buffered output compare channel whose output appears on the PTB5/TCH0B pin. The TIMB channel registers of the linked pair alternately control the output.

Setting the MS0B bit in TIMB channel 0 status and control register (TBSC0) links channel 0 and channel 1. The output compare value in the TIMB channel 0 registers initially controls the output on the PTB5/TCH0B pin. Writing to the TIMB channel 1 registers enables the TIMB channel 1 registers to synchronously control the output after the TIMB overflows. At each subsequent overflow, the TIMB channel registers (0 or 1) that control the output are the ones written to last. TSC0 controls and monitors the buffered output compare function, and TIMB channel 1 status and control register (TBSC1) is unused. While the MS0B bit is set, the channel 1 pin, PTB6/TCH1B, is available as a general-purpose input/output (I/O) pin.

NOTE: *In buffered output compare operation, do not write new output compare values to the currently active channel registers. User software should track the currently active channel to prevent writing a new value to the active channel. Writing to the active channel registers is the same as generating unbuffered output compares.*

12.4.4 Pulse-Width Modulation (PWM)

By using the toggle-on-overflow feature with an output compare channel, the TIMB can generate a PWM signal. The value in the TIMB counter modulo registers determines the period of the PWM signal. The channel pin toggles when the counter reaches the value in the TIMB counter modulo registers. The time between overflows is the period of the PWM signal.

As [Figure 12-3](#) shows, the output compare value in the TIMB channel registers determines the pulse width of the PWM signal. The time between overflow and output compare is the pulse width. Program the TIMB to clear the channel pin on output compare if the state of the PWM pulse is logic 1. Program the TIMB to set the pin if the state of the PWM pulse is logic 0.

Use these methods to synchronize unbuffered changes in the PWM pulse width on channel x:

- When changing to a shorter pulse width, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current pulse. The interrupt routine has until the end of the PWM period to write the new value.
- When changing to a longer pulse width, enable TIMB overflow interrupts and write the new value in the TIMB overflow interrupt routine. The TIMB overflow interrupt occurs at the end of the current PWM period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same PWM period.

NOTE: *In PWM signal generation, do not program the PWM channel to toggle on output compare. Toggling on output compare prevents reliable 0 percent duty cycle generation and removes the ability of the channel to self-correct in the event of software error or noise. Toggling on output compare also can cause incorrect PWM signal generation when changing the PWM pulse width to a new, much larger value.*

12.4.4.2 Buffered PWM Signal Generation

Channels 0 and 1 can be linked to form a buffered PWM channel whose output appears on the PTB5/TCH0B pin. The TIMB channel registers of the linked pair alternately control the pulse width of the output.

Setting the MS0B bit in TIMB channel 0 status and control register (TBSC0) links channel 0 and channel 1. The TIMB channel 0 registers initially control the pulse width on the PTB5/TCH0B pin. Writing to the TIMB channel 1 registers enables the TIMB channel 1 registers to synchronously control the pulse width at the beginning of the next PWM period. At each subsequent overflow, the TIMB channel registers (0 or 1) that control the pulse width are the ones written to last. TBSC0 controls and monitors the buffered PWM function, and TIMB channel 1 status and control register (TBSC1) is unused. While the MS0B bit is set, the channel 1 pin, PTB6/TCH1B, is available as a general-purpose I/O pin.

Serial Communications Interface (SCI)

Ad-
dress: \$003A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R8	T8	0	0	ORIE	NEIE	FEIE	PEIE
Write:	R		R	R				
Reset:	U	U	0	0	0	0	0	0

R = Reserved
 U = Unaffected

Figure 13-9. SCI Control Register 3 (SCC3)

R8 — Received Bit 8

When the SCI is receiving 9-bit characters, R8 is the read-only ninth bit (bit 8) of the received character. R8 is received at the same time that the SCDR receives the other 8 bits.

When the SCI is receiving 8-bit characters, R8 is a copy of the eighth bit (bit 7). Reset has no effect on the R8 bit.

T8 — Transmitted Bit 8

When the SCI is transmitting 9-bit characters, T8 is the read/write ninth bit (bit 8) of the transmitted character. T8 is loaded into the transmit shift register at the same time that the SCDR is loaded into the transmit shift register. Reset has no effect on the T8 bit.

ORIE — Receiver Overrun Interrupt Enable Bit

This read/write bit enables SCI error CPU interrupt requests generated by the receiver overrun bit, OR.

- 1 = SCI error CPU interrupt requests from OR bit enabled
- 0 = SCI error CPU interrupt requests from OR bit disabled

NEIE — Receiver Noise Error Interrupt Enable Bit

This read/write bit enables SCI error CPU interrupt requests generated by the noise error bit, NE. Reset clears NEIE.

- 1 = SCI error CPU interrupt requests from NE bit enabled
- 0 = SCI error CPU interrupt requests from NE bit disabled

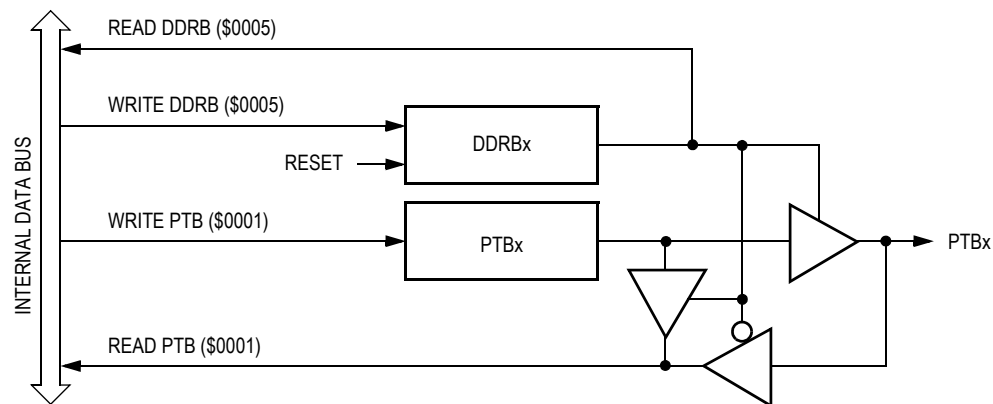


Figure 14-7. Port B I/O Circuit

When bit $DDRBx$ is a logic 1, reading address \$0001 reads the $PTBx$ data latch. When bit $DDRBx$ is a logic 0, reading address \$0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. [Table 14-2](#) summarizes the operation of the port B pins.

Table 14-2. Port B Pin Functions

DDRB Bit	PTB Bit	I/O Pin Mode	Accesses to DDRB	Accesses to PTB	
			Read/Write	Read	Write
0	X ⁽¹⁾	Input, Hi-Z ⁽²⁾	DDRB[6:0]	Pin	PTB[6:0] ⁽³⁾
1	X	Output	DDRB[6:0]	PTB[6:0]	PTB[6:0]

1. X = don't care
2. Hi-Z = high impedance
3. Writing affects data register, but does not affect input.

14.5 Port C

Port C is a 2-bit special-purpose I/O port sharing its pins with the pulse width modulator for motor control module (PMC) FAULT input pins. These two pins mirror the state of FAULT1 and FAULT4 pins. Level changes on these input pins will be interpreted as fault conditions.

The port C data register contains a data latch for each of the two port pins.

15.7 Monitor Mode

The COP is disabled in monitor mode when $V_{DD} + V_{HI}$ is present on the IRQ pin or on the RST pin.

15.8 Wait Mode

The WAIT instruction puts the MCU in low power-consumption standby mode.

The COP continues to operate during wait mode.

15.9 Stop Mode

Stop mode turns off the COP prescaler clock. Service the COP immediately before entering or after exiting stop mode to ensure a full COP timeout period after entering or exiting stop mode.

15.10 COP Module During Break Mode

The COP is disabled during a break interrupt when $V_{DD} + V_{HI}$ is present on the RST pin.

Low-Voltage Inhibit (LVI)

With the LVIPWR bit in the configuration register programmed to logic 1, the LVI module is active after a STOP instruction.

With the LVIRST bit in the configuration register programmed to logic 1, the LVI module can generate a reset and bring the MCU out of stop mode.



21.7 Memory Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
RAM data retention voltage	V_{RDR}	1.3	—	—	V
FLASH program bus clock frequency	—	1	—	—	MHz
FLASH read bus clock frequency	$f_{Read}^{(1)}$	32k	—	8.4M	Hz
FLASH page erase time	$t_{Erase}^{(2)}$	1	—	—	ms
FLASH mass erase time	$t_{MErase}^{(3)}$	4	—	—	ms
FLASH PGM/ERASE to HVEN set up time	t_{nvs}	10	—	—	μ s
FLASH high-voltage hold time	t_{nvh}	5	—	—	μ s
FLASH high-voltage hold time (mass erase)	t_{nvhl}	100	—	—	μ s
FLASH program hold time	t_{pgs}	5	—	—	μ s
FLASH program time	t_{PROG}	30	—	40	μ s
FLASH return to read time	$t_{rcv}^{(4)}$	1	—	—	μ s
FLASH cumulative program HV period	$t_{HV}^{(5)}$	—	—	4	ms
FLASH row erase endurance ⁽⁶⁾	—	10k	100k ⁽⁷⁾	—	Cycles
FLASH row program endurance ⁽⁸⁾	—	10k	100k ⁽⁷⁾	—	Cycles
FLASH data retention time ⁽⁹⁾	—	10	100 ⁽¹⁰⁾	—	Years

Notes:

- f_{Read} is defined as the frequency range for which the FLASH memory can be read.
- If the page erase time is longer than t_{Erase} (Min), there is no erase-disturb, but it reduces the endurance of the FLASH memory.
- If the mass erase time is longer than t_{MErase} (Min), there is no erase-disturb, but it reduces the endurance of the FLASH memory.
- t_{rcv} is defined as the time it needs before the FLASH can be read after turning off the high voltage charge pump, by clearing HVEN to logic 0.
- t_{HV} is defined as the cumulative high voltage programming time to the same row before next erase.
 t_{HV} must satisfy this condition: $t_{nvs} + t_{nvh} + t_{pgs} + (t_{PROG} \times 64) \leq t_{HV} \text{ max.}$
- The minimum row endurance value specifies each row of the FLASH memory is guaranteed to work for at least this many erase / program cycles.
- FLASH endurance is a function of the temperature at which erasure occurs. Typical endurance degrades when the temperature while erasing is less than 25°C.
- The minimum row endurance value specifies each row of the FLASH memory is guaranteed to work for at least this many erase / program cycles.
- The FLASH is guaranteed to retain data over the entire operating temperature range for at least the minimum time specified.
- Freescall performs reliability testing for data retention. These tests are based on samples tested at elevated temperatures. Due to the higher activation energy of the elevated test temperature, calculated life tests correspond to more than 100 years of operation/storage at 55°C



Ordering Information