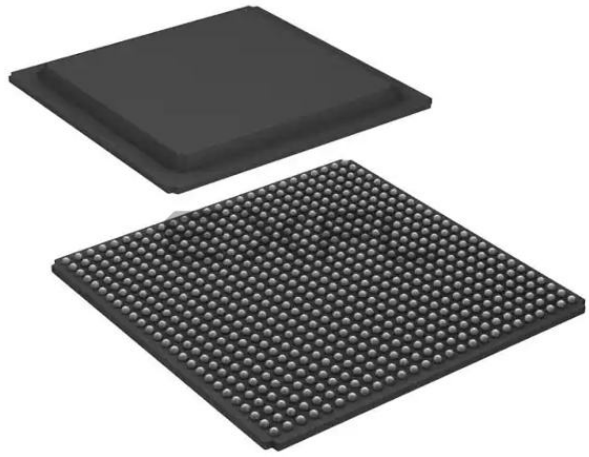

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	2816
Number of Logic Elements/Cells	25344
Total RAM Bits	589824
Number of I/O	502
Number of Gates	1400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1400an-4fg676c

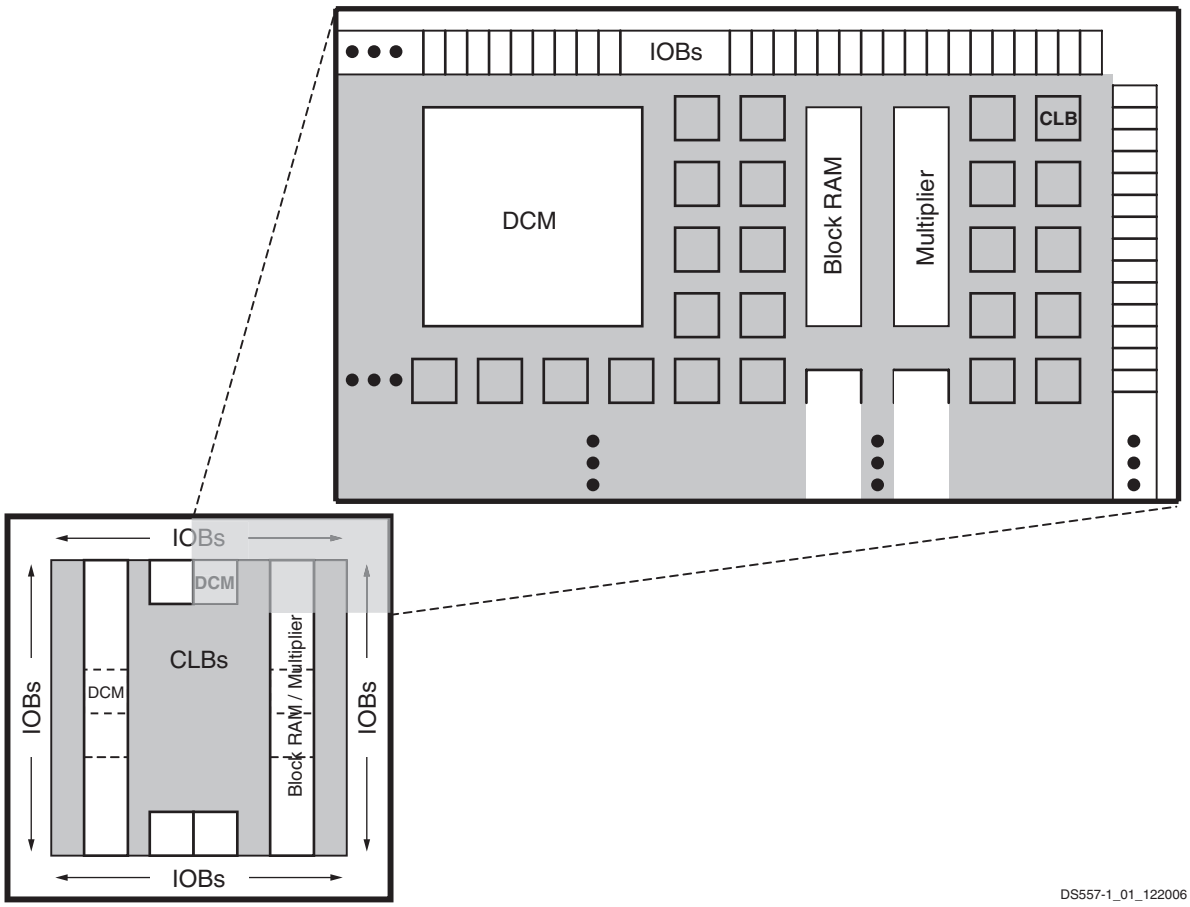
Architectural Overview

The Spartan-3AN FPGA architecture is compatible with that of the Spartan-3A FPGA. The architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. They support a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S50AN, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S50AN has DCMs only at the top, while the XC3S700AN and XC3S1400AN add two DCMs in the middle of the two columns of block RAM and multipliers.

The Spartan-3AN FPGA features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3S700AN and XC3S1400AN have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S50AN has only two DCMs at the top and only one Block RAM/Multiplier column.

Figure 1: **Spartan-3AN Family Architecture**

Pb and Pb-Free Packaging

Spartan-3AN FPGAs are available in both leaded (Pb) and Pb-free packaging options (see Table 5). The Pb-free packages are available for all devices and include a 'G' character in the ordering code. Leaded (non-Pb-free) packages are available for selected devices. The ordering code for the leaded devices does not have an extra 'G'. Leaded and Pb-free devices have the same pin-out.

Table 5: **Pb and Pb-Free Package Options**

Pins			144		256		400		484		676	
Type			TQFP		FTBGA		FBGA		FBGA		FBGA	
Material			Pb-Free	Pb	Pb-Free	Pb	Pb-Free	Pb	Pb-Free	Pb	Pb-Free	Pb
Device	Speed	Range	TQG144	TQ144	FTG256	FT256	FGG400	FG400	FGG484	FG484	FGG676	FG676
XC3S50AN	-4	C, I	✔	SCD4100(1)	✔	✔						
	-5	C	✔	Note 2	✔	✔						
XC3S200AN	-4	C, I			✔	✔						
	-5	C			✔	✔						
XC3S400AN	-4	C, I			✔	✔	✔	✔				
	-5	C			✔	✔	✔	Note 2				
XC3S700AN	-4	C, I							✔	✔		
	-5	C							✔	Note 2		
XC3S1400AN	-4	C, I							✔	✔	✔	✔
	-5	C							✔	✔	✔	Note 2

Notes:

1. To order a Pb package for the XC3S50AN -4 option, append SCD4100 to the part number (XC3S50AN-4TQ144C4100).
2. For Pb packaging for these options, contact your Xilinx sales representative.

Table 15: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards *(Cont'd)***

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}[2]		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
DIFF_SSTL3_II[8]	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the "Using I/O Resources" chapter in UG331.
4. See External Termination Requirements for Differential I/O, page 22.
5. LVPECL is supported on inputs only, not outputs. Requires V_{CCAUX} = 3.3V ± 10%.
6. LVPECL_33 maximum $V_{ICM} = V_{CCAUX} - (V_{ID} / 2)$
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. $(V_{CCAUX} - 300\ mV) \leq V_{ICM} \leq (V_{CCAUX} - 37\ mV)$
8. V_{REF} inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The V_{REF} settings are the same as for the single-ended versions in Table 13. Other differential standards do not use V_{REF}.
9. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the "Using I/O Resources" chapter in UG331.

Differential Output Pairs

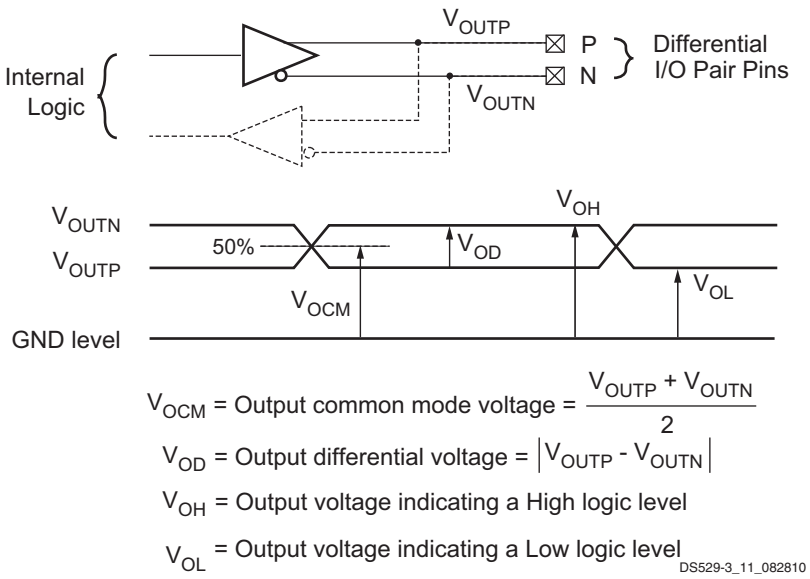


Figure 7: **Differential Output Voltages**

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

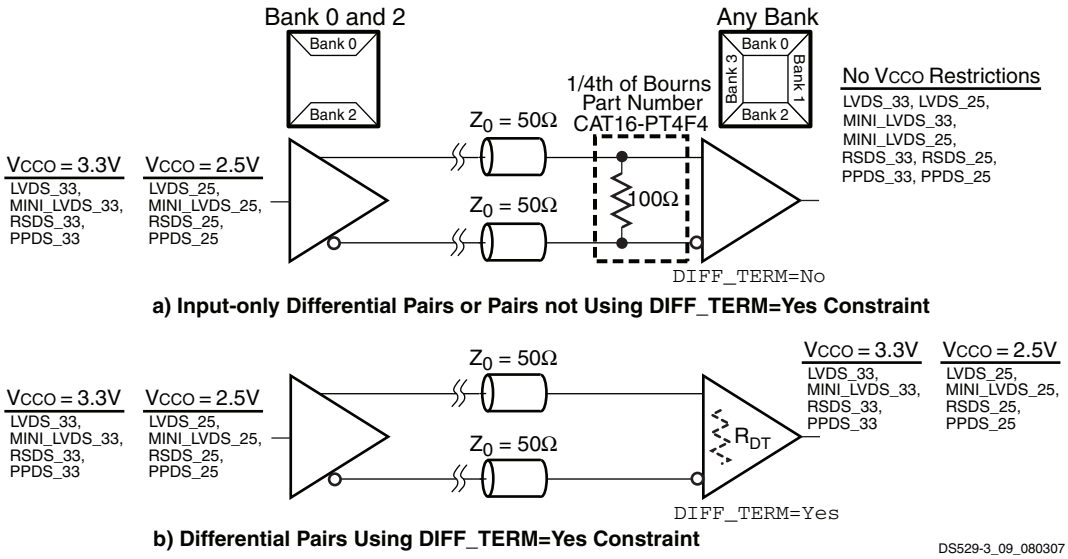


Figure 8: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

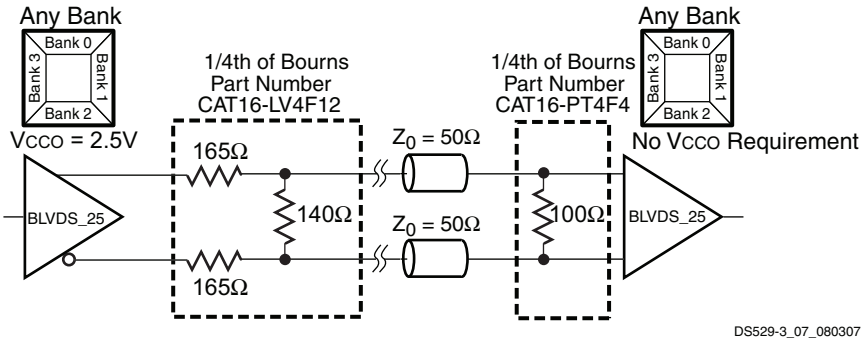


Figure 9: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

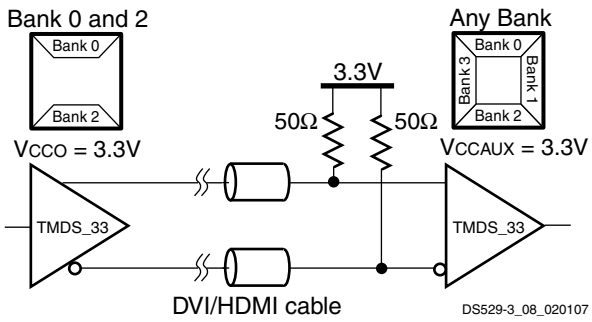


Figure 10: **External Input Resistors Required for TMDS_33 I/O Standard**

Switching Characteristics

All Spartan-3AN FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document are designated as Preview, Advance, Preliminary, or Production, as shown in Table 19. Each category is defined as follows:

Preview: These specifications are based on estimates only and should not be used for timing analysis.

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGA designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

In some cases, a particular family member (and speed grade) is released to Production at a different time than when the speed file is released with the Production label. Any labeling discrepancies are corrected in subsequent speed file releases. See Table 19 for devices that can be considered to have the Production label.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3AN devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

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Timing parameters and their representative values are selected for inclusion either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3AN speed files (v1.41), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 19. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 19: **Spartan-3AN Family v1.41 Speed Grade Designations**

Device	Preview	Advance	Preliminary	Production
XC3S50AN				-4, -5
XC3S200AN				-4, -5
XC3S400AN				-4, -5
XC3S700AN				-4, -5
XC3S1400AN				-4, -5

Table 20 provides the recent history of the Spartan-3AN speed files.

Table 20: **Spartan-3AN Speed File Version History**

Version	ISE Release	Description
1.41	ISE 10.1.03	Updated for Spartan-3A family. No change to data for Spartan-3AN family.
1.40	ISE 10.1.02	Updated for Spartan-3A family. No change to data for Spartan-3AN family.
1.39	ISE 10.1	Updated for Spartan-3A family. No change to data for Spartan-3AN family.
1.38	ISE 9.2.03i	Updated to Production. No change to data.
1.37	ISE 9.2.01i	Updated pin-to-pin setup and hold times, TMDS output adjustment, multiplier setup/hold times, and block RAM clock width.
1.36	ISE 9.2i	Added -5 speed grade, updated to Advance.
1.34	ISE 9.1.03i	Updated pin-to-pin timing.
1.32	ISE 9.1.01i	Preview speed files for -4 speed grade.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 21: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, with DCM(3)	XC3S50AN	3.18	3.42	ns
			XC3S200AN	3.21	3.27	ns
			XC3S400AN	2.97	3.33	ns
			XC3S700AN	3.39	3.50	ns
			XC3S1400AN	3.51	3.99	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, without DCM	XC3S50AN	4.59	5.02	ns
			XC3S200AN	4.88	5.24	ns
			XC3S400AN	4.68	5.12	ns
			XC3S700AN	4.97	5.34	ns
			XC3S1400AN	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 26. If the latter is true, *add* the appropriate Output adjustment from Table 29.
3. DCM output jitter is included in all measurements.

Output Propagation Times

Table 27: **Timing for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
T_{IOCKP}	When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.87	3.13	ns
Propagation Times						
T_{IOOP}	The time it takes for data to travel from the IOB's O input to the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	2.78	2.91	ns
Set/Reset Times						
T_{IOSRP}	Time from asserting the OFF's SR input to setting/resetting data at the Output pin	LVCMOS25(2), 12 mA output drive, Fast slew rate	All	3.63	3.89	ns
T_{IOGSRQ}	Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin			8.62	9.65	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 29.

Table 29: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26(3)	2.26(3)	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns

Table 29: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns

Block RAM Timing

Table 38: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{RCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.06	–	2.49	ns
Setup Times						
T_{RCCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.32	–	0.36	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.28	–	0.31	–	ns
T_{RCCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.69	–	0.77	–	ns
T_{RCCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.12	–	1.26	–	ns
Hold Times						
T_{RCKC_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCKD_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCKC_ENB}	Hold time on the EN input after the active transition at the CLK input	0	–	0	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0	–	0	–	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.56	–	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.56	–	1.79	–	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency	0	320	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10.

Configuration Clock (CCLK) Characteristics

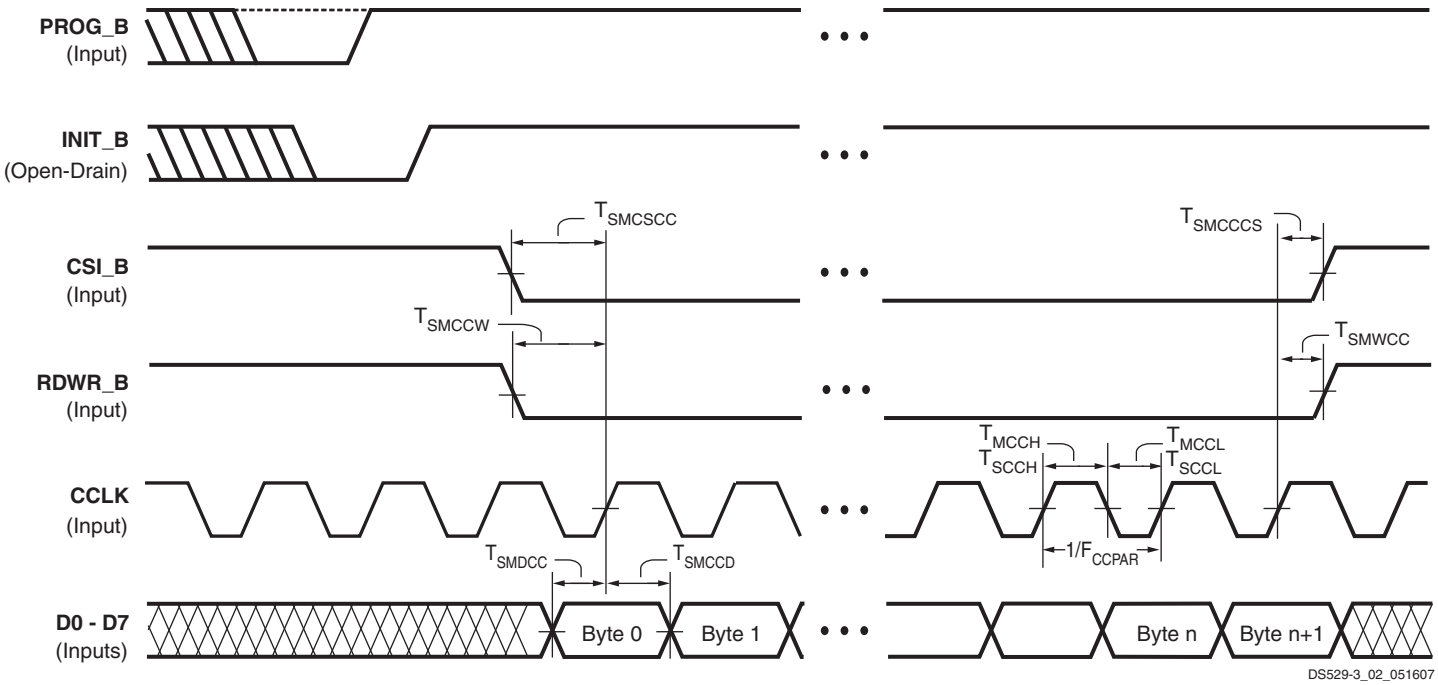
Table 51: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting[1]	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T_{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T_{CCLK6}		6 (*default*)	Commercial	207	417	ns
			Industrial	195		ns
T_{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T_{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T_{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T_{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T_{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T_{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T_{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T_{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T_{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T_{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T_{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T_{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
$T_{CCLK100}$		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0–D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0–D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See UG332, Chapter 7, section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 15: **Waveforms for Slave Parallel Configuration**

Table 56: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}(2)	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		15	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1.0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10.
2. Some Xilinx documents refer to Parallel modes as SelectMAP modes.

TQG144: 144-lead Thin Quad Flat Package

The XC3S50AN is available in the 144-lead thin quad flat package, TQG144.

Table 68 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type (as defined in Table 62). The XC3S50AN does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 68: **Spartan-3AN TQG144 Pinout**

Bank	Pin Name	Pin	Type
0	IO_0	P142	I/O
0	IO_L01N_0	P111	I/O
0	IO_L01P_0	P110	I/O
0	IO_L02N_0	P113	I/O
0	IO_L02P_0/VREF_0	P112	VREF
0	IO_L03N_0	P117	I/O
0	IO_L03P_0	P115	I/O
0	IO_L04N_0	P116	I/O
0	IO_L04P_0	P114	I/O
0	IO_L05N_0	P121	I/O
0	IO_L05P_0	P120	I/O
0	IO_L06N_0/GCLK5	P126	GCLK
0	IO_L06P_0/GCLK4	P124	GCLK
0	IO_L07N_0/GCLK7	P127	GCLK
0	IO_L07P_0/GCLK6	P125	GCLK
0	IO_L08N_0/GCLK9	P131	GCLK
0	IO_L08P_0/GCLK8	P129	GCLK
0	IO_L09N_0/GCLK11	P132	GCLK
0	IO_L09P_0/GCLK10	P130	GCLK
0	IO_L10N_0	P135	I/O
0	IO_L10P_0	P134	I/O
0	IO_L11N_0	P139	I/O
0	IO_L11P_0	P138	I/O
0	IO_L12N_0/PUDC_B	P143	DUAL
0	IO_L12P_0/VREF_0	P141	VREF
0	IP_0	P140	INPUT
0	IP_0/VREF_0	P123	VREF
0	VCCO_0	P119	VCCO
0	VCCO_0	P136	VCCO
1	IO_1	P79	I/O
1	IO_L01N_1/LDC2	P78	DUAL
1	IO_L01P_1/HDC	P76	DUAL
1	IO_L02N_1/LDC0	P77	DUAL

Table 68: **Spartan-3AN TQG144 Pinout *(Cont'd)***

Bank	Pin Name	Pin	Type
1	IO_L02P_1/LDC1	P75	DUAL
1	IO_L03N_1	P84	I/O
1	IO_L03P_1	P82	I/O
1	IO_L04N_1/RHCLK1	P85	RHCLK
1	IO_L04P_1/RHCLK0	P83	RHCLK
1	IO_L05N_1/TRDY1/RHCLK3	P88	RHCLK
1	IO_L05P_1/RHCLK2	P87	RHCLK
1	IO_L06N_1/RHCLK5	P92	RHCLK
1	IO_L06P_1/RHCLK4	P90	RHCLK
1	IO_L07N_1/RHCLK7	P93	RHCLK
1	IO_L07P_1/IRDY1/RHCLK6	P91	RHCLK
1	IO_L08N_1	P98	I/O
1	IO_L08P_1	P96	I/O
1	IO_L09N_1	P101	I/O
1	IO_L09P_1	P99	I/O
1	IO_L10N_1	P104	I/O
1	IO_L10P_1	P102	I/O
1	IO_L11N_1	P105	I/O
1	IO_L11P_1	P103	I/O
1	IP_1/VREF_1	P80	VREF
1	IP_1/VREF_1	P97	VREF
1	VCCO_1	P86	VCCO
1	VCCO_1	P95	VCCO
2	IO_2/MOSI/CSI_B	P62	DUAL
2	IO_L01N_2/M0	P38	DUAL
2	IO_L01P_2/M1	P37	DUAL
2	IO_L02N_2/CSO_B	P41	DUAL
2	IO_L02P_2/M2	P39	DUAL
2	IO_L03N_2/VS1	P44	DUAL
2	IO_L03P_2/RDWR_B	P42	DUAL
2	IO_L04N_2/VS0	P45	DUAL
2	IO_L04P_2/VS2	P43	DUAL
2	IO_L05N_2/D7	P48	DUAL

TQG144 Footprint

Note: Pin 1 indicator in top-left corner and logo orientation.

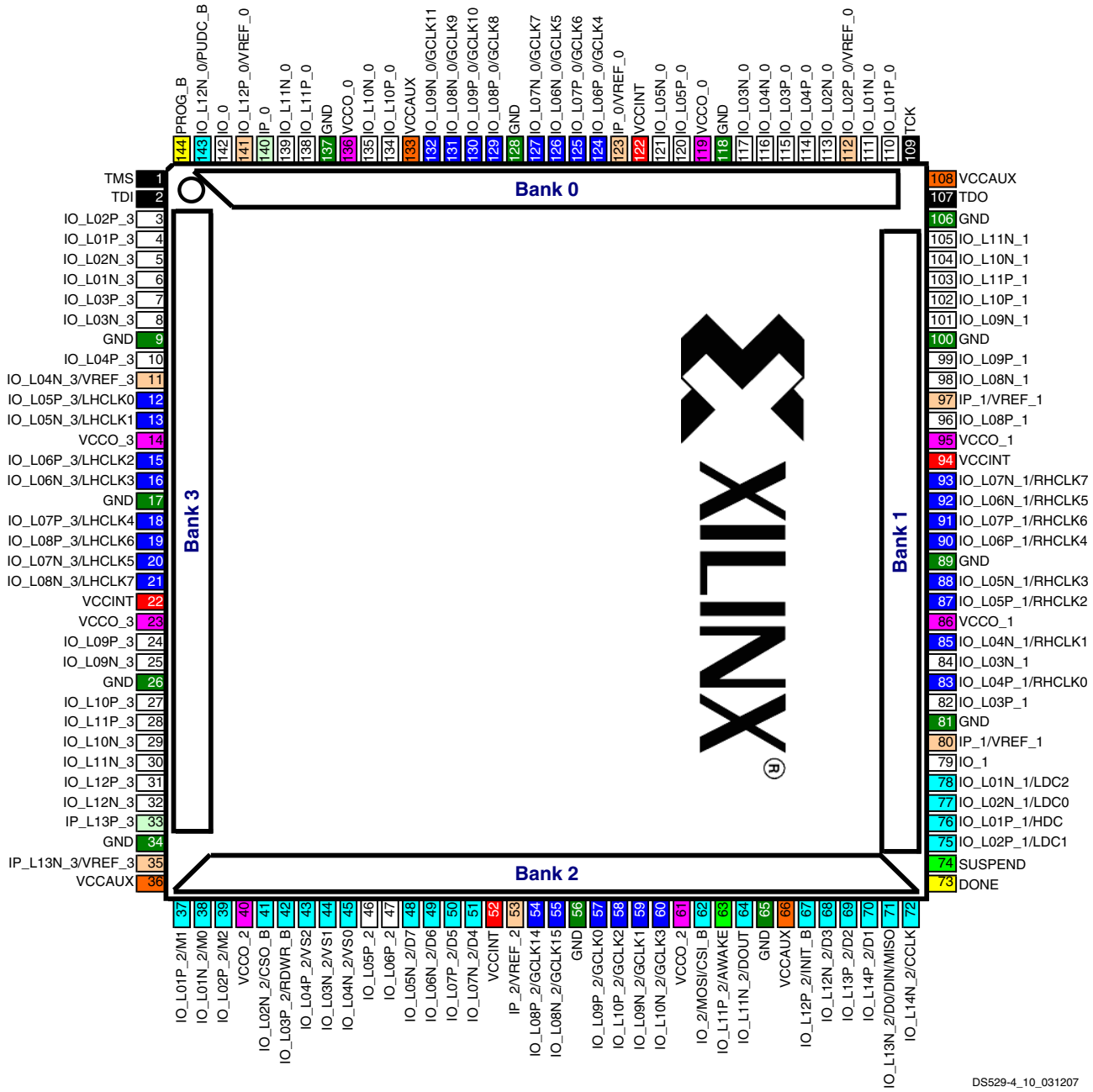


Figure 19: **XC3S50AN FPGA in TQG144 Package Footprint (Top View)**

42	**I/O:** Unrestricted, general-purpose user I/O	25	**DUAL:** Configuration pins, then possible user I/O	8	**VREF:** User I/O or input voltage reference for bank
2	**INPUT:** Unrestricted, general-purpose input pin	30	**CLK:** User I/O, input, or global buffer input	8	**VCCO:** Output voltage supply for bank
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core supply voltage (+1.2V)
0	**N.C.:** Not connected	13	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage
2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins				

Table 70: **Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN) *(Cont'd)***

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
1	IO_L10P_1	IO_L10P_1/A8	J12	DUAL
1	IO_L11N_1/RHCLK1	IO_L11N_1/RHCLK1	K14	RHCLK
1	IO_L11P_1/RHCLK0	IO_L11P_1/RHCLK0	K15	RHCLK
1	IO_L12N_1/TRDY1/RHCLK3	IO_L12N_1/TRDY1/RHCLK3	J16	RHCLK
1	IO_L12P_1/RHCLK2	IO_L12P_1/RHCLK2	K16	RHCLK
1	IO_L14N_1/RHCLK5	IO_L14N_1/RHCLK5	H14	RHCLK
1	IO_L14P_1/RHCLK4	IO_L14P_1/RHCLK4	J14	RHCLK
1	IO_L15N_1/RHCLK7	IO_L15N_1/RHCLK7	H16	RHCLK
1	IO_L15P_1/IRDY1/RHCLK6	IO_L15P_1/IRDY1/RHCLK6	H15	RHCLK
1	N.C.	IO_L16N_1/A11	F16	DUAL
1	N.C.	IO_L16P_1/A10	G16	DUAL
1	N.C.	IO_L17N_1/A13	G14	DUAL
1	N.C.	IO_L17P_1/A12	H13	DUAL
1	N.C.	IO_L18N_1/A15	F15	DUAL
1	N.C.	IO_L18P_1/A14	E16	DUAL
1	N.C.	IO_L19N_1/A17	F14	DUAL
1	N.C.	IO_L19P_1/A16	G13	DUAL
1	IO_L20N_1	IO_L20N_1/A19	F13	DUAL
1	IO_L20P_1	IO_L20P_1/A18	E14	DUAL
1	IO_L22N_1	IO_L22N_1/A21	D15	DUAL
1	IO_L22P_1	IO_L22P_1/A20	D16	DUAL
1	IO_L23N_1	IO_L23N_1/A23	D14	DUAL
1	IO_L23P_1	IO_L23P_1/A22	E13	DUAL
1	IO_L24N_1	IO_L24N_1/A25	C15	DUAL
1	IO_L24P_1	IO_L24P_1/A24	C16	DUAL
1	IP_L04N_1/VREF_1	IP_L04N_1/VREF_1	K12	VREF
1	IP_L04P_1	IP_L04P_1	K11	INPUT
1	N.C.	IP_L09N_1	J11	INPUT
1	N.C.	IP_L09P_1/VREF_1	J10	VREF
1	IP_L13N_1	IP_L13N_1	H11	INPUT
1	IP_L13P_1	IP_L13P_1	H10	INPUT
1	IP_L21N_1	IP_L21N_1	G11	INPUT
1	IP_L21P_1/VREF_1	IP_L21P_1/VREF_1	G12	VREF
1	IP_L25N_1	IP_L25N_1	F11	INPUT
1	IP_L25P_1/VREF_1	IP_L25P_1/VREF_1	F12	VREF
1	VCCO_1	VCCO_1	E15	VCCO
1	VCCO_1	VCCO_1	H12	VCCO
1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	N15	VCCO

Footprint Migration Differences

Unconnected Balls on XC3S50AN

Table 73 summarizes any footprint and functionality differences between the XC3S50AN and the XC3S200AN or XC3S400AN devices for migration between these devices in the FTG256 package. The XC3S200AN and XC3S400AN have identical pinouts. The XC3S50AN pinout is compatible with the XC3S200AN and XC3S400AN, however, there are 51 unconnected balls and one functionally different ball. Generally, designs migrate upward from the XC3S50AN to either the XC3S200AN or XC3S400AN. If using differential I/O, see Table 74. If using the BPI configuration mode (parallel Flash), see Table 75.

In Table 73, the arrow (→) indicates that this pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

Table 73: **FTG256 XC3S50AN Footprint Migration/Differences**

FTG256 Ball	Bank	XC3S50AN	Migration	XC3S200AN or XC3S400AN
A7	0	N.C.	→	I/O
A12	0	N.C.	→	I/O
B12	0	INPUT	→	I/O
C7	0	N.C.	→	I/O
D10	0	N.C.	→	I/O
E2	3	N.C.	→	I/O
E3	3	N.C.	→	I/O
E7	0	N.C.	→	I/O/VREF
E10	0	N.C.	→	I/O/VREF
E16	1	N.C.	→	I/O
F3	3	N.C.	→	I/O
F8	0	N.C.	→	I/O
F14	1	N.C.	→	I/O
F15	1	N.C.	→	I/O
F16	1	N.C.	→	I/O
G3	3	N.C.	→	I/O
G4	3	N.C.	→	I/O
G5	3	N.C.	→	INPUT/VREF
G6	3	N.C.	→	INPUT
G13	1	N.C.	→	I/O
G14	1	N.C.	→	I/O
G16	1	N.C.	→	I/O
H4	3	N.C.	→	I/O
H5	3	N.C.	→	I/O
H6	3	N.C.	→	I/O
H13	1	N.C.	→	I/O
J4	3	N.C.	→	I/O
J6	3	N.C.	→	I/O
J10	1	N.C.	→	INPUT/VREF
J11	1	N.C.	→	INPUT
K4	3	N.C.	→	I/O

FTG256 Footprint (XC3S50AN)

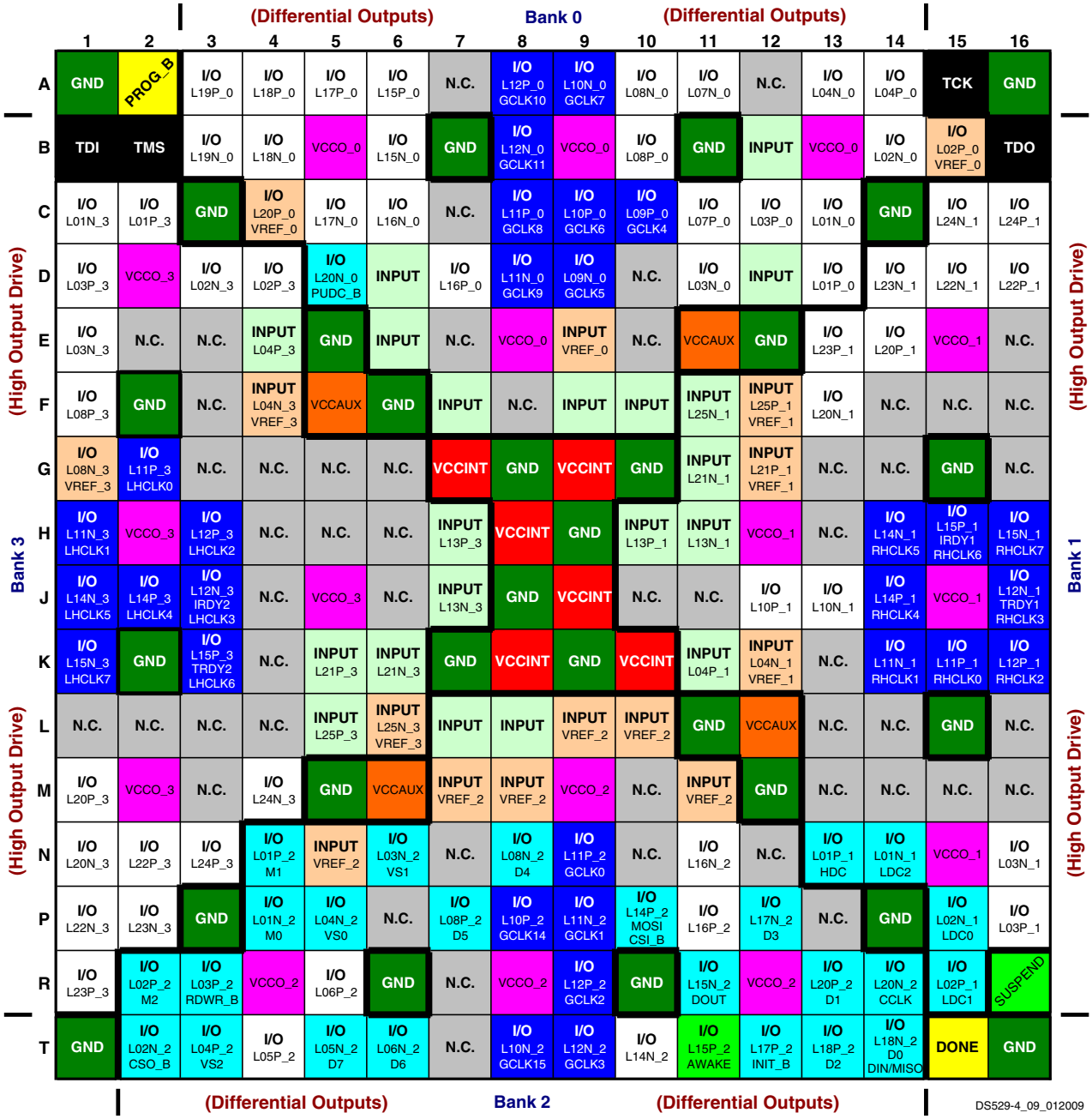


Figure 20: **XC3S50AN FTG256 Package Footprint (Top View)**

53	**I/O:** Unrestricted, general-purpose user I/O	25	**DUAL:** Configuration pins, then possible user I/O	15	**VREF:** User I/O or input voltage reference for bank	2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
20	**INPUT:** Unrestricted, general-purpose input pin	30	**CLK:** User I/O, input, or global buffer input	16	**VCCO:** Output voltage supply for bank		
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)		
51	**N.C.:** Not connected (XC3S50AN only)	28	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage		

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
2	VCCO_2	AA13	VCCO
2	VCCO_2	AA18	VCCO
2	VCCO_2	AA5	VCCO
2	VCCO_2	AA9	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	U9	VCCO
3	IO_L01N_3	D2	I/O
3	IO_L01P_3	C1	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	E4	I/O
3	IO_L03P_3	D3	I/O
3	IO_L05N_3	G5	I/O
3	IO_L05P_3	G6	I/O
3	IO_L06N_3	E1	I/O
3	IO_L06P_3	D1	I/O
3	IO_L07N_3	E3	I/O
3	IO_L07P_3	F4	I/O
3	IO_L08N_3	G4	I/O
3	IO_L08P_3	F3	I/O
3	IO_L09N_3	H6	I/O
3	IO_L09P_3	H5	I/O
3	IO_L10N_3	J5	I/O
3	IO_L10P_3	K6	I/O
3	IO_L12N_3	F1	I/O
3	IO_L12P_3	F2	I/O
3	IO_L13N_3	G1	I/O
3	IO_L13P_3	G3	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	H4	I/O
3	IO_L16N_3	H1	I/O
3	IO_L16P_3	H2	I/O
3	IO_L17N_3/VREF_3	J1	VREF
3	IO_L17P_3	J3	I/O
3	IO_L18N_3	K4	I/O
3	IO_L18P_3	K5	I/O
3	IO_L20N_3	K2	I/O
3	IO_L20P_3	K3	I/O
3	IO_L21N_3/LHCLK1	L3	LHCLK
3	IO_L21P_3/LHCLK0	L5	LHCLK

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
3	IO_L22N_3/IRDY2/LHCLK3	L1	LHCLK
3	IO_L22P_3/LHCLK2	K1	LHCLK
3	IO_L24N_3/LHCLK5	M2	LHCLK
3	IO_L24P_3/LHCLK4	M1	LHCLK
3	IO_L25N_3/LHCLK7	M4	LHCLK
3	IO_L25P_3/TRDY2/LHCLK6	M3	LHCLK
3	IO_L26N_3	N3	I/O
3	IO_L26P_3/VREF_3	N1	VREF
3	IO_L28N_3	P2	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P5	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	M5	I/O
3	IO_L32N_3	R2	I/O
3	IO_L32P_3	R1	I/O
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	R3	I/O
3	IO_L34N_3	T4	I/O
3	IO_L34P_3	R5	I/O
3	IO_L36N_3	T3	I/O
3	IO_L36P_3/VREF_3	T1	VREF
3	IO_L37N_3	U2	I/O
3	IO_L37P_3	U1	I/O
3	IO_L38N_3	V3	I/O
3	IO_L38P_3	V1	I/O
3	IO_L40N_3	U5	I/O
3	IO_L40P_3	T5	I/O
3	IO_L41N_3	U4	I/O
3	IO_L41P_3	U3	I/O
3	IO_L42N_3	W2	I/O
3	IO_L42P_3	W1	I/O
3	IO_L43N_3	W3	I/O
3	IO_L43P_3	V4	I/O
3	IO_L44N_3	Y2	I/O
3	IO_L44P_3	Y1	I/O
3	IO_L45N_3	AA2	I/O
3	IO_L45P_3	AA1	I/O
3	IP_3/VREF_3	J8	VREF
3	IP_3/VREF_3	R6	VREF

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
3	IP_L58N_3/VREF_3	AA5	VREF
3	IP_L58P_3	AA4	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IP_L66P_3	AE1	INPUT
3	VCCO_3	AB2	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	W5	VCCO
GND	GND	A1	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND
GND	GND	A26	GND
GND	GND	AA1	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	AD3	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD24	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	C3	GND
GND	GND	C9	GND

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
GND	GND	C14	GND
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	J24	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND

User I/Os by Bank

Table 83 indicates how the 502 available user-I/O pins are distributed between the four I/O banks on the FGG676 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 83: **User I/Os Per Bank for the XC3S1400AN in the FGG676 Package**

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	120	82	20	1	9	8
Right	1	130	67	15	30	10	8
Bottom	2	120	67	14	21	10	8
Left	3	132	97	18	0	9	8
Total		**502**	**313**	**67**	**52**	**38**	**32**

Footprint Migration Differences

The XC3S1400AN is the only Spartan-3AN FPGA offered in the FGG676 package. The XC3S1400AN FPGA is pin compatible with the Spartan-3A XC3S1400A FPGA in the FG(G)676 package, although the Spartan-3A FPGA requires an external configuration source.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device. Noted that family is available in Pb-free packages only.
09/12/07	2.0.1	Minor updates to text.
09/24/07	2.1	Update thermal characteristics in Table 67.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that non-Pb-free packages may be available for selected devices. Updated thermal characteristics in Table 67. Updated links.
06/02/08	3.1	Add Package Overview section. Removed VREF and INPUT designations and diamond symbols on unconnected N.C. pins for XC3S700AN FGG484 in Table 78 and Figure 22 and for XC3S1400AN FGG676 in Table 82 and Figure 23.
11/19/09	3.2	Renamed package 'Footprint Area' to 'Body Area' throughout document. Noted in Introduction that references to Pb-free package code also apply to the Pb package. Added Pb packages to Table 65 and Table 66. Changed Body Area of TQ144/TQG144 packages in Table 65. Corrected bank designation for SUSPEND to VCCAUX. Noted that non-Pb-free (Pb) packages are available for selected devices. Updated Table 79 and Figure 22 for I/O vs. Input pin counts.
12/02/10	4.0	Upgraded Notice of Disclaimer.
04/01/11	4.1	Updated the CLK description in Table 62. In Table 64, added device/package combinations for the XC3S50AN and XC3S400AN in the FT(G)256 package and the XC3S1400AN in the FG(G)484 package. In Table 65, updated the maximum I/Os for the FG484/FGG484 packages, removed the Mass column, and updated Note 1. In Table 65, changed the FTG256 link from PK115_FTG256, FGG676 link from PK111_FGG676, and the TQG144 link from PK126_TQG144. Completely replaced the section FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array with new information on the added device/package combinations and new figures and tables. Revised U16, U7, and T8 in Table 78. Added Table 80 and Table 81 and updated Figure 23.