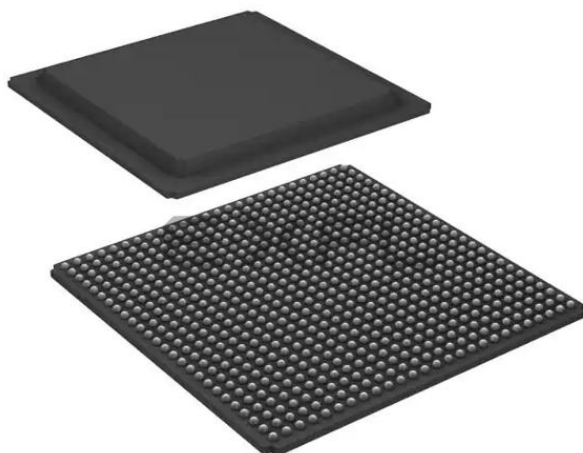




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	2816
Number of Logic Elements/Cells	25344
Total RAM Bits	589824
Number of I/O	502
Number of Gates	1400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1400an-4fg676i

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 21: Pin-to-Pin Clock-to-Output Times for the IOB Output Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
T _{ICKOFDCM}	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate, with DCM ⁽³⁾	XC3S50AN	3.18	3.42	ns
			XC3S200AN	3.21	3.27	ns
			XC3S400AN	2.97	3.33	ns
			XC3S700AN	3.39	3.50	ns
			XC3S1400AN	3.51	3.99	ns
T _{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate, without DCM	XC3S50AN	4.59	5.02	ns
			XC3S200AN	4.88	5.24	ns
			XC3S400AN	4.68	5.12	ns
			XC3S700AN	4.97	5.34	ns
			XC3S1400AN	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 30](#) and are based on the operating conditions set forth in [Table 10](#) and [Table 13](#).
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from [Table 26](#). If the latter is true, *add* the appropriate Output adjustment from [Table 29](#).
3. DCM output jitter is included in all measurements.

Table 25: Propagation Times for the IOB Input Path (Cont'd)

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T _{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	5	XC3S1400AN	3.17	3.52	ns
			6		3.52	3.92	ns
			7		3.82	4.18	ns
			8		4.10	4.57	ns
			9		3.84	4.31	ns
			10		4.20	4.79	ns
			11		4.46	5.06	ns
			12		4.87	5.51	ns
			13		5.07	5.73	ns
			14		5.43	6.08	ns
			15		5.73	6.33	ns
			16		6.01	6.77	ns
T _{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25 ⁽²⁾	IFD_DELAY_VALUE=0	XC3S50AN	1.70	1.81	ns
				XC3S200AN	1.85	2.04	ns
				XC3S400AN	1.44	1.74	ns
				XC3S700AN	1.48	1.74	ns
				XC3S1400AN	1.50	1.97	ns

Table 32: Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair

Signal Standard (IOSTANDARD)		Package Type			
		TQG144		FTG256, FGG400, FGG484, FGG676	
		Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
Single-Ended Standards					
LVTTTL	Slow	2	20	20	60
		4	10	10	41
		6	10	10	29
		8	6	6	22
		12	6	6	13
		16	5	5	11
		24	4	4	9
	Fast	2	10	10	10
		4	6	6	6
		6	5	5	5
		8	3	3	3
		12	3	3	3
		16	3	3	3
		24	2	2	2
	QuietIO	2	40	40	80
		4	24	24	48
		6	20	20	36
		8	16	16	27
		12	12	12	16
		16	9	9	13
		24	9	9	12

Table 32: Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair (Cont'd)

Signal Standard (IOSTANDARD)		Package Type			
		TQG144		FTG256, FGG400, FGG484, FGG676	
		Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
LVCMOS33	Slow	2	24	24	76
		4	14	14	46
		6	11	11	27
		8	10	10	20
		12	9	9	13
		16	8	8	10
		24	—	8	—
	Fast	2	10	10	10
		4	8	8	8
		6	5	5	5
		8	4	4	4
		12	4	4	4
		16	2	2	2
		24	—	2	—
	QuietIO	2	36	36	76
		4	32	32	46
		6	24	24	32
		8	16	16	26
		12	16	16	18
		16	12	12	14
		24	—	10	—

18 x 18 Embedded Multiplier Timing

Table 37: 18 x 18 Embedded Multiplier Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T _{MULT}	Combinational multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	–	4.36	–	4.88	ns
Clock-to-Output Times						
T _{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register ^(2,3)	–	0.84	–	1.30	ns
T _{MSCKP_A} T _{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register ^(2,4)	–	4.44	–	4.97	ns
Setup Times						
T _{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽³⁾	3.56	–	3.98	–	ns
T _{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register ⁽⁴⁾	0.00	–	0.00	–	ns
T _{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register ⁽⁴⁾	0.00	–	0.00	–	ns
Hold Times						
T _{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽³⁾	0.00	–	0.00	–	ns
T _{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register ⁽⁴⁾	0.35	–	0.45	–	ns
T _{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register ⁽⁴⁾	0.35	–	0.45	–	ns
Clock Frequency						
F _{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register ⁽⁵⁾	0	280	0	250	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 10](#).
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. The PREG register is typically used when inferring a single-stage multiplier.
4. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.
5. Combinational delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.

Table 42: Switching Characteristics for the DFS

Symbol	Description	Device	Speed Grade				Units	
			-5		-4			
			Min	Max	Min	Max		
Output Frequency Ranges								
CLKOUT_FREQ_FX	Frequency for the CLKFX and CLKFX180 outputs	All	5	350	5	320	MHz	
Output Clock Jitter (2)(3)								
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	CLKIN ≤ 20 MHz	All	Typ	Max	Typ	Max	
			Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip				ps	
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(4)(5)								
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion	All	—	±[1% of CLKFX period + 350]	—	±[1% of CLKFX period + 350]	ps	
Phase Alignment(5)								
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used	All	—	±200	—	±200	ps	
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used	All	—	±[1% of CLKFX period + 200]	—	±[1% of CLKFX period + 200]	ps	
Lock Time								
LOCK_FX(2)	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F _{CLKIN} ≤ 15 MHz	All	—	5	—	5	ms
		F _{CLKIN} > 15 MHz		—	450	—	450	μs

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 10 and Table 41.
- For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
- Maximum output jitter is characterized within a reasonable noise environment (40 SSOs and 25% CLB switching) on an XC3S1400A FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
- The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
- Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of “±[1% of CLKFX period + 200]”. Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Configuration Clock (CCLK) Characteristics

Table 51: Master Mode CCLK Output Period by *ConfigRate* Option Setting

Symbol	Description	ConfigRate Setting ⁽¹⁾	Temperature Range	Minimum	Maximum	Units
T _{CCLK1}	CCLK clock period by ConfigRate setting	1 <i>(power-on value)</i>	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T _{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T _{CCLK6}		6 <i>(default)</i>	Commercial	207	417	ns
			Industrial	195		ns
T _{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T _{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T _{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T _{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T _{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T _{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T _{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T _{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T _{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T _{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T _{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T _{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
T _{CCLK100}		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the *ConfigRate* option value when generating a configuration bitstream.

Table 52: Master Mode CCLK Output Frequency by ConfigRate Option Setting

Symbol	Description	ConfigRate Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ConfigRate setting	1 (power-on value)	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F_{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F_{CCLK6}		6 (default)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F_{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F_{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F_{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F_{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F_{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F_{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F_{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F_{CCLK25}		25	Commercial	10.00	20.90	MHz
			Industrial		22.23	MHz
F_{CCLK27}		27	Commercial	10.80	22.39	MHz
			Industrial		23.81	MHz
F_{CCLK33}		33	Commercial	13.20	27.48	MHz
			Industrial		29.23	MHz
F_{CCLK44}		44	Commercial	17.60	37.60	MHz
			Industrial		40.00	MHz
F_{CCLK50}		50	Commercial	20.00	44.80	MHz
			Industrial		47.66	MHz
$F_{CCLK100}$		100	Commercial	40.00	88.68	MHz
			Industrial		94.34	MHz

Table 53: Master Mode CCLK Output Minimum Low and High Time

Symbol	Description		ConfigRate Setting																Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T _{MCCL} , T _{MCCH}	Master Mode CCLK	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
	Minimum Low and High Time	Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Introduction

This section describes how the various pins on a Spartan®-3AN FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331:

- **UG331: Spartan-3 Generation FPGA User Guide**
http://www.xilinx.com/support/documentation/user_guides/ug331.pdf

Spartan-3AN FPGAs are available in Pb-free, RoHS packages, indicated by a “G” in the middle of the package code. Lead (Pb) packages are available for selected devices, with the same pinout and without the “G” in the ordering code (see [Table 5, page 7](#)). The Pb-free package code can be selected in the software for the Pb packages since the pinouts are identical. References to the Pb-free package code in this document apply also to the Pb package.

Pin Types

Most pins on a Spartan-3AN FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3AN FPGA packages, as outlined in [Table 62](#). In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 62: Types of Pins on Spartan-3AN FPGAs

Type with Color Code	Description	Pin Name(s) in Type ⁽¹⁾
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI™ clamp diode.	IP_# IP_Lxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN DOUT CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxx_#/VREF_# IO/VREF_# IO_Lxx_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are all devices in the TQG144 package and the XC3S50AN in the FTG256 package. The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: Spartan-3 Generation FPGA User Guide for additional information on these signals.	IO_Lxx_#/GCLK[15:0], IO_Lxx_#/LHCLK[7:0], IO_Lxx_#/RHCLK[7:0]

FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FTG256, supports the XC3S50AN, XC3S200AN, and XC3S400AN devices. Table 70 lists all the package pins for these devices. They are sorted by bank number and then by the pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The differential I/O pairs that have different assignments between the XC3S50AN and the XC3S200AN or XC3S400AN are highlighted in light blue in Table 70. See Footprint Migration Differences, page 87 for additional information. The table also shows the pin number for each pin and the pin type (as defined in Table 62).

The footprints for the XC3S200AN and XC3S400AN in the FTG256 are identical. Figure 21 shows the common footprint for the XC3S200AN and XC3S400AN. The XC3S50AN footprint is compatible with the XC3S200AN and XC3S400AN, however, there are 51 unconnected balls (indicated as N.C. in Table 70).

Table 73 summarizes the XC3S50AN FPGA footprint migration differences for the FTG256 package.

The XC3S50AN does not support the address output pins for the byte-wide peripheral interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 70: Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN)

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
0	IO_L01N_0	IO_L01N_0	C13	I/O
0	IO_L01P_0	IO_L01P_0	D13	I/O
0	IO_L02N_0	IO_L02N_0	B14	I/O
0	IO_L02P_0/VREF_0	IO_L02P_0/VREF_0	B15	VREF
0	IO_L03N_0	IO_L03N_0	D11	I/O
0	IO_L03P_0	IO_L03P_0	C12	I/O
0	IO_L04N_0	IO_L04N_0	A13	I/O
0	IO_L04P_0	IO_L04P_0	A14	I/O
0	N.C.	IO_L05N_0	A12	I/O
0	IP_0	IO_L05P_0	B12	I/O
0	N.C.	IO_L06N_0/VREF_0	E10	VREF
0	N.C.	IO_L06P_0	D10	I/O
0	IO_L07N_0	IO_L07N_0	A11	I/O
0	IO_L07P_0	IO_L07P_0	C11	I/O
0	IO_L08N_0	IO_L08N_0	A10	I/O
0	IO_L08P_0	IO_L08P_0	B10	I/O
0	IO_L09N_0/GCLK5	IO_L09N_0/GCLK5	D9	GCLK
0	IO_L09P_0/GCLK4	IO_L09P_0/GCLK4	C10	GCLK
0	IO_L10N_0/GCLK7	IO_L10N_0/GCLK7	A9	GCLK
0	IO_L10P_0/GCLK6	IO_L10P_0/GCLK6	C9	GCLK
0	IO_L11N_0/GCLK9	IO_L11N_0/GCLK9	D8	GCLK
0	IO_L11P_0/GCLK8	IO_L11P_0/GCLK8	C8	GCLK
0	IO_L12N_0/GCLK11	IO_L12N_0/GCLK11	B8	GCLK
0	IO_L12P_0/GCLK10	IO_L12P_0/GCLK10	A8	GCLK
0	N.C.	IO_L13N_0	C7	I/O
0	N.C.	IO_L13P_0	A7	I/O

User I/Os by Bank

Table 71 and Table 72 indicate how the available user-I/O pins are distributed between the four I/O banks on the FTG256 package. The AWAKE pin is counted as a dual-purpose I/O. The XC3S50AN FPGA in the FTG256 package has 51 unconnected balls, labeled with an N.C. type. These pins are also indicated in Figure 20.

Table 71: User I/Os Per Bank on XC3S50AN in the FTG256 Package

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	40	21	7	1	3	8
Right	1	32	12	5	4	3	8
Bottom	2	40	5	2	21	6	6
Left	3	32	15	6	0	3	8
Total		144	53	20	26	15	30

Table 72: User I/Os Per Bank on XC3S200AN and XC3S400AN in the FTG256 Package

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	47	27	6	1	5	8
Right	1	50	1	6	30	5	8
Bottom	2	48	11	2	21	6	8
Left	3	50	30	7	0	5	8
Total		195	69	21	52	21	32

XC3S50AN Differential I/O Alignment Differences

Also, some differential I/O pairs on the XC3S50AN FPGA are aligned differently than the corresponding pairs on the XC3S200AN or XC3S400AN FPGAs, as shown in [Table 74](#). All the mismatched pairs are in I/O Bank 2. The N side of each pair is shaded.

Table 74: Differential I/O Differences in FTG256

FTG256 Ball	Bank	XC3S50AN	XC3S200AN or XC3S400AN
T3	2	IO_L04P_2/VS2	IO_L03N_2/VS2
N6		IO_L03N_2/VS1	IO_L04P_2/VS1
R5		IO_L06P_2	IO_L05N_2
T5		IO_L05N_2/D7	IO_L06P_2/D7
P10		IO_L14P_2/MOSI/CSI_B	IO_L14N_2/MOSI/CSI_B
T10		IO_L14N_2	IO_L14P_2
R13		IO_L20P_2	IO_L18N_2
T14		IO_L18N_2	IO_L20P_2

XC3S50AN Does Not Have BPI Mode Address Outputs

The XC3S50AN FPGA does not generate the BPI-mode address pins during configuration. [Table 75](#) summarizes these differences.

Table 75: XC3S50AN BPI Functional Differences

FTG256 Ball	Bank	XC3S50AN	XC3S200AN or XC3S400AN
N16	1	IO_L03N_1	IO_L03N_1/A1
P16		IO_L03P_1	IO_L03P_1/A0
J13		IO_L10N_1	IO_L10N_1/A9
J12		IO_L10P_1	IO_L10P_1/A8
F13		IO_L20N_1	IO_L20N_1/A19
E14		IO_L20P_1	IO_L20P_1/A18
D15		IO_L22N_1	IO_L22N_1/A21
D16		IO_L22P_1	IO_L22P_1/A20
D14		IO_L23N_1	IO_L23N_1/A23
E13		IO_L23P_1	IO_L23P_1/A22
C15		IO_L24N_1	IO_L24N_1/A25
C16		IO_L24P_1	IO_L24P_1/A24

The Spartan-3AN FPGAs are pin compatible with the same density Spartan-3A FPGAs in the FT(G)256 package, although the Spartan-3A FPGAs require an external configuration source.

Table 76: Spartan-3AN FGG400 Pinout (Cont'd)

Bank	Pin Name	FGG400 Ball	Type
3	IO_L34P_3	U1	I/O
3	IO_L36N_3	T4	I/O
3	IO_L36P_3	R5	I/O
3	IO_L37N_3	V2	I/O
3	IO_L37P_3	V1	I/O
3	IO_L38N_3	W2	I/O
3	IO_L38P_3	W1	I/O
3	IP_3	H7	INPUT
3	IP_L04N_3/VREF_3	G6	VREF
3	IP_L04P_3	G7	INPUT
3	IP_L11N_3/VREF_3	J7	VREF
3	IP_L11P_3	J8	INPUT
3	IP_L15N_3	K7	INPUT
3	IP_L15P_3	K8	INPUT
3	IP_L19N_3	K5	INPUT
3	IP_L19P_3	K6	INPUT
3	IP_L23N_3	L6	INPUT
3	IP_L23P_3	L7	INPUT
3	IP_L27N_3	M7	INPUT
3	IP_L27P_3	M8	INPUT
3	IP_L31N_3	N7	INPUT
3	IP_L31P_3	M6	INPUT
3	IP_L35N_3	N6	INPUT
3	IP_L35P_3	P5	INPUT
3	IP_L39N_3/VREF_3	P7	VREF
3	IP_L39P_3	P6	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	N5	VCCO
3	VCCO_3	U2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A20	GND
GND	GND	B6	GND
GND	GND	B14	GND
GND	GND	C3	GND
GND	GND	C18	GND
GND	GND	D9	GND
GND	GND	E5	GND

Table 76: Spartan-3AN FGG400 Pinout (Cont'd)

Bank	Pin Name	FGG400 Ball	Type
GND	GND	E12	GND
GND	GND	F15	GND
GND	GND	G2	GND
GND	GND	G19	GND
GND	GND	H8	GND
GND	GND	H13	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	K1	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K17	GND
GND	GND	L4	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L20	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P2	GND
GND	GND	P19	GND
GND	GND	R6	GND
GND	GND	R9	GND
GND	GND	T16	GND
GND	GND	U12	GND
GND	GND	V3	GND
GND	GND	V18	GND
GND	GND	W7	GND
GND	GND	W15	GND
GND	GND	Y1	GND
GND	GND	Y10	GND
GND	GND	Y20	GND
VCCAUX	SUSPEND	R15	PWR MGMT
VCCAUX	DONE	W19	CONFIG
VCCAUX	PROG_B	D5	CONFIG
VCCAUX	TCK	A19	JTAG
VCCAUX	TDI	F5	JTAG
VCCAUX	TDO	E17	JTAG

Table 76: Spartan-3AN FGG400 Pinout (Cont'd)

Bank	Pin Name	FGG400 Ball	Type
VCCAUX	TMS	E4	JTAG
VCCAUX	VCCAUX	A13	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	H1	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L8	VCCAUX
VCCAUX	VCCAUX	N20	VCCAUX
VCCAUX	VCCAUX	T5	VCCAUX
VCCAUX	VCCAUX	Y8	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	N10	VCCINT

User I/Os by Bank

Table 77 indicates how the 311 available user-I/O pins are distributed between the four I/O banks on the FGG400 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 77: User I/Os Per Bank for the XC3S400AN in the FGG400 Package

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	77	50	12	1	6	8
Right	1	79	21	12	30	8	8
Bottom	2	76	35	6	21	6	8
Left	3	79	49	16	0	6	8
Total		311	155	46	52	26	32

Footprint Migration Differences

The XC3S400AN is the only Spartan-3AN FPGA offered in the FGG400 package.

The XC3S400AN FPGA is pin compatible with the Spartan-3A XC3S400A FPGA in the FG(G)400 package, although the Spartan-3A FPGA requires an external configuration source.

Table 78: Spartan-3AN FGG484 Pinout (Cont'd)

Bank	Pin Name	FGG484 Ball	Type
3	IP_L04N_3/VREF_3	H7	VREF
3	IP_L04P_3	H8	INPUT
3	IP_L11N_3	K8	INPUT
3	IP_L11P_3	J7	INPUT
3	IP_L15N_3/VREF_3	L8	VREF
3	IP_L15P_3	K7	INPUT
3	IP_L19N_3	M8	INPUT
3	IP_L19P_3	L7	INPUT
3	IP_L23N_3	M6	INPUT
3	IP_L23P_3	M7	INPUT
3	IP_L27N_3	N9	INPUT
3	IP_L27P_3	N8	INPUT
3	IP_L31N_3	N5	INPUT
3	IP_L31P_3	N6	INPUT
3	IP_L35N_3	P8	INPUT
3	IP_L35P_3	N7	INPUT
3	IP_L39N_3	R8	INPUT
3	IP_L39P_3	P7	INPUT
3	IP_L46N_3/VREF_3	T6	VREF
3	IP_L46P_3	R7	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J6	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P6	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA7	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	B7	GND
GND	GND	C20	GND
GND	GND	C3	GND
GND	GND	D14	GND
GND	GND	D9	GND

Table 78: Spartan-3AN FGG484 Pinout (Cont'd)

Bank	Pin Name	FGG484 Ball	Type
GND	GND	F11	GND
GND	GND	F17	GND
GND	GND	F6	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L17	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P10	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	T12	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U17	GND
GND	GND	U6	GND
GND	GND	W10	GND
GND	GND	W14	GND
GND	GND	Y20	GND
GND	GND	Y3	GND
VCCAUX	SUSPEND	U18	PWR MGMT

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
0	IO_L33N_0	B10	I/O
0	IO_L33P_0	A10	I/O
0	IO_L34N_0	D10	I/O
0	IO_L34P_0	C10	I/O
0	IO_L35N_0	H12	I/O
0	IO_L35P_0	G12	I/O
0	IO_L36N_0	B9	I/O
0	IO_L36P_0	A9	I/O
0	IO_L37N_0	D9	I/O
0	IO_L37P_0	E10	I/O
0	IO_L38N_0	B8	I/O
0	IO_L38P_0	A8	I/O
0	IO_L39N_0	K12	I/O
0	IO_L39P_0	J12	I/O
0	IO_L40N_0	D8	I/O
0	IO_L40P_0	C8	I/O
0	IO_L41N_0	C6	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L42P_0	B7	I/O
0	IO_L43N_0	K11	I/O
0	IO_L43P_0	J11	I/O
0	IO_L44N_0	D6	I/O
0	IO_L44P_0	C5	I/O
0	IO_L45N_0	B4	I/O
0	IO_L45P_0	A4	I/O
0	IO_L46N_0	H10	I/O
0	IO_L46P_0	G10	I/O
0	IO_L47N_0	H9	I/O
0	IO_L47P_0	G9	I/O
0	IO_L48N_0	E7	I/O
0	IO_L48P_0	F7	I/O
0	IO_L51N_0	B3	I/O
0	IO_L51P_0	A3	I/O
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L52P_0/VREF_0	F8	VREF
0	IP_0	A5	INPUT
0	IP_0	A7	INPUT
0	IP_0	A13	INPUT
0	IP_0	A17	INPUT

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
0	IP_0	A23	INPUT
0	IP_0	C4	INPUT
0	IP_0	D12	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	E11	INPUT
0	IP_0	E18	INPUT
0	IP_0	E20	INPUT
0	IP_0	F10	INPUT
0	IP_0	G14	INPUT
0	IP_0	G16	INPUT
0	IP_0	H13	INPUT
0	IP_0	H18	INPUT
0	IP_0	J10	INPUT
0	IP_0	J13	INPUT
0	IP_0	J15	INPUT
0	IP_0/VREF_0	D7	VREF
0	IP_0/VREF_0	D14	VREF
0	IP_0/VREF_0	G11	VREF
0	IP_0/VREF_0	J17	VREF
0	N.C.	A24	N.C.
0	N.C.	B24	N.C.
0	N.C.	D5	N.C.
0	N.C.	E9	N.C.
0	N.C.	F18	N.C.
0	N.C.	E6	N.C.
0	N.C.	F9	N.C.
0	N.C.	G18	N.C.
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L04N_1	W21	I/O
1	IO_L04P_1	W20	I/O
1	IO_L05N_1	AC25	I/O
1	IO_L05P_1	AD26	I/O
1	IO_L06N_1	AB26	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L07P_1	AB23	I/O
1	IO_L08N_1	V19	I/O
1	IO_L08P_1	V18	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L10N_1	U20	I/O
1	IO_L10P_1	V21	I/O
1	IO_L11N_1	AA25	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L13P_1	Y22	I/O
1	IO_L14N_1	T20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L15N_1	Y25	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L18N_1	V22	I/O
1	IO_L18P_1	W23	I/O
1	IO_L19N_1	V25	I/O
1	IO_L19P_1	V24	I/O
1	IO_L21N_1	U22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L22N_1	R20	I/O
1	IO_L22P_1	R19	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IO_L23P_1	U23	I/O
1	IO_L25N_1/A3	R22	DUAL

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
1	IO_L25P_1/A2	R21	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L26P_1/A4	T23	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L29P_1/A8	R25	DUAL
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L37N_1	N21	I/O
1	IO_L37P_1	P22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IO_L38P_1/A12	L24	DUAL
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L41N_1	K26	I/O
1	IO_L41P_1	K25	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L42P_1/A16	N20	DUAL
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L45N_1	M22	I/O
1	IO_L45P_1	M21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L50N_1	K21	I/O
1	IO_L50P_1	L22	I/O
1	IO_L51N_1	G24	I/O

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IP_2	AD16	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AF7	INPUT
2	IP_2	Y11	INPUT
2	IP_2/VREF_2	AA9	VREF
2	IP_2/VREF_2	AA20	VREF
2	IP_2/VREF_2	AB6	VREF
2	IP_2/VREF_2	AB10	VREF
2	IP_2/VREF_2	AC10	VREF
2	IP_2/VREF_2	AD12	VREF
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IP_2/VREF_2	AF22	VREF
2	IP_2/VREF_2	Y16	VREF
2	N.C.	AA8	N.C.
2	N.C.	AC5	N.C.
2	N.C.	AC22	N.C.
2	N.C.	AD5	N.C.
2	N.C.	Y18	N.C.
2	N.C.	Y19	N.C.
2	N.C.	AD23	N.C.
2	N.C.	W18	N.C.
2	N.C.	Y8	N.C.
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
3	IO_L01N_3	J9	I/O
3	IO_L01P_3	J8	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	H7	I/O
3	IO_L03P_3	G6	I/O

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L07P_3	E3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L11N_3	F2	I/O
3	IO_L11P_3	E1	I/O
3	IO_L13N_3	J6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L14N_3	F3	I/O
3	IO_L14P_3	G3	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IO_L18N_3	L7	I/O
3	IO_L18P_3	K6	I/O
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28N_3	M6	I/O
3	IO_L28P_3	M5	I/O
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	N5	I/O
3	IO_L31N_3	N2	I/O
3	IO_L31P_3	N1	I/O
3	IO_L32N_3/LHCLK1	N7	LHCLK
3	IO_L32P_3/LHCLK0	N6	LHCLK
3	IO_L33N_3/IRDY2/LHCLK3	P2	LHCLK
3	IO_L33P_3/LHCLK2	P1	LHCLK
3	IO_L34N_3/LHCLK5	P3	LHCLK
3	IO_L34P_3/LHCLK4	P4	LHCLK
3	IO_L35N_3/LHCLK7	P10	LHCLK
3	IO_L35P_3/TRDY2/LHCLK6	N9	LHCLK
3	IO_L36N_3	R2	I/O
3	IO_L36P_3/VREF_3	R1	VREF
3	IO_L37N_3	R4	I/O
3	IO_L37P_3	R3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L38P_3	T3	I/O
3	IO_L39N_3	P6	I/O
3	IO_L39P_3	P7	I/O
3	IO_L40N_3	R6	I/O
3	IO_L40P_3	R5	I/O
3	IO_L41N_3	P9	I/O
3	IO_L41P_3	P8	I/O
3	IO_L42N_3	U4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L43N_3	R9	I/O
3	IO_L43P_3/VREF_3	R10	VREF
3	IO_L44N_3	U2	I/O
3	IO_L44P_3	U1	I/O
3	IO_L45N_3	R7	I/O
3	IO_L45P_3	R8	I/O
3	IO_L47N_3	V2	I/O
3	IO_L47P_3	V1	I/O
3	IO_L48N_3	T9	I/O
3	IO_L48P_3	T10	I/O
3	IO_L49N_3	V5	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L51P_3	T7	I/O

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
3	IO_L52N_3	W4	I/O
3	IO_L52P_3	W3	I/O
3	IO_L53N_3	Y2	I/O
3	IO_L53P_3	Y1	I/O
3	IO_L55N_3	AA3	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L56N_3	U8	I/O
3	IO_L56P_3	U7	I/O
3	IO_L57N_3	Y6	I/O
3	IO_L57P_3	Y5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L61N_3	V8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L65P_3	AD1	I/O
3	IP_L04N_3/VREF_3	C1	VREF
3	IP_L04P_3	C2	INPUT
3	IP_L08N_3	D1	INPUT
3	IP_L08P_3	D2	INPUT
3	IP_L12N_3/VREF_3	H4	VREF
3	IP_L12P_3	G5	INPUT
3	IP_L16N_3	G1	INPUT
3	IP_L16P_3	G2	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IP_L24N_3	K1	INPUT
3	IP_L24P_3	J1	INPUT
3	IP_L46N_3	V4	INPUT
3	IP_L46P_3	U3	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IP_L50P_3	W1	INPUT
3	IP_L54N_3	Y4	INPUT
3	IP_L54P_3	Y3	INPUT

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device. Noted that family is available in Pb-free packages only.
09/12/07	2.0.1	Minor updates to text.
09/24/07	2.1	Update thermal characteristics in Table 67 .
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that non-Pb-free packages may be available for selected devices. Updated thermal characteristics in Table 67 . Updated links.
06/02/08	3.1	Add Package Overview section. Removed VREF and INPUT designations and diamond symbols on unconnected N.C. pins for XC3S700AN FGG484 in Table 78 and Figure 22 and for XC3S1400AN FGG676 in Table 82 and Figure 23 .
11/19/09	3.2	Renamed package 'Footprint Area' to 'Body Area' throughout document. Noted in Introduction that references to Pb-free package code also apply to the Pb package. Added Pb packages to Table 65 and Table 66 . Changed Body Area of TQ144/TQG144 packages in Table 65 . Corrected bank designation for SUSPEND to VCCAUX. Noted that non-Pb-free (Pb) packages are available for selected devices. Updated Table 79 and Figure 22 for I/O vs. Input pin counts.
12/02/10	4.0	Upgraded Notice of Disclaimer .
04/01/11	4.1	Updated the CLK description in Table 62 . In Table 64 , added device/package combinations for the XC3S50AN and XC3S400AN in the FT(G)256 package and the XC3S1400AN in the FG(G)484 package. In Table 65 , updated the maximum I/Os for the FG484/FGG484 packages, removed the Mass column, and updated Note 1. In Table 65 , changed the FTG256 link from PK115_FTG256 , FGG676 link from PK111_FGG676 , and the TQG144 link from PK126_TQG144 . Completely replaced the section FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array with new information on the added device/package combinations and new figures and tables. Revised U16, U7, and T8 in Table 78 . Added Table 80 and Table 81 and updated Figure 23 .

Notice of Disclaimer

THE XILINX HARDWARE FPGA AND CPLD DEVICES REFERRED TO HEREIN ("PRODUCTS") ARE SUBJECT TO THE TERMS AND CONDITIONS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT <http://www.xilinx.com/warranty.htm>. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED IN THE XILINX DATA SHEET. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, OR ANY OTHER APPLICATION THAT INVOKES THE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). USE OF PRODUCTS IN CRITICAL APPLICATIONS IS AT THE SOLE RISK OF CUSTOMER, SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

CRITICAL APPLICATIONS DISCLAIMER

XILINX PRODUCTS (INCLUDING HARDWARE, SOFTWARE AND/OR IP CORES) ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS IN LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, CLASS III MEDICAL DEVICES, NUCLEAR FACILITIES, APPLICATIONS RELATED TO THE DEPLOYMENT OF AIRBAGS, OR ANY OTHER APPLICATIONS THAT COULD LEAD TO DEATH, PERSONAL INJURY OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (INDIVIDUALLY AND COLLECTIVELY, "CRITICAL APPLICATIONS"). FURTHERMORE, XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN ANY APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE OR AIRCRAFT, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR. CUSTOMER AGREES, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE XILINX PRODUCTS, TO THOROUGHLY TEST THE SAME FOR SAFETY PURPOSES. TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN CRITICAL APPLICATIONS.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.