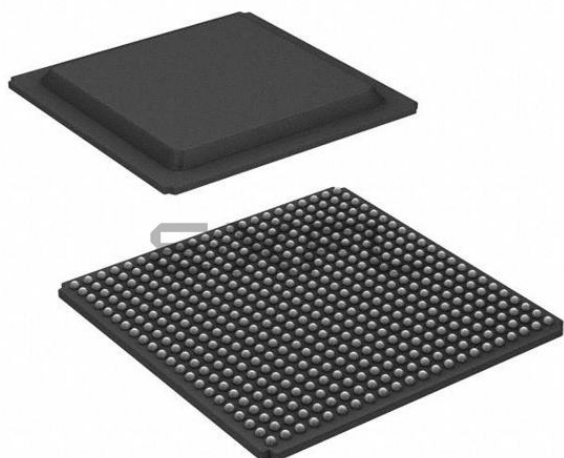




Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	2816
Number of Logic Elements/Cells	25344
Total RAM Bits	589824
Number of I/O	372
Number of Gates	1400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1400an-4fgg484c

Single-Ended I/O Standards

Table 13: Recommended Operating Conditions for User I/Os Using Single-Ended Standards

IOSTANDARD Attribute	V _{CCO} for Drivers ⁽²⁾			V _{REF}			V _{IL}	V _{IH} ⁽³⁾
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V _{REF} is not used for these I/O standards			0.8	2.0
LVC MOS33 ⁽⁴⁾	3.0	3.3	3.6				0.8	2.0
LVC MOS25 ⁽⁴⁾⁽⁵⁾	2.3	2.5	2.7				0.7	1.7
LVC MOS18	1.65	1.8	1.95				0.4	0.8
LVC MOS15	1.4	1.5	1.6				0.4	0.8
LVC MOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3 ⁽⁶⁾	3.0	3.3	3.6				0.3 • V _{CCO}	0.5 • V _{CCO}
PCI66_3 ⁽⁶⁾	3.0	3.3	3.6				0.3 • V _{CCO}	0.5 • V _{CCO}
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	V _{REF} – 0.1	V _{REF} + 0.1
HSTL_III	1.4	1.5	1.6	–	0.9	–	V _{REF} – 0.1	V _{REF} + 0.1
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	V _{REF} – 0.1	V _{REF} + 0.1
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	V _{REF} – 0.1	V _{REF} + 0.1
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	V _{REF} – 0.1	V _{REF} + 0.1
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	V _{REF} – 0.125	V _{REF} + 0.125
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	V _{REF} – 0.125	V _{REF} + 0.125
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38	V _{REF} – 0.150	V _{REF} + 0.150
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38	V _{REF} – 0.150	V _{REF} + 0.150
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	V _{REF} – 0.2	V _{REF} + 0.2
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	V _{REF} – 0.2	V _{REF} + 0.2

Notes:

- Descriptions of the symbols used in this table are as follows:
V_{CCO} – the supply voltage for output drivers
V_{REF} – the reference voltage for setting the input switching threshold
V_{IL} – the input voltage that indicates a Low logic level
V_{IH} – the input voltage that indicates a High logic level
- In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVC MOS25 inputs and for PCI™ I/O standards.
- For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 6.
- There is approximately 100 mV of hysteresis on inputs using LVC MOS33 and LVC MOS25 I/O standards.
- All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVC MOS33 standard. The Dual-Purpose configuration pins use the LVC MOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
- For information on PCI IP solutions, see www.xilinx.com/pci. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

Switching Characteristics

All Spartan-3AN FPGAs ship in two speed grades: -4 and the higher performance -5. Switching characteristics in this document are designated as Preview, Advance, Preliminary, or Production, as shown in Table 19. Each category is defined as follows:

Preview: These specifications are based on estimates only and should not be used for timing analysis.

Advance: These specifications are based on simulations only and are typically available soon after establishing FPGA specifications. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

Preliminary: These specifications are based on complete early silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting preliminary delays is greatly reduced compared to Advance data.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGA designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx® ISE® software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

In some cases, a particular family member (and speed grade) is released to Production at a different time than when the speed file is released with the Production label. Any labeling discrepancies are corrected in subsequent speed file releases. See Table 19 for devices that can be considered to have the Production label.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan-3AN devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Create a Xilinx user account and sign up to receive automatic e-mail notification whenever this data sheet or the associated user guides are updated.

- Sign Up for Alerts

<https://secure.xilinx.com/webreg/register.do?group=myprofile&languageID=1>

Timing parameters and their representative values are selected for inclusion either because they are important as general design requirements or they indicate fundamental device performance characteristics. The Spartan-3AN speed files (v1.41), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 19. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 19: Spartan-3AN Family v1.41 Speed Grade Designations

Device	Preview	Advance	Preliminary	Production
XC3S50AN				-4, -5
XC3S200AN				-4, -5
XC3S400AN				-4, -5
XC3S700AN				-4, -5
XC3S1400AN				-4, -5

Table 20 provides the recent history of the Spartan-3AN speed files.

Table 20: Spartan-3AN Speed File Version History

Version	ISE Release	Description
1.41	ISE 10.1.03	Updated for Spartan-3A family. No change to data for Spartan-3AN family.
1.40	ISE 10.1.02	Updated for Spartan-3A family. No change to data for Spartan-3AN family.
1.39	ISE 10.1	Updated for Spartan-3A family. No change to data for Spartan-3AN family.
1.38	ISE 9.2.03i	Updated to Production. No change to data.
1.37	ISE 9.2.01i	Updated pin-to-pin setup and hold times, TMDS output adjustment, multiplier setup/hold times, and block RAM clock width.
1.36	ISE 9.2i	Added -5 speed grade, updated to Advance.
1.34	ISE 9.1.03i	Updated pin-to-pin timing.
1.32	ISE 9.1.01i	Preview speed files for -4 speed grade.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 21: Pin-to-Pin Clock-to-Output Times for the IOB Output Path

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Max	Max	
Clock-to-Output Times						
T _{ICKOFDCM}	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate, with DCM ⁽³⁾	XC3S50AN	3.18	3.42	ns
			XC3S200AN	3.21	3.27	ns
			XC3S400AN	2.97	3.33	ns
			XC3S700AN	3.39	3.50	ns
			XC3S1400AN	3.51	3.99	ns
T _{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25 ⁽²⁾ , 12 mA output drive, Fast slew rate, without DCM	XC3S50AN	4.59	5.02	ns
			XC3S200AN	4.88	5.24	ns
			XC3S400AN	4.68	5.12	ns
			XC3S700AN	4.97	5.34	ns
			XC3S1400AN	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in [Table 30](#) and are based on the operating conditions set forth in [Table 10](#) and [Table 13](#).
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from [Table 26](#). If the latter is true, *add* the appropriate Output adjustment from [Table 29](#).
3. DCM output jitter is included in all measurements.

Input Propagation Times

Table 25: Propagation Times for the IOB Input Path

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
Propagation Times							
T _{IOPI}	The time it takes for data to travel from the Input pin to the I output with no input delay programmed	LVCMOS25 ⁽²⁾	IBUF_DELAY_VALUE=0	XC3S50AN	1.04	1.12	ns
				XC3S200AN	0.87	0.87	ns
				XC3S400AN	0.65	0.72	ns
				XC3S700AN	0.92	0.92	ns
				XC3S1400AN	0.96	1.21	ns
T _{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	1	XC3S50AN	1.79	2.07	ns
			2		2.13	2.46	ns
			3		2.36	2.71	ns
			4		2.88	3.21	ns
			5		3.11	3.46	ns
			6		3.45	3.84	ns
			7		3.75	4.19	ns
			8		4.00	4.47	ns
			9		3.61	4.11	ns
			10		3.95	4.50	ns
			11		4.18	4.67	ns
			12		4.75	5.20	ns
			13		4.98	5.44	ns
			14		5.31	5.95	ns
			15		5.62	6.28	ns
			16		5.86	6.57	ns
			1	XC3S200AN	1.57	1.65	ns
			2		1.87	1.97	ns
			3		2.16	2.33	ns
			4		2.68	2.96	ns
			5		2.87	3.19	ns
			6		3.20	3.60	ns
			7		3.57	4.02	ns
			8		3.79	4.26	ns
			9		3.42	3.86	ns
			10		3.79	4.25	ns
			11		4.02	4.55	ns
			12		4.62	5.24	ns
			13		4.86	5.53	ns
			14		5.18	5.94	ns

Table 29: Output Timing Adjustments for IOB (Cont'd)

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26 ⁽³⁾	2.26 ⁽³⁾	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns

Table 29: Output Timing Adjustments for IOB (Cont'd)

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns

Configurable Logic Block (CLB) Timing

Table 33: CLB (SLICEM) Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T _{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T _{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T _{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T _{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	0	–	ns
T _{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	–	0	–	ns
Clock Timing						
T _{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T _{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F _{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T _{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T _{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 10](#).

18 x 18 Embedded Multiplier Timing

Table 37: 18 x 18 Embedded Multiplier Timing

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Combinatorial Delay						
T _{MULT}	Combinational multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	–	4.36	–	4.88	ns
Clock-to-Output Times						
T _{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register ^(2,3)	–	0.84	–	1.30	ns
T _{MSCKP_A} T _{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register ^(2,4)	–	4.44	–	4.97	ns
Setup Times						
T _{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽³⁾	3.56	–	3.98	–	ns
T _{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register ⁽⁴⁾	0.00	–	0.00	–	ns
T _{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register ⁽⁴⁾	0.00	–	0.00	–	ns
Hold Times						
T _{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused) ⁽³⁾	0.00	–	0.00	–	ns
T _{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register ⁽⁴⁾	0.35	–	0.45	–	ns
T _{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register ⁽⁴⁾	0.35	–	0.45	–	ns
Clock Frequency						
F _{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register ⁽⁵⁾	0	280	0	250	MHz

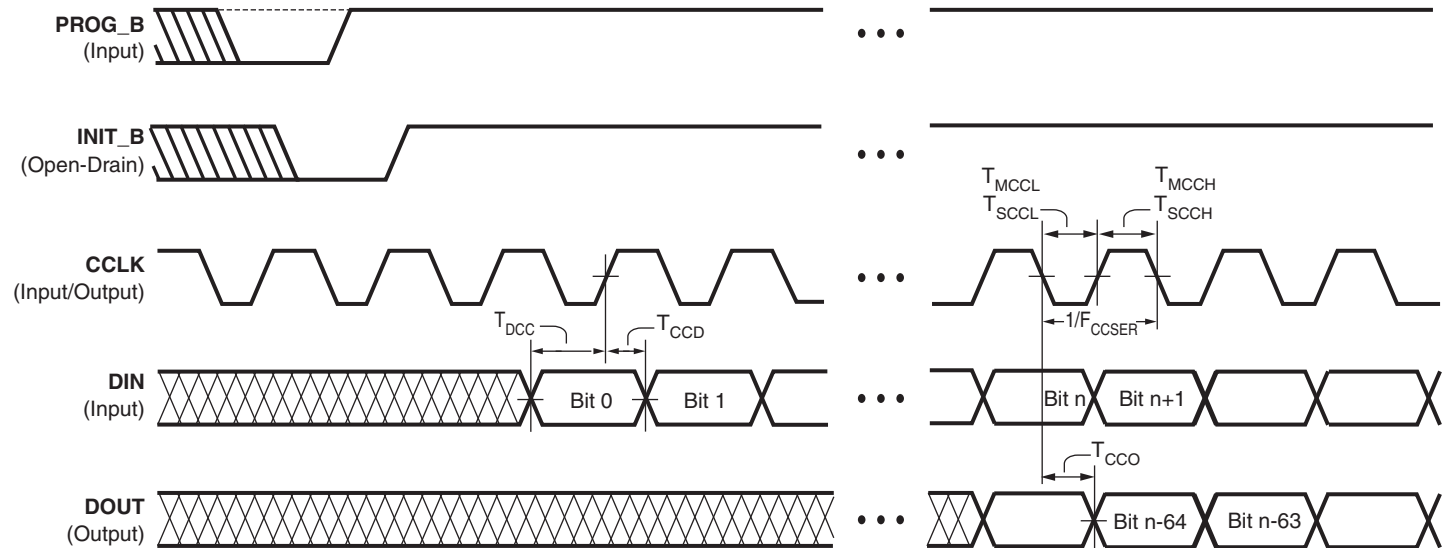
Notes:

1. The numbers in this table are based on the operating conditions set forth in [Table 10](#).
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. The PREG register is typically used when inferring a single-stage multiplier.
4. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.
5. Combinational delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.

Table 54: Slave Mode CCLK Input Low and High Time

Symbol	Description	Min	Max	Units
T_{SCCL} , T_{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing



DS312-3_05_103105

Figure 14: Waveforms for Master Serial and Slave Serial Configuration

Table 55: Timing for the Master Serial and Slave Serial Configuration Modes

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T _{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10	ns
Setup Times						
T _{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	7	—	ns
Hold Times						
T _{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Master	0	—	ns
			Slave	1.0		
Clock Timing						
T _{CCH}	High pulse width at the CCLK input pin		Master	See Table 53		
			Slave	See Table 54		
T _{CCL}	Low pulse width at the CCLK input pin		Master	See Table 53		
			Slave	See Table 54		
F _{CCSER}	Frequency of the clock signal at the CCLK input pin ⁽²⁾	No bitstream compression	Slave	0	100	MHz
		With bitstream compression		0	100	MHz

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 10.
- For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device (XC3S200AN). Timing specifications updated for v1.38 speed files. DC specifications updated with production values. Other changes throughout.
08/31/07	2.0.1	Updated for Production release of XC3S1400AN. Improved t_{PEP} for XC3S700AN in Table 48 .
09/12/07	2.0.2	Updated for Production release of XC3S700AN.
09/24/07	2.1	Updated for Production release of XC3S400AN. Updated Software Version Requirements to note that Production speed files are available as of Service Pack 3. Removed PCIX IOSTANDARD due to limited PCIX interface support. Added note that SPI_ACCESS (In-System Flash) is not currently supported in simulation.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that SPI_ACCESS simulation is supported in ISE 10.1 software. Removed DNA_RETENTION limit of 10 years in Table 17 since number of Read cycles is the only unique limit. Updated Setup, Hold, and Propagation Times for the IOB Input Path to show values by device in Table 23 and Table 25 . Increased SSO recommendation for SSTL18_II in Table 32 . Updated Figure 17 and Table 59 to show BPI data synchronous to CCLK rising edge. Updated links.
06/02/08	3.1	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 7 and updated V_{CCO} POR levels in Figure 13 . Clarified power sequencing in Note 1 of Table 7 , Table 8 , and Figure 13 . Added V_{IN} to Recommended Operating Conditions in Table 10 and added reference to XAPP459 , "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins." Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 12%-58% in Table 12 . Noted latest speed file v1.39 in ISE 10.1 software in Table 19 . Added reference to Sample Window in Table 24 . Changed Internal SPI interface max frequency to 50 MHz and updated other Internal SPI timing parameters to match names and values from speed file in Table 47 . Restored Units column to Table 49 . Updated CCLK output maximum period in Table 51 to match minimum frequency in Table 52 . Added references to User Guides.
11/19/09	3.2	Updated selected I/O standard DC characteristics. Changed typical quiescent current temperature from ambient to junction. Removed references to older software versions. Updated column 3 header of Table 17 and Table 18 . Added table note to Table 18 . Added T_{IOP1} and T_{IOPD} propagation times in Table 25 . Updated T_{LOCKHZ} and T_{LOCKON} synchronous output enable/disable times in Table 28 . Removed V_{REF} requirements for differential HSTL and differential SSTL in Table 30 . Improved DIFF_SSTL18_II SSO limits in Table 32 . Updated table note 3 in Table 39 . Removed references to old software versions from Table 47 and Table 48 . Added description of spread spectrum in Spread Spectrum section. Updated BPI configuration waveforms in Figure 17 . Updated T_{ACC} equation in Table 60 .
12/02/10	4.0	Added I_{IK} to Table 6 . Updated V_{IN} in Table 10 and added a footnote to I_L in Table 11 to note potential leakage between pins of a differential pair. Added note 6 to Table 13 . Corrected CLK High and Low Time symbol in Table 46 . Corrected symbols for $T_{SUSPEND_GTS}$ and $T_{SUSPEND_GWE}$ in Table 49 . Updated link to sign up for Alerts and updated Notice of Disclaimer .
04/01/11	4.1	In Table 31 , added the equivalent pairs per bank for the XC3S50AN and XC3S400AN in the FT(G)256 package and the XC3S1400AN in the FG(G)484 package.

Introduction

This section describes how the various pins on a Spartan®-3AN FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331:

- **UG331: Spartan-3 Generation FPGA User Guide**
http://www.xilinx.com/support/documentation/user_guides/ug331.pdf

Spartan-3AN FPGAs are available in Pb-free, RoHS packages, indicated by a “G” in the middle of the package code. Lead (Pb) packages are available for selected devices, with the same pinout and without the “G” in the ordering code (see [Table 5, page 7](#)). The Pb-free package code can be selected in the software for the Pb packages since the pinouts are identical. References to the Pb-free package code in this document apply also to the Pb package.

Pin Types

Most pins on a Spartan-3AN FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3AN FPGA packages, as outlined in [Table 62](#). In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 62: Types of Pins on Spartan-3AN FPGAs

Type with Color Code	Description	Pin Name(s) in Type ⁽¹⁾
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI™ clamp diode.	IP_# IP_Lxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: Spartan-3 Generation Configuration User Guide for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN DOUT CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxy_#/VREF_# IO/VREF_# IO_Lxy_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are all devices in the TQG144 package and the XC3S50AN in the FTG256 package. The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: Spartan-3 Generation FPGA User Guide for additional information on these signals.	IO_Lxy_#/GCLK[15:0], IO_Lxy_#/LHCLK[7:0], IO_Lxy_#/RHCLK[7:0]

Table 70: Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN) (Cont'd)

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
0	N.C.	IO_L14N_0/VREF_0	E7	VREF
0	N.C.	IO_L14P_0	F8	I/O
0	IO_L15N_0	IO_L15N_0	B6	I/O
0	IO_L15P_0	IO_L15P_0	A6	I/O
0	IO_L16N_0	IO_L16N_0	C6	I/O
0	IO_L16P_0	IO_L16P_0	D7	I/O
0	IO_L17N_0	IO_L17N_0	C5	I/O
0	IO_L17P_0	IO_L17P_0	A5	I/O
0	IO_L18N_0	IO_L18N_0	B4	I/O
0	IO_L18P_0	IO_L18P_0	A4	I/O
0	IO_L19N_0	IO_L19N_0	B3	I/O
0	IO_L19P_0	IO_L19P_0	A3	I/O
0	IO_L20N_0/PUDC_B	IO_L20N_0/PUDC_B	D5	DUAL
0	IO_L20P_0/VREF_0	IO_L20P_0/VREF_0	C4	VREF
0	IP_0	IP_0	D6	INPUT
0	IP_0	IP_0	D12	INPUT
0	IP_0	IP_0	E6	INPUT
0	IP_0	IP_0	F7	INPUT
0	IP_0	IP_0	F9	INPUT
0	IP_0	IP_0	F10	INPUT
0	IP_0/VREF_0	IP_0/VREF_0	E9	VREF
0	VCCO_0	VCCO_0	B5	VCCO
0	VCCO_0	VCCO_0	B9	VCCO
0	VCCO_0	VCCO_0	B13	VCCO
0	VCCO_0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	IO_L01N_1/LDC2	N14	DUAL
1	IO_L01P_1/HDC	IO_L01P_1/HDC	N13	DUAL
1	IO_L02N_1/LDC0	IO_L02N_1/LDC0	P15	DUAL
1	IO_L02P_1/LDC1	IO_L02P_1/LDC1	R15	DUAL
1	IO_L03N_1	IO_L03N_1/A1	N16	DUAL
1	IO_L03P_1	IO_L03P_1/A0	P16	DUAL
1	N.C.	IO_L05N_1/VREF_1	M14	VREF
1	N.C.	IO_L05P_1	M13	I/O
1	N.C.	IO_L06N_1/A3	K13	DUAL
1	N.C.	IO_L06P_1/A2	L13	DUAL
1	N.C.	IO_L07N_1/A5	M16	DUAL
1	N.C.	IO_L07P_1/A4	M15	DUAL
1	N.C.	IO_L08N_1/A7	L16	DUAL
1	N.C.	IO_L08P_1/A6	L14	DUAL
1	IO_L10N_1	IO_L10N_1/A9	J13	DUAL

User I/Os by Bank

Table 71 and Table 72 indicate how the available user-I/O pins are distributed between the four I/O banks on the FTG256 package. The AWAKE pin is counted as a dual-purpose I/O. The XC3S50AN FPGA in the FTG256 package has 51 unconnected balls, labeled with an N.C. type. These pins are also indicated in Figure 20.

Table 71: User I/Os Per Bank on XC3S50AN in the FTG256 Package

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	40	21	7	1	3	8
Right	1	32	12	5	4	3	8
Bottom	2	40	5	2	21	6	6
Left	3	32	15	6	0	3	8
Total		144	53	20	26	15	30

Table 72: User I/Os Per Bank on XC3S200AN and XC3S400AN in the FTG256 Package

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	47	27	6	1	5	8
Right	1	50	1	6	30	5	8
Bottom	2	48	11	2	21	6	8
Left	3	50	30	7	0	5	8
Total		195	69	21	52	21	32

Footprint Migration Differences

Unconnected Balls on XC3S50AN

[Table 73](#) summarizes any footprint and functionality differences between the XC3S50AN and the XC3S200AN or XC3S400AN devices for migration between these devices in the FTG256 package. The XC3S200AN and XC3S400AN have identical pinouts. The XC3S50AN pinout is compatible with the XC3S200AN and XC3S400AN, however, there are 51 unconnected balls and one functionally different ball. Generally, designs migrate upward from the XC3S50AN to either the XC3S200AN or XC3S400AN. If using differential I/O, see [Table 74](#). If using the BPI configuration mode (parallel Flash), see [Table 75](#).

In [Table 73](#), the arrow (→) indicates that this pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

Table 73: FTG256 XC3S50AN Footprint Migration/Differences

FTG256 Ball	Bank	XC3S50AN	Migration	XC3S200AN or XC3S400AN
A7	0	N.C.	→	I/O
A12	0	N.C.	→	I/O
B12	0	INPUT	→	I/O
C7	0	N.C.	→	I/O
D10	0	N.C.	→	I/O
E2	3	N.C.	→	I/O
E3	3	N.C.	→	I/O
E7	0	N.C.	→	I/O/VREF
E10	0	N.C.	→	I/O/VREF
E16	1	N.C.	→	I/O
F3	3	N.C.	→	I/O
F8	0	N.C.	→	I/O
F14	1	N.C.	→	I/O
F15	1	N.C.	→	I/O
F16	1	N.C.	→	I/O
G3	3	N.C.	→	I/O
G4	3	N.C.	→	I/O
G5	3	N.C.	→	INPUT/VREF
G6	3	N.C.	→	INPUT
G13	1	N.C.	→	I/O
G14	1	N.C.	→	I/O
G16	1	N.C.	→	I/O
H4	3	N.C.	→	I/O
H5	3	N.C.	→	I/O
H6	3	N.C.	→	I/O
H13	1	N.C.	→	I/O
J4	3	N.C.	→	I/O
J6	3	N.C.	→	I/O
J10	1	N.C.	→	INPUT/VREF
J11	1	N.C.	→	INPUT
K4	3	N.C.	→	I/O

FGG400: 400-Ball Fine-Pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FGG400, supports the XC3S400AN FPGA as shown in [Table 76](#) and [Figure 22](#).

[Table 76](#) lists all the FGG400 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type (as defined in [Table 62](#)).

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 76: Spartan-3AN FGG400 Pinout

Bank	Pin Name	FGG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK

Table 76: Spartan-3AN FGG400 Pinout (Cont'd)

Bank	Pin Name	FGG400 Ball	Type
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O

Table 76: Spartan-3AN FGG400 Pinout (Cont'd)

Bank	Pin Name	FGG400 Ball	Type
0	IO_L32N_0/PUDC_B	B2	DUAL
0	IO_L32P_0/VREF_0	A2	VREF
0	IP_0	E14	INPUT
0	IP_0	F11	INPUT
0	IP_0	F14	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT
0	IP_0	G10	INPUT
0	IP_0	G12	INPUT
0	IP_0	G13	INPUT
0	IP_0	H9	INPUT
0	IP_0	H10	INPUT
0	IP_0	H11	INPUT
0	IP_0	H12	INPUT
0	IP_0/VREF_0	G11	VREF
0	VCCO_0	B4	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	D7	VCCO
0	VCCO_0	D13	VCCO
0	VCCO_0	F10	VCCO
1	IO_L01N_1/LDC2	V20	DUAL
1	IO_L01P_1/HDC	W20	DUAL
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	V19	DUAL
1	IO_L03N_1/A1	R16	DUAL
1	IO_L03P_1/A0	T17	DUAL
1	IO_L05N_1	T20	I/O
1	IO_L05P_1	T18	I/O
1	IO_L06N_1	U20	I/O
1	IO_L06P_1	U19	I/O
1	IO_L07N_1	P17	I/O
1	IO_L07P_1	P16	I/O
1	IO_L08N_1	R17	I/O
1	IO_L08P_1	R18	I/O
1	IO_L09N_1	R20	I/O
1	IO_L09P_1	R19	I/O
1	IO_L10N_1/VREF_1	P20	VREF
1	IO_L10P_1	P18	I/O
1	IO_L12N_1/A3	N17	DUAL

Table 76: Spartan-3AN FGG400 Pinout (Cont'd)

Bank	Pin Name	FGG400 Ball	Type
1	IO_L12P_1/A2	N15	DUAL
1	IO_L13N_1/A5	N19	DUAL
1	IO_L13P_1/A4	N18	DUAL
1	IO_L14N_1/A7	M18	DUAL
1	IO_L14P_1/A6	M17	DUAL
1	IO_L16N_1/A9	L16	DUAL
1	IO_L16P_1/A8	L15	DUAL
1	IO_L17N_1/RHCLK1	M20	RHCLK
1	IO_L17P_1/RHCLK0	M19	RHCLK
1	IO_L18N_1/TRDY1/RHCLK3	L18	RHCLK
1	IO_L18P_1/RHCLK2	L19	RHCLK
1	IO_L20N_1/RHCLK5	L17	RHCLK
1	IO_L20P_1/RHCLK4	K18	RHCLK
1	IO_L21N_1/RHCLK7	J20	RHCLK
1	IO_L21P_1/IRDY1/RHCLK6	K20	RHCLK
1	IO_L22N_1/A11	J18	DUAL
1	IO_L22P_1/A10	J19	DUAL
1	IO_L24N_1	K16	I/O
1	IO_L24P_1	J17	I/O
1	IO_L25N_1/A13	H18	DUAL
1	IO_L25P_1/A12	H19	DUAL
1	IO_L26N_1/A15	G20	DUAL
1	IO_L26P_1/A14	H20	DUAL
1	IO_L28N_1	H17	I/O
1	IO_L28P_1	G18	I/O
1	IO_L29N_1/A17	F19	DUAL
1	IO_L29P_1/A16	F20	DUAL
1	IO_L30N_1/A19	F18	DUAL
1	IO_L30P_1/A18	G17	DUAL
1	IO_L32N_1	E19	I/O
1	IO_L32P_1	E20	I/O
1	IO_L33N_1	F17	I/O
1	IO_L33P_1	E18	I/O
1	IO_L34N_1	D18	I/O
1	IO_L34P_1	D20	I/O
1	IO_L36N_1/A21	F16	DUAL
1	IO_L36P_1/A20	G16	DUAL
1	IO_L37N_1/A23	C19	DUAL
1	IO_L37P_1/A22	C20	DUAL
1	IO_L38N_1/A25	B19	DUAL

Bank 0										Bank 1										Bank 2									
11	12	13	14	15	16	17	18	19	20																				
GND	I/O L13N_0	VCCAUX	I/O L07N_0	I/O L08N_0	I/O L05N_0	I/O L04N_0	I/O L01N_0	TCK	GND																				
I/O L14P_0	I/O L13P_0	I/O L11P_0	GND	I/O L08P_0	VCCO_0	I/O L04P_0 VREF_0	I/O L01P_0	I/O L38N_1 A25	I/O L38P_1 A24																				
I/O L14N_0	I/O L11N_0	I/O L10N_0 VREF_0	I/O L07P_0	I/O L06N_0	I/O L05P_0	I/O L02N_0	GND	I/O L37N_1 A23	I/O L37P_1 A22																				
I/O L15P_0 GCLK4	I/O L12P_0	VCCO_0	I/O L10P_0	I/O L06P_0	I/O L03P_0	I/O L02P_0 VREF_0	I/O L34N_1	VCCO_1	I/O L34P_1																				
I/O L15N_0 GCLK5	GND	I/O L09P_0	INPUT	I/O L03N_0	VCCAUX	TDO	I/O L33P_1	I/O L32N_1	I/O L32P_1																				
INPUT	I/O L12N_0	I/O L09N_0	INPUT	GND	I/O L36N_1 A21	I/O L33N_1	I/O L30N_1 A19	I/O L29N_1 A17	I/O L29P_1 A16																				
INPUT VREF_0	INPUT	INPUT	INPUT L39P_1 VREF_1	INPUT L39N_1	I/O L36P_1 A20	I/O L30P_1 A18	I/O L28P_1	GND	I/O L26N_1 A15																				
INPUT	INPUT	GND	INPUT L35N_1	INPUT L35P_1	VCCO_1	I/O L28N_1	I/O L25N_1 A13	I/O L25P_1 A12	I/O L26P_1 A14																				
GND	VCCINT	INPUT L31N_1 VREF_1	INPUT L27N_1	INPUT L27P_1	INPUT L27N_1	I/O L24P_1	I/O L22N_1 A11	I/O L22P_1 A10	I/O L21N_1 RHCLK7																				
VCCINT	GND	VCCAUX	INPUT L23N_1	INPUT L23P_1 VREF_1	I/O L24N_1	GND	I/O L20P_1 RHCLK4	VCCO_1	I/O L21P_1 IRDY1 RHCLK6																				
GND	VCCINT	INPUT L19N_1	INPUT L19P_1	I/O L16P_1 A8	I/O L16N_1 A9	I/O L20N_1 RHCLK5	I/O L18N_1 TRDY1 RHCLK3	I/O L18P_1 RHCLK2	GND																				
VCCINT	GND	INPUT L15N_1	INPUT L15P_1 VREF_1	INPUT L11N_1 VREF_1	INPUT L11P_1	I/O L14P_1 A6	I/O L14N_1 A7	I/O L17P_1 RHCLK0	I/O L17N_1 RHCLK1																				
GND	INPUT VREF_2	GND	INPUT VREF_1	I/O L12P_1 A2	VCCO_1	I/O L12N_1 A3	I/O L13P_1 A4	I/O L13N_1 A5	VCCAUX																				
INPUT VREF_2	INPUT	INPUT	INPUT L04P_1 VREF_1	INPUT L04N_1 VREF_1	I/O L07P_1	I/O L07N_1	I/O L10P_1	GND	I/O L10N_1 VREF_1																				
VCCO_2	I/O L19N_2	I/O L23N_2	INPUT VREF_2	SUSPEND	I/O L03N_1 A1	I/O L08N_1	I/O L08P_1	I/O L09P_1	I/O L09N_1																				
INPUT	I/O L19P_2	I/O L23P_2	I/O L25N_2	I/O L27N_2	GND	I/O L03P_1 A0	I/O L05P_1	VCCO_1	I/O L05N_1																				
I/O L18P_2 GCLK2	GND	I/O L22P_2 AWAKE	VCCO_2	I/O L27P_2	I/O L29N_2	I/O L31N_2	I/O L02N_1 LDC0	I/O L06P_1	I/O L06N_1																				
I/O L17N_2 GCLK1	I/O L18N_2 GCLK3	I/O L22N_2 DOUT	I/O L25P_2	I/O L26N_2 D1	I/O L29P_2	I/O L31P_2	GND	I/O L02P_1 LDC1	I/O L01N_1 LDC2																				
VCCO_2	I/O L20N_2 MOSI CSL_B	I/O L21N_2	I/O L24N_2 D3	GND	I/O L28N_2	VCCO_2	I/O L32P_2 D0 DIN/MISO	DONE	I/O L01P_1 HDC																				
I/O L17P_2 GCLK0	I/O L20P_2	I/O L21P_2	I/O L24P_2 INIT_B	I/O L26P_2 D2	I/O L28P_2	I/O L30P_2	I/O L30N_2	I/O L32N_2 CCLK	GND																				

Right Half of FGG400
Package (Top View)

DS557_4_22_030911

Figure 22: FGG400 Package Footprint (Top View)

Table 78: Spartan-3AN FGG484 Pinout (Cont'd)

Bank	Pin Name	FGG484 Ball	Type
2	IO_L10N_2	AB7	I/O
2	IO_L10P_2	Y7	I/O
2	IO_L11N_2/VS0	Y8	DUAL
2	IO_L11P_2/VS1	W8	DUAL
2	IO_L12N_2	AB8	I/O
2	IO_L12P_2	AA8	I/O
2	IO_L13N_2	Y10	I/O
2	IO_L13P_2	V10	I/O
2	IO_L14N_2/D6	AB9	DUAL
2	IO_L14P_2/D7	Y9	DUAL
2	IO_L15N_2	AB10	I/O
2	IO_L15P_2	AA10	I/O
2	IO_L16N_2/D4	AB11	DUAL
2	IO_L16P_2/D5	Y11	DUAL
2	IO_L17N_2/GCLK13	V11	GCLK
2	IO_L17P_2/GCLK12	U11	GCLK
2	IO_L18N_2/GCLK15	Y12	GCLK
2	IO_L18P_2/GCLK14	W12	GCLK
2	IO_L19N_2/GCLK1	AB12	GCLK
2	IO_L19P_2/GCLK0	AA12	GCLK
2	IO_L20N_2/GCLK3	U12	GCLK
2	IO_L20P_2/GCLK2	V12	GCLK
2	IO_L21N_2	Y13	I/O
2	IO_L21P_2	AB13	I/O
2	IO_L22N_2/MOSI/CSI_B	AB14	DUAL
2	IO_L22P_2	AA14	I/O
2	IO_L23N_2	Y14	I/O
2	IO_L23P_2	W13	I/O
2	IO_L24N_2/DOOUT	AA15	DUAL
2	IO_L24P_2/AWAKE	AB15	PWR MGMT
2	IO_L25N_2	Y15	I/O
2	IO_L25P_2	W15	I/O
2	IO_L26N_2/D3	U13	DUAL
2	IO_L26P_2/INIT_B	V13	DUAL
2	IO_L27N_2	Y16	I/O
2	IO_L27P_2	AB16	I/O
2	IO_L28N_2/D1	Y17	DUAL
2	IO_L28P_2/D2	AA17	DUAL
2	IO_L29N_2	AB18	I/O
2	IO_L29P_2	AB17	I/O

Table 78: Spartan-3AN FGG484 Pinout (Cont'd)

Bank	Pin Name	FGG484 Ball	Type
2	IO_L30N_2	V15	I/O
2	IO_L30P_2	V14	I/O
2	IO_L31N_2	V16	I/O
2	IO_L31P_2	W16	I/O
2	IO_L32N_2	AA19	I/O
2	IO_L32P_2	AB19	I/O
2	IO_L33N_2	V17	I/O
2	IO_L33P_2	W18	I/O
2	IO_L34N_2	W17	I/O
2	IO_L34P_2	Y18	I/O
2	IO_L35N_2	AA21	I/O
2	IO_L35P_2	AB21	I/O
2	IO_L36N_2/CCLK	AA20	DUAL
2	IO_L36P_2/D0/DIN/MISO	AB20	DUAL
2	IP_2	P12	INPUT
2	IP_2	R10	INPUT
2	IP_2	R11	INPUT
2	IP_2	R9	INPUT
2	IP_2	T13	INPUT
2	IP_2	T14	INPUT
2	IP_2	T9	INPUT
2	IP_2	U10	INPUT
2	IP_2	U15	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ♦	U16	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ♦	U7	INPUT
2	IP_2	U8	INPUT
2	IP_2	V7	INPUT
2	IP_2/VREF_2	R12	VREF
2	IP_2/VREF_2	R13	VREF
2	IP_2/VREF_2	R14	VREF
2	IP_2/VREF_2	T10	VREF
2	IP_2/VREF_2	T11	VREF
2	IP_2/VREF_2	T15	VREF
2	IP_2/VREF_2	T16	VREF
2	IP_2/VREF_2	T7	VREF
2	XC3S1400AN: IP_2/VREF_2 XC3S700AN: N.C. ♦	T8	VREF
2	IP_2/VREF_2	V8	VREF

Table 78: Spartan-3AN FGG484 Pinout (Cont'd)

Bank	Pin Name	FGG484 Ball	Type
VCCAUX	DONE	Y19	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A21	JTAG
VCCAUX	TDI	F5	JTAG
VCCAUX	TDO	E19	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	H11	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	P11	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P13	VCCINT

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
3	IP_L58N_3/VREF_3	AA5	VREF
3	IP_L58P_3	AA4	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IP_L66P_3	AE1	INPUT
3	VCCO_3	AB2	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	W5	VCCO
GND	GND	A1	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND
GND	GND	A26	GND
GND	GND	AA1	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	AD3	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD24	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	C3	GND
GND	GND	C9	GND

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
GND	GND	C14	GND
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	J24	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND

Notice of Disclaimer

THE XILINX HARDWARE FPGA AND CPLD DEVICES REFERRED TO HEREIN ("PRODUCTS") ARE SUBJECT TO THE TERMS AND CONDITIONS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT <http://www.xilinx.com/warranty.htm>. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED IN THE XILINX DATA SHEET. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, OR ANY OTHER APPLICATION THAT INVOKES THE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). USE OF PRODUCTS IN CRITICAL APPLICATIONS IS AT THE SOLE RISK OF CUSTOMER, SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

CRITICAL APPLICATIONS DISCLAIMER

XILINX PRODUCTS (INCLUDING HARDWARE, SOFTWARE AND/OR IP CORES) ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS IN LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, CLASS III MEDICAL DEVICES, NUCLEAR FACILITIES, APPLICATIONS RELATED TO THE DEPLOYMENT OF AIRBAGS, OR ANY OTHER APPLICATIONS THAT COULD LEAD TO DEATH, PERSONAL INJURY OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (INDIVIDUALLY AND COLLECTIVELY, "CRITICAL APPLICATIONS"). FURTHERMORE, XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN ANY APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE OR AIRCRAFT, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR. CUSTOMER AGREES, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE XILINX PRODUCTS, TO THOROUGHLY TEST THE SAME FOR SAFETY PURPOSES. TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN CRITICAL APPLICATIONS.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.