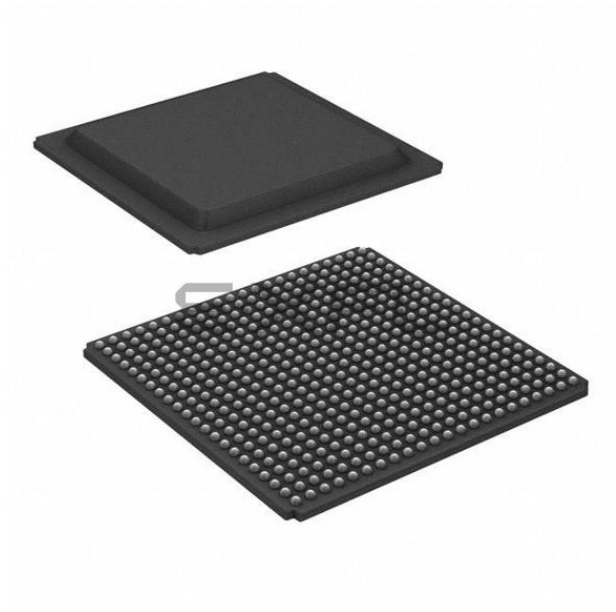
AMD Xilinx - XC3S1400AN-5FGG484C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2816
Number of Logic Elements/Cells	25344
Total RAM Bits	589824
Number of I/O	372
Number of Gates	1400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s1400an-5fgg484c

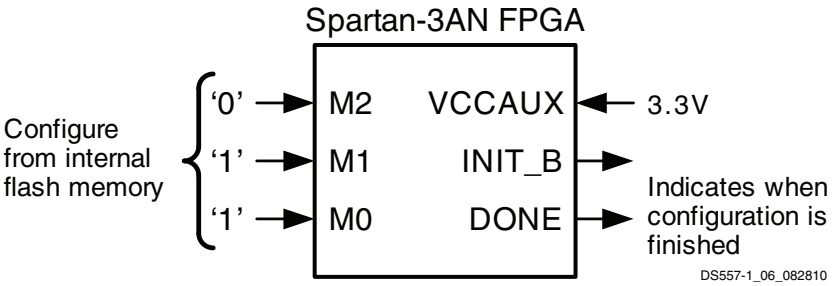


Figure 2: **Spartan-3AN FPGA Configuration Interface from Internal SPI Flash Memory**

Configuration

Spartan-3AN FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored on-chip in nonvolatile Flash memory, or externally in a PROM or some other nonvolatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Configure from internal SPI Flash memory (Figure 2)
  - Completely self-contained
  - Reduced board space
  - Easy-to-use configuration interface
- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an external industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary-Scan (JTAG), typically downloaded from a processor or system tester

The MultiBoot feature stores multiple configuration files in the on-chip Flash, providing extended life with field upgrades. MultiBoot also supports multiple system solutions with a single board to minimize inventory and simplify the addition of new features, even in the field. Flexibility is maintained to do additional MultiBoot configurations via the external configuration method.

The Spartan-3AN device authentication protocol prevents cloning. Design cloning, unauthorized overbuilding, and complete reverse engineering have driven device security requirements to higher and higher levels. Authentication moves the security from bitstream protection to the next generation of design-level security protecting both the design and embedded microcode. The authentication algorithm is entirely user defined, implemented using FPGA logic. Every product, generation, or design can have a different algorithm and functionality to enhance security.

In-System Flash Memory

Each Spartan-3AN FPGA contains abundant integrated SPI serial Flash memory, shown in Table 3, used primarily to store the FPGA's configuration bitstream. However, the Flash memory array is large enough to store at least two MultiBoot FPGA configuration bitstreams or nonvolatile data required by the FPGA application, such as code-shadowed MicroBlaze processor applications.

Table 3: **Spartan-3AN Device In-System Flash Memory**

Part Number	Total Flash Memory (Bits)	FPGA Bitstream (Bits)	Additional Flash Memory (Bits)(1)
XC3S50AN	1,081,344	437,312	642,048
XC3S200AN	4,325,376	1,196,128	3,127,872
XC3S400AN	4,325,376	1,886,560	2,437,248
XC3S700AN	8,650,752	2,732,640	5,917,824
XC3S1400AN	17,301,504	4,755,296	12,545,280

Notes:

1. Aligned to next available page location.

After configuration, the FPGA design has full access to the in-system Flash memory via an internal SPI interface; the control logic is implemented with FPGA logic. Additionally, the FPGA application itself can store nonvolatile data or provide live, in-system Flash updates.

The Spartan-3AN device in-system Flash memory supports leading-edge serial Flash features.

- Small page size (264 or 528 bytes) simplifies nonvolatile data storage
- Randomly accessible, byte addressable
- Up to 66 MHz serial data transfers
- SRAM page buffers
  - Read Flash data while programming another Flash page
  - EEPROM-like byte write functionality
  - Two buffers in most devices, one in XC3S50AN
- Page, Block, and Sector Erase

Ordering Information

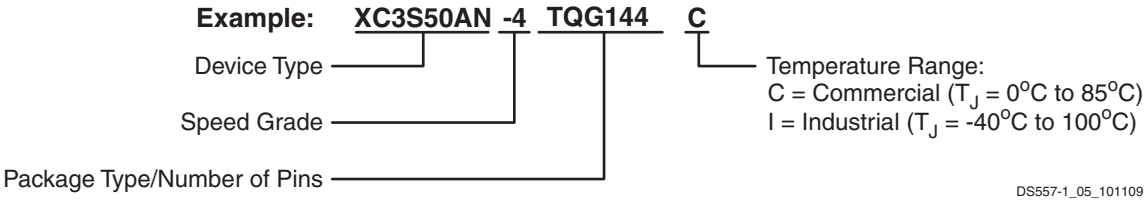


Figure 5: **Device Numbering Format**

Device	Speed Grade		Package Type / Number of Pins		Temperature Range (T_J)	
XC3S50AN	-4	Standard Performance	TQ144/ TQG144	144-pin Thin Quad Flat Pack (TQFP)	C	Commercial (0°C to 85°C)
XC3S200AN	-5	High Performance(1)	FT256/ FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)	I	Industrial (–40°C to 100°C)
XC3S400AN			FG400/ FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3S700AN			FG484/ FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3S1400AN			FG676/ FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)		

Notes:

1. The -5 speed grade is exclusively available in the Commercial temperature range.
2. See Table 4 and Table 5 for available package combinations.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device.
09/12/07	2.0.1	Noted that only dual-mark devices are guaranteed for both -4I and -5C.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that non-Pb-free packages may be available for selected devices.
06/02/08	3.1	Minor updates.
11/19/09	3.2	Updated document throughout to reflect availability of Pb package options. Added references to the Extended Spartan-3A family. Removed table note 2 from Table 2. In Table 4, added Pb packages, added table note 4, and updated table note 2. Added Table 5.
12/02/10	4.0	Updated Notice of Disclaimer.
04/01/11	4.1	In Table 2, revised the Maximum Differential I/O Pairs and Maximum User I/O values for the XC3S50AN. In Table 4, added packages to the XC3S50AN, XC3S400AN, and XC3S1400AN. Updated Pb and Pb-Free Packaging section and Table 5 to include the new device/package combinations for the XC3S50AN, XC3S400AN, and XC3S1400AN.

General Recommended Operating Conditions

Table 10: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V_{CCO} (1)	Output driver supply voltage			1.10	–	3.60	V
V_{CCAUX}	Auxiliary supply voltage	V_{CCAUX} = 3.3V		3.00	3.30	3.60	V
V_{IN} (2)	Input voltage	PCI IOSTANDARD		–0.5	–	V_{CCO} + 0.5	V
		All other IOSTANDARDs	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_# (3)	–0.5	–	4.10	V
T_{IN}	Input signal transition time (4)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 13 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 15 lists that specific to the differential standards.
2. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
3. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
4. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

Pin-to-Pin Setup and Hold Times

Table 22: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50AN	2.45	2.68	ns
			XC3S200AN	2.59	2.84	ns
			XC3S400AN	2.38	2.68	ns
			XC3S700AN	2.38	2.57	ns
			XC3S1400AN	1.91	2.17	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 5, without DCM	XC3S50AN	2.55	2.76	ns
			XC3S200AN	2.32	2.76	ns
			XC3S400AN	2.21	2.60	ns
			XC3S700AN	2.28	2.63	ns
			XC3S1400AN	2.33	2.41	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50AN	–0.36	–0.36	ns
			XC3S200AN	–0.52	–0.52	ns
			XC3S400AN	–0.33	–0.29	ns
			XC3S700AN	–0.17	–0.12	ns
			XC3S1400AN	–0.07	0.00	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 5, without DCM	XC3S50AN	–0.63	–0.58	ns
			XC3S200AN	–0.56	–0.56	ns
			XC3S400AN	–0.42	–0.42	ns
			XC3S700AN	–0.80	–0.75	ns
			XC3S1400AN	–0.69	–0.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 26. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 26. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Propagation Times

Table 25: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
Propagation Times							
T_{IOPI}	The time it takes for data to travel from the Input pin to the I output with no input delay programmed	LVCMOS25(2)	IBUF_DELAY_VALUE=0	XC3S50AN	1.04	1.12	ns
				XC3S200AN	0.87	0.87	ns
				XC3S400AN	0.65	0.72	ns
				XC3S700AN	0.92	0.92	ns
				XC3S1400AN	0.96	1.21	ns
T_{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25(2)	1	XC3S50AN	1.79	2.07	ns
			2		2.13	2.46	ns
			3		2.36	2.71	ns
			4		2.88	3.21	ns
			5		3.11	3.46	ns
			6		3.45	3.84	ns
			7		3.75	4.19	ns
			8		4.00	4.47	ns
			9		3.61	4.11	ns
			10		3.95	4.50	ns
			11		4.18	4.67	ns
			12		4.75	5.20	ns
			13		4.98	5.44	ns
			14		5.31	5.95	ns
			15		5.62	6.28	ns
			16		5.86	6.57	ns
			1	XC3S200AN	1.57	1.65	ns
			2		1.87	1.97	ns
			3		2.16	2.33	ns
			4		2.68	2.96	ns
			5		2.87	3.19	ns
			6		3.20	3.60	ns
			7		3.57	4.02	ns
			8		3.79	4.26	ns
			9		3.42	3.86	ns
			10		3.79	4.25	ns
			11		4.02	4.55	ns
			12		4.62	5.24	ns
			13		4.86	5.53	ns
			14		5.18	5.94	ns

Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair**

Signal Standard (IOSTANDARD)			Package Type			
			TQG144		FTG256, FGG400, FGG484, FGG676	
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
Single-Ended Standards						
LVTTL	Slow	2	20	20	60	60
		4	10	10	41	41
		6	10	10	29	29
		8	6	6	22	22
		12	6	6	13	13
		16	5	5	11	11
		24	4	4	9	9
	Fast	2	10	10	10	10
		4	6	6	6	6
		6	5	5	5	5
		8	3	3	3	3
		12	3	3	3	3
		16	3	3	3	3
		24	2	2	2	2
	QuietIO	2	40	40	80	80
		4	24	24	48	48
		6	20	20	36	36
		8	16	16	27	27
		12	12	12	16	16
		16	9	9	13	13
		24	9	9	12	12

Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type			
			TQG144		FTG256, FGG400, FGG484, FGG676	
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
LVCMOS33	Slow	2	24	24	76	76
		4	14	14	46	46
		6	11	11	27	27
		8	10	10	20	20
		12	9	9	13	13
		16	8	8	10	10
		24	–	8	–	9
	Fast	2	10	10	10	10
		4	8	8	8	8
		6	5	5	5	5
		8	4	4	4	4
		12	4	4	4	4
		16	2	2	2	2
		24	–	2	–	2
	QuietIO	2	36	36	76	76
		4	32	32	46	46
		6	24	24	32	32
		8	16	16	26	26
		12	16	16	18	18
		16	12	12	14	14
		24	–	10	–	10

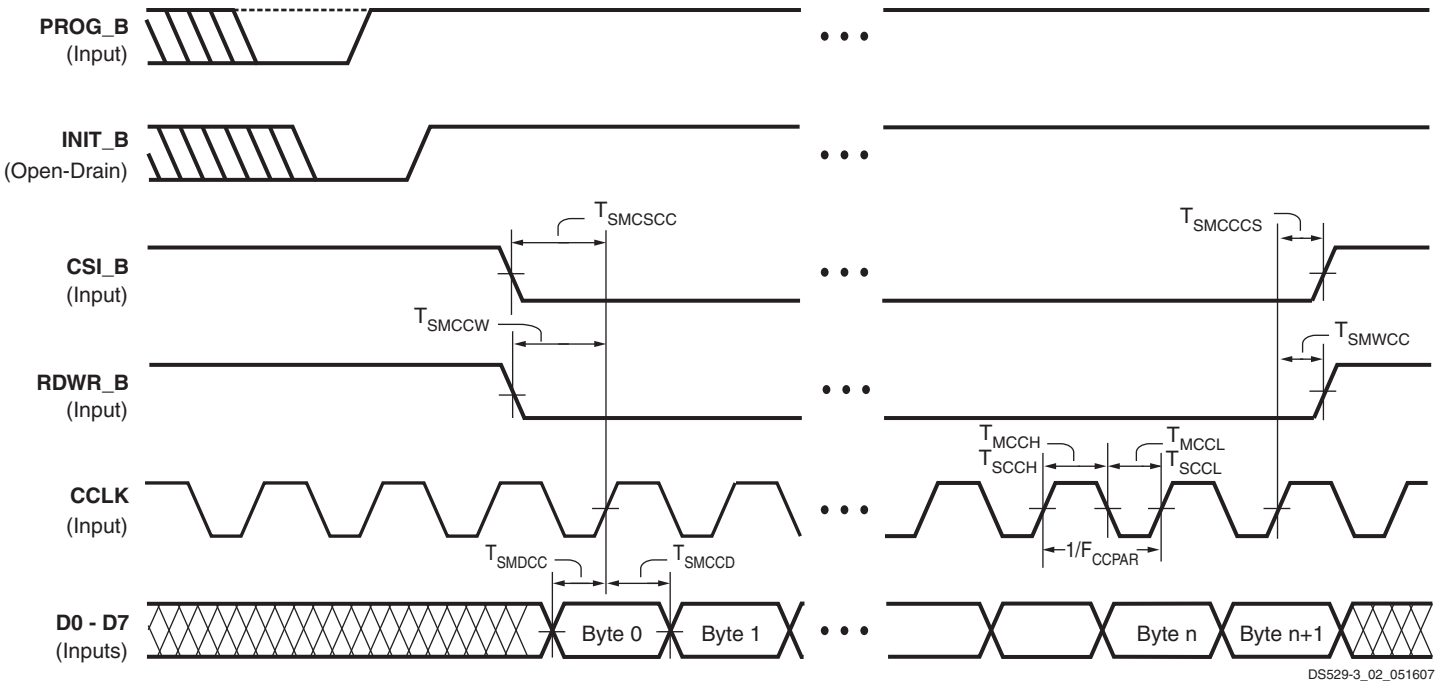
Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type			
			TQG144		FTG256, FGG400, FGG484, FGG676	
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
LVCMOS25	Slow	2	16	16	76	76
		4	10	10	46	46
		6	8	8	33	33
		8	7	7	24	24
		12	6	6	18	18
		16	–	6	–	11
		24	–	5	–	7
	Fast	2	12	12	18	18
		4	10	10	14	14
		6	8	8	6	6
		8	6	6	6	6
		12	3	3	3	3
		16	–	3	–	3
		24	–	2	–	2
	QuietIO	2	36	36	76	76
		4	30	30	60	60
		6	24	24	48	48
		8	20	20	36	36
		12	12	12	36	36
		16	–	12	–	36
		24	–	8	–	8

Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type			
			TQG144		FTG256, FGG400, FGG484, FGG676	
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
LVCMOS18	Slow	2	13	13	64	64
		4	8	8	34	34
		6	8	8	22	22
		8	7	7	18	18
		12	–	5	–	13
		16	–	5	–	10
	Fast	2	13	13	18	18
		4	8	8	9	9
		6	7	7	7	7
		8	4	4	4	4
		12	–	4	–	4
		16	–	3	–	3
	QuietIO	2	30	30	64	64
		4	24	24	64	64
		6	20	20	48	48
		8	16	16	36	36
		12	–	12	–	36
		16	–	12	–	24
LVCMOS15	Slow	2	12	12	55	55
		4	7	7	31	31
		6	7	7	18	18
		8	–	6	–	15
		12	–	5	–	10
	Fast	2	10	10	25	25
		4	7	7	10	10
		6	6	6	6	6
		8	–	4	–	4
		12	–	3	–	3
	QuietIO	2	30	30	70	70
		4	21	21	40	40
		6	18	18	31	31
		8	–	12	–	31
		12	–	12	–	20

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0–D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0–D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See UG332, Chapter 7, section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 15: **Waveforms for Slave Parallel Configuration**

Table 56: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}(2)	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		15	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1.0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10.
2. Some Xilinx documents refer to Parallel modes as SelectMAP modes.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device (XC3S200AN). Timing specifications updated for v1.38 speed files. DC specifications updated with production values. Other changes throughout.
08/31/07	2.0.1	Updated for Production release of XC3S1400AN. Improved t_{PEP} for XC3S700AN in Table 48.
09/12/07	2.0.2	Updated for Production release of XC3S700AN.
09/24/07	2.1	Updated for Production release of XC3S400AN. Updated Software Version Requirements to note that Production speed files are available as of Service Pack 3. Removed PCIX IOSTANDARD due to limited PCIX interface support. Added note that SPI_ACCESS (In-System Flash) is not currently supported in simulation.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that SPI_ACCESS simulation is supported in ISE 10.1 software. Removed DNA_RETENTION limit of 10 years in Table 17 since number of Read cycles is the only unique limit. Updated Setup, Hold, and Propagation Times for the IOB Input Path to show values by device in Table 23 and Table 25. Increased SSO recommendation for SSTL18_II in Table 32. Updated Figure 17 and Table 59 to show BPI data synchronous to CCLK rising edge. Updated links.
06/02/08	3.1	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 7 and updated V_{CCO} POR levels in Figure 13. Clarified power sequencing in Note 1 of Table 7, Table 8, and Figure 13. Added V_{IN} to Recommended Operating Conditions in Table 10 and added reference to XAPP459, “Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins.” Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 12%-58% in Table 12. Noted latest speed file v1.39 in ISE 10.1 software in Table 19. Added reference to Sample Window in Table 24. Changed Internal SPI interface max frequency to 50 MHz and updated other Internal SPI timing parameters to match names and values from speed file in Table 47. Restored Units column to Table 49. Updated CCLK output maximum period in Table 51 to match minimum frequency in Table 52. Added references to User Guides.
11/19/09	3.2	Updated selected I/O standard DC characteristics. Changed typical quiescent current temperature from ambient to junction. Removed references to older software versions. Updated column 3 header of Table 17 and Table 18. Added table note to Table 18. Added T_{IOPI} and T_{IOPID} propagation times in Table 25. Updated T_{IOCKHZ} and T_{IOCKON} synchronous output enable/disable times in Table 28. Removed V_{REF} requirements for differential HSTL and differential SSTL in Table 30. Improved DIFF_SSTL18_II SSO limits in Table 32. Updated table note 3 in Table 39. Removed references to old software versions from Table 47 and Table 48. Added description of spread spectrum in Spread Spectrum section. Updated BPI configuration waveforms in Figure 17. Updated T_{ACC} equation in Table 60.
12/02/10	4.0	Added I_{IK} to Table 6. Updated V_{IN} in Table 10 and added a footnote to I_L in Table 11 to note potential leakage between pins of a differential pair. Added note 6 to Table 13. Corrected CLK High and Low Time symbol in Table 46. Corrected symbols for $T_{SUSPEND\_GTS}$ and $T_{SUSPEND\_GWE}$ in Table 49. Updated link to sign up for Alerts and updated Notice of Disclaimer.
04/01/11	4.1	In Table 31, added the equivalent pairs per bank for the XC3S50AN and XC3S400AN in the FT(G)256 package and the XC3S1400AN in the FG(G)484 package.

Notice of Disclaimer

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx website at the specified location in Table 66.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx website for each package.

Table 66: **Xilinx Package Documentation**

Package	Drawing	MDDS
TQ144	Package Drawing	PK169_TQ144
TQG144		PK461_TQG144
FT256	Package Drawing	PK158_FT256
FTG256		PK424_FTG256
FG400	Package Drawing	PK182_FG400
FGG400		PK108_FGG400
FG484	Package Drawing	PK183_FG484
FGG484		PK110_FGG484
FG676	Package Drawing	PK155_FG676
FGG676		PK394_FGG676

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3AN FPGA is reported using either the XPower Power Estimator or the XPower Analyzer calculator integrated in the Xilinx® ISE® development software. Table 67 provides the thermal characteristics for the various Spartan-3AN FPGA packages. This information is also available using the Thermal Query tool at http://www.xilinx.com/cgi-bin/thermal/thermal.pl.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The “Still Air (0 LFM)” column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 67: **Spartan-3AN FPGA Package Thermal Characteristics**

Device	Package[1]	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
XC3S50AN	TQG144	13.4	32.8	38.9	32.8	32.5	31.7	°C/Watt
	FTG256							°C/Watt
XC3S200AN	FTG256	7.4	23.3	29.0	23.8	23.0	22.3	°C/Watt
XC3S400AN	FTG256							°C/Watt
	FGG400	6.2	12.9	22.5	16.7	15.6	15.0	°C/Watt
XC3S700AN	FGG484	5.3	11.5	19.4	15.0	13.9	13.4	°C/Watt
XC3S1400AN	FGG484							°C/Watt
	FGG676	4.3	10.9	17.7	13.7	12.6	12.1	°C/Watt

Notes:

1. Thermal characteristics are similar for leaded (non-Pb-free) packages.
2. Use the Thermal Query tool at http://www.xilinx.com/cgi-bin/thermal/thermal.pl for specific device information.

User I/Os by Bank

Table 69 indicates how the 108 available user-I/O pins are distributed between the four I/O banks on the TQG144 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 69: **User I/Os Per Bank for the XC3S50AN in the TQG144 Package**

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	27	14	1	1	3	8
Right	1	25	11	0	4	2	8
Bottom	2	30	2	0	21	1	6
Left	3	26	15	1	0	2	8
Total		**108**	**42**	**2**	**26**	**8**	**30**

Footprint Migration Differences

The XC3S50AN FPGA is the only Spartan-3AN device offered in the TQG144 package. The XC3S50AN FPGA is pin compatible with the Spartan-3A XC3S50A FPGA in the TQ(G)144 package, although the Spartan-3A FPGA requires an external configuration source.

FTG256 Footprint (XC3S50AN)

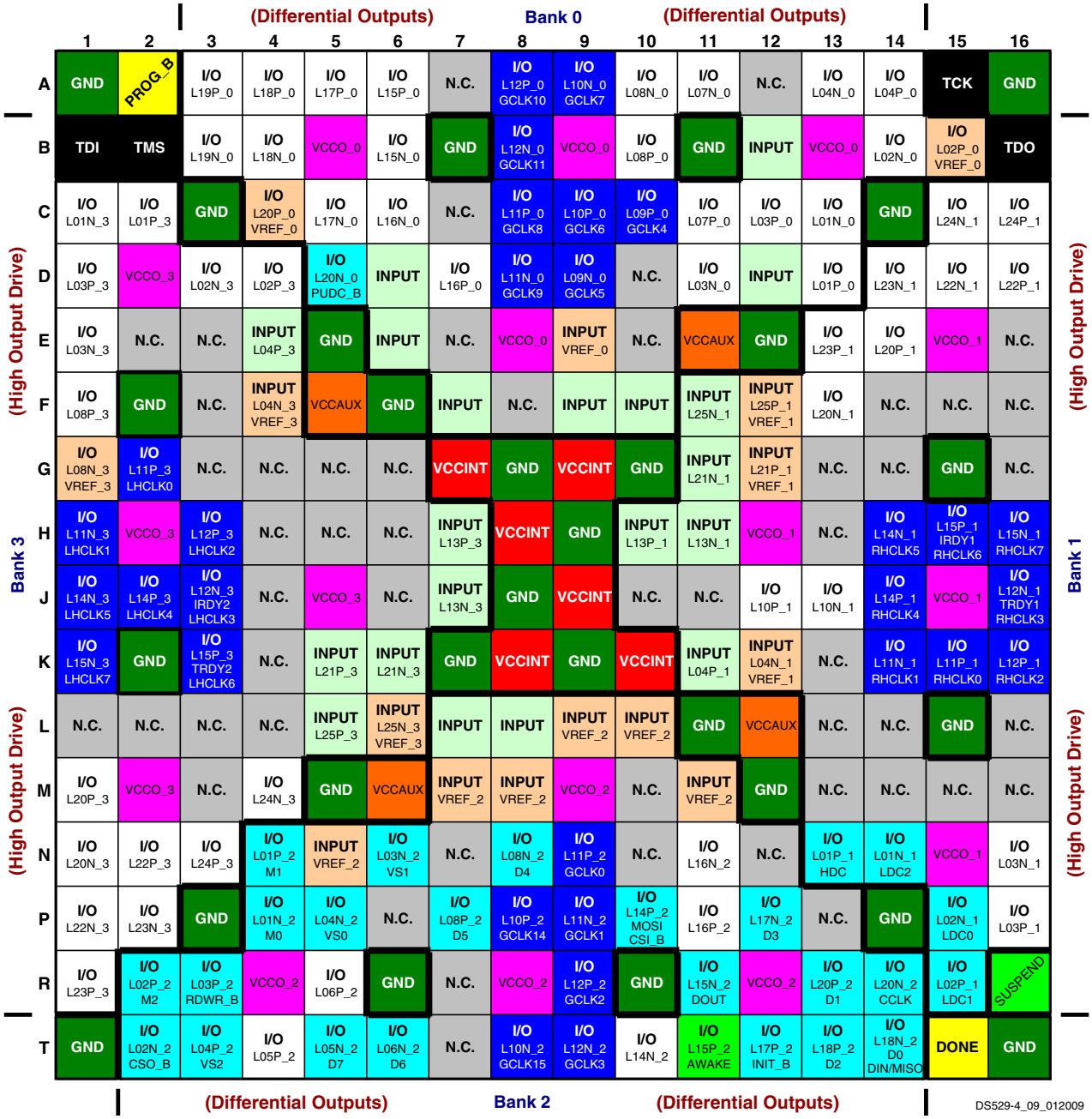


Figure 20: **XC3S50AN FTG256 Package Footprint (Top View)**

53	**I/O:** Unrestricted, general-purpose user I/O	25	**DUAL:** Configuration pins, then possible user I/O	15	**VREF:** User I/O or input voltage reference for bank	2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
20	**INPUT:** Unrestricted, general-purpose input pin	30	**CLK:** User I/O, input, or global buffer input	16	**VCCO:** Output voltage supply for bank		
2	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	6	**VCCINT:** Internal core supply voltage (+1.2V)		
51	**N.C.:** Not connected (XC3S50AN only)	28	**GND:** Ground	4	**VCCAUX:** Auxiliary supply voltage		

FGG400: 400-Ball Fine-Pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FGG400, supports the XC3S400AN FPGA as shown in Table 76 and Figure 22.

Table 76 lists all the FGG400 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type (as defined in Table 62).

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 76: **Spartan-3AN FGG400 Pinout**

Bank	Pin Name	FGG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK

Table 76: **Spartan-3AN FGG400 Pinout *(Cont'd)***

Bank	Pin Name	FGG400 Ball	Type
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
1	IO_L25N_1/RHCLK7	K19	RHCLK
1	IO_L25P_1/IRDY1/RHCLK6	K20	RHCLK
1	IO_L26N_1/A11	J22	DUAL
1	IO_L26P_1/A10	K22	DUAL
1	IO_L28N_1	L19	I/O
1	IO_L28P_1	L18	I/O
1	IO_L29N_1/A13	J20	DUAL
1	IO_L29P_1/A12	J21	DUAL
1	IO_L30N_1/A15	G22	DUAL
1	IO_L30P_1/A14	H22	DUAL
1	IO_L32N_1	K18	I/O
1	IO_L32P_1	K17	I/O
1	IO_L33N_1/A17	H20	DUAL
1	IO_L33P_1/A16	H21	DUAL
1	IO_L34N_1/A19	F21	DUAL
1	IO_L34P_1/A18	F22	DUAL
1	IO_L36N_1	G20	I/O
1	IO_L36P_1	G19	I/O
1	IO_L37N_1	H19	I/O
1	IO_L37P_1	J18	I/O
1	IO_L38N_1	F20	I/O
1	IO_L38P_1	E20	I/O
1	IO_L40N_1	F18	I/O
1	IO_L40P_1	F19	I/O
1	IO_L41N_1	D22	I/O
1	IO_L41P_1	E22	I/O
1	IO_L42N_1	D20	I/O
1	IO_L42P_1	D21	I/O
1	IO_L44N_1/A21	C21	DUAL
1	IO_L44P_1/A20	C22	DUAL
1	IO_L45N_1/A23	B21	DUAL
1	IO_L45P_1/A22	B22	DUAL
1	IO_L46N_1/A25	G17	DUAL
1	IO_L46P_1/A24	G18	DUAL
1	IP_L04N_1/VREF_1	R16	VREF
1	IP_L04P_1	R15	INPUT
1	IP_L08N_1	P16	INPUT
1	IP_L08P_1	P15	INPUT
1	IP_L12N_1/VREF_1	R18	VREF
1	IP_L12P_1	R17	INPUT

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
1	IP_L16N_1/VREF_1	N16	VREF
1	IP_L16P_1	N15	INPUT
1	IP_L23N_1	M16	INPUT
1	IP_L23P_1	M17	INPUT
1	IP_L27N_1	L16	INPUT
1	IP_L27P_1/VREF_1	M15	VREF
1	IP_L31N_1	K16	INPUT
1	IP_L31P_1	L15	INPUT
1	IP_L35N_1	K15	INPUT
1	IP_L35P_1/VREF_1	K14	VREF
1	IP_L39N_1	H18	INPUT
1	IP_L39P_1	H17	INPUT
1	IP_L43N_1/VREF_1	J15	VREF
1	IP_L43P_1	J16	INPUT
1	IP_L47N_1	H15	INPUT
1	IP_L47P_1/VREF_1	H16	VREF
1	VCCO_1	E21	VCCO
1	VCCO_1	J17	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	P17	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	V21	VCCO
2	IO_L01N_2/M0	W5	DUAL
2	IO_L01P_2/M1	V6	DUAL
2	IO_L02N_2/CSO_B	Y4	DUAL
2	IO_L02P_2/M2	W4	DUAL
2	IO_L03N_2	AA3	I/O
2	IO_L03P_2	AB2	I/O
2	IO_L04N_2	AA4	I/O
2	IO_L04P_2	AB3	I/O
2	IO_L05N_2	Y5	I/O
2	IO_L05P_2	W6	I/O
2	IO_L06N_2	AB5	I/O
2	IO_L06P_2	AB4	I/O
2	IO_L07N_2	Y6	I/O
2	IO_L07P_2	W7	I/O
2	IO_L08N_2	AB6	I/O
2	IO_L08P_2	AA6	I/O
2	IO_L09N_2/VS2	W9	DUAL
2	IO_L09P_2/RDWR_B	V9	DUAL

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
2	IO_L10N_2	AB7	I/O
2	IO_L10P_2	Y7	I/O
2	IO_L11N_2/VS0	Y8	DUAL
2	IO_L11P_2/VS1	W8	DUAL
2	IO_L12N_2	AB8	I/O
2	IO_L12P_2	AA8	I/O
2	IO_L13N_2	Y10	I/O
2	IO_L13P_2	V10	I/O
2	IO_L14N_2/D6	AB9	DUAL
2	IO_L14P_2/D7	Y9	DUAL
2	IO_L15N_2	AB10	I/O
2	IO_L15P_2	AA10	I/O
2	IO_L16N_2/D4	AB11	DUAL
2	IO_L16P_2/D5	Y11	DUAL
2	IO_L17N_2/GCLK13	V11	GCLK
2	IO_L17P_2/GCLK12	U11	GCLK
2	IO_L18N_2/GCLK15	Y12	GCLK
2	IO_L18P_2/GCLK14	W12	GCLK
2	IO_L19N_2/GCLK1	AB12	GCLK
2	IO_L19P_2/GCLK0	AA12	GCLK
2	IO_L20N_2/GCLK3	U12	GCLK
2	IO_L20P_2/GCLK2	V12	GCLK
2	IO_L21N_2	Y13	I/O
2	IO_L21P_2	AB13	I/O
2	IO_L22N_2/MOSI/CSI_B	AB14	DUAL
2	IO_L22P_2	AA14	I/O
2	IO_L23N_2	Y14	I/O
2	IO_L23P_2	W13	I/O
2	IO_L24N_2/DOUT	AA15	DUAL
2	IO_L24P_2/AWAKE	AB15	PWR MGMT
2	IO_L25N_2	Y15	I/O
2	IO_L25P_2	W15	I/O
2	IO_L26N_2/D3	U13	DUAL
2	IO_L26P_2/INIT_B	V13	DUAL
2	IO_L27N_2	Y16	I/O
2	IO_L27P_2	AB16	I/O
2	IO_L28N_2/D1	Y17	DUAL
2	IO_L28P_2/D2	AA17	DUAL
2	IO_L29N_2	AB18	I/O
2	IO_L29P_2	AB17	I/O

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
2	IO_L30N_2	V15	I/O
2	IO_L30P_2	V14	I/O
2	IO_L31N_2	V16	I/O
2	IO_L31P_2	W16	I/O
2	IO_L32N_2	AA19	I/O
2	IO_L32P_2	AB19	I/O
2	IO_L33N_2	V17	I/O
2	IO_L33P_2	W18	I/O
2	IO_L34N_2	W17	I/O
2	IO_L34P_2	Y18	I/O
2	IO_L35N_2	AA21	I/O
2	IO_L35P_2	AB21	I/O
2	IO_L36N_2/CCLK	AA20	DUAL
2	IO_L36P_2/D0/DIN/MISO	AB20	DUAL
2	IP_2	P12	INPUT
2	IP_2	R10	INPUT
2	IP_2	R11	INPUT
2	IP_2	R9	INPUT
2	IP_2	T13	INPUT
2	IP_2	T14	INPUT
2	IP_2	T9	INPUT
2	IP_2	U10	INPUT
2	IP_2	U15	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ◆	U16	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ◆	U7	INPUT
2	IP_2	U8	INPUT
2	IP_2	V7	INPUT
2	IP_2/VREF_2	R12	VREF
2	IP_2/VREF_2	R13	VREF
2	IP_2/VREF_2	R14	VREF
2	IP_2/VREF_2	T10	VREF
2	IP_2/VREF_2	T11	VREF
2	IP_2/VREF_2	T15	VREF
2	IP_2/VREF_2	T16	VREF
2	IP_2/VREF_2	T7	VREF
2	XC3S1400AN: IP_2/VREF_2 XC3S700AN: N.C. ◆	T8	VREF
2	IP_2/VREF_2	V8	VREF

FGG676: 676-Ball Fine-Pitch Ball Grid Array

The 676-ball fine-pitch ball grid array, FGG676, supports the XC3S1400AN FPGA.

Table 82 lists all the FGG676 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type (as defined in Table 62).

The XC3S1400AN has 17 unconnected balls, indicated as N.C. in Table 82 and Figure 24.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 82: **Spartan-3AN FGG676 Pinout**

Bank	Pin Name	FGG676 Ball	Type
0	IO_L01N_0	F20	I/O
0	IO_L01P_0	G20	I/O
0	IO_L02N_0	F19	I/O
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L05N_0	C22	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L06P_0	D23	I/O
0	IO_L07N_0	A22	I/O
0	IO_L07P_0	B23	I/O
0	IO_L08N_0	G17	I/O
0	IO_L08P_0	H17	I/O
0	IO_L09N_0	B21	I/O
0	IO_L09P_0	C21	I/O
0	IO_L10N_0	D21	I/O
0	IO_L10P_0	E21	I/O
0	IO_L11N_0	C20	I/O
0	IO_L11P_0	D20	I/O
0	IO_L12N_0	K16	I/O
0	IO_L12P_0	J16	I/O
0	IO_L13N_0	E17	I/O
0	IO_L13P_0	F17	I/O
0	IO_L14N_0	A20	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L15N_0	A19	I/O
0	IO_L15P_0	B19	I/O
0	IO_L16N_0	H15	I/O
0	IO_L16P_0	G15	I/O
0	IO_L17N_0	C18	I/O
0	IO_L17P_0	D18	I/O

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
0	IO_L18N_0	A18	I/O
0	IO_L18P_0	B18	I/O
0	IO_L19N_0	B17	I/O
0	IO_L19P_0	C17	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L20P_0	F15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L22N_0	C15	I/O
0	IO_L22P_0	D16	I/O
0	IO_L23N_0	A15	I/O
0	IO_L23P_0	B15	I/O
0	IO_L24N_0	F14	I/O
0	IO_L24P_0	E14	I/O
0	IO_L25N_0/GCLK5	J14	GCLK
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L27N_0/GCLK9	G13	GCLK
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L29N_0	B12	I/O
0	IO_L29P_0	A12	I/O
0	IO_L30N_0	C12	I/O
0	IO_L30P_0	D13	I/O
0	IO_L31N_0	F12	I/O
0	IO_L31P_0	E12	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IO_L32P_0	C11	I/O

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
2	IO_L15N_2	AC9	I/O
2	IO_L15P_2	AB9	I/O
2	IO_L16N_2	W12	I/O
2	IO_L16P_2	V12	I/O
2	IO_L17N_2/VS2	AA12	DUAL
2	IO_L17P_2/RDWR_B	Y12	DUAL
2	IO_L18N_2	AF8	I/O
2	IO_L18P_2	AE8	I/O
2	IO_L19N_2/VS0	AF9	DUAL
2	IO_L19P_2/VS1	AE9	DUAL
2	IO_L20N_2	W13	I/O
2	IO_L20P_2	V13	I/O
2	IO_L21N_2	AC12	I/O
2	IO_L21P_2	AB12	I/O
2	IO_L22N_2/D6	AF10	DUAL
2	IO_L22P_2/D7	AE10	DUAL
2	IO_L23N_2	AC11	I/O
2	IO_L23P_2	AD11	I/O
2	IO_L24N_2/D4	AE12	DUAL
2	IO_L24P_2/D5	AF12	DUAL
2	IO_L25N_2/GCLK13	Y13	GCLK
2	IO_L25P_2/GCLK12	AA13	GCLK
2	IO_L26N_2/GCLK15	AE13	GCLK
2	IO_L26P_2/GCLK14	AF13	GCLK
2	IO_L27N_2/GCLK1	AA14	GCLK
2	IO_L27P_2/GCLK0	Y14	GCLK
2	IO_L28N_2/GCLK3	AE14	GCLK
2	IO_L28P_2/GCLK2	AF14	GCLK
2	IO_L29N_2	AC14	I/O
2	IO_L29P_2	AD14	I/O
2	IO_L30N_2/MOSI/CSI_B	AB15	DUAL
2	IO_L30P_2	AC15	I/O
2	IO_L31N_2	W15	I/O
2	IO_L31P_2	V14	I/O
2	IO_L32N_2/DOUT	AE15	DUAL
2	IO_L32P_2/AWAKE	AD15	PWR MGMT
2	IO_L33N_2	AD17	I/O
2	IO_L33P_2	AE17	I/O
2	IO_L34N_2/D3	Y15	DUAL
2	IO_L34P_2/INIT_B	AA15	DUAL

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
2	IO_L35N_2	U15	I/O
2	IO_L35P_2	V15	I/O
2	IO_L36N_2/D1	AE18	DUAL
2	IO_L36P_2/D2	AF18	DUAL
2	IO_L37N_2	AE19	I/O
2	IO_L37P_2	AF19	I/O
2	IO_L38N_2	AB16	I/O
2	IO_L38P_2	AC16	I/O
2	IO_L39N_2	AE20	I/O
2	IO_L39P_2	AF20	I/O
2	IO_L40N_2	AC19	I/O
2	IO_L40P_2	AD19	I/O
2	IO_L41N_2	AC20	I/O
2	IO_L41P_2	AD20	I/O
2	IO_L42N_2	U16	I/O
2	IO_L42P_2	V16	I/O
2	IO_L43N_2	Y17	I/O
2	IO_L43P_2	AA17	I/O
2	IO_L44N_2	AD21	I/O
2	IO_L44P_2	AE21	I/O
2	IO_L45N_2	AC21	I/O
2	IO_L45P_2	AD22	I/O
2	IO_L46N_2	V17	I/O
2	IO_L46P_2	W17	I/O
2	IO_L47N_2	AA18	I/O
2	IO_L47P_2	AB18	I/O
2	IO_L48N_2	AE23	I/O
2	IO_L48P_2	AF23	I/O
2	IO_L51N_2	AE25	I/O
2	IO_L51P_2	AF25	I/O
2	IO_L52N_2/CCLK	AE24	DUAL
2	IO_L52P_2/D0/DIN/MISO	AF24	DUAL
2	IP_2	AA19	INPUT
2	IP_2	AB13	INPUT
2	IP_2	AB17	INPUT
2	IP_2	AB20	INPUT
2	IP_2	AC7	INPUT
2	IP_2	AC13	INPUT
2	IP_2	AC17	INPUT
2	IP_2	AC18	INPUT

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
3	IO_L30N_3	N4	I/O
3	IO_L30P_3	N5	I/O
3	IO_L31N_3	N2	I/O
3	IO_L31P_3	N1	I/O
3	IO_L32N_3/LHCLK1	N7	LHCLK
3	IO_L32P_3/LHCLK0	N6	LHCLK
3	IO_L33N_3/IRDY2/LHCLK3	P2	LHCLK
3	IO_L33P_3/LHCLK2	P1	LHCLK
3	IO_L34N_3/LHCLK5	P3	LHCLK
3	IO_L34P_3/LHCLK4	P4	LHCLK
3	IO_L35N_3/LHCLK7	P10	LHCLK
3	IO_L35P_3/TRDY2/LHCLK6	N9	LHCLK
3	IO_L36N_3	R2	I/O
3	IO_L36P_3/VREF_3	R1	VREF
3	IO_L37N_3	R4	I/O
3	IO_L37P_3	R3	I/O
3	IO_L38N_3	T4	I/O
3	IO_L38P_3	T3	I/O
3	IO_L39N_3	P6	I/O
3	IO_L39P_3	P7	I/O
3	IO_L40N_3	R6	I/O
3	IO_L40P_3	R5	I/O
3	IO_L41N_3	P9	I/O
3	IO_L41P_3	P8	I/O
3	IO_L42N_3	U4	I/O
3	IO_L42P_3	T5	I/O
3	IO_L43N_3	R9	I/O
3	IO_L43P_3/VREF_3	R10	VREF
3	IO_L44N_3	U2	I/O
3	IO_L44P_3	U1	I/O
3	IO_L45N_3	R7	I/O
3	IO_L45P_3	R8	I/O
3	IO_L47N_3	V2	I/O
3	IO_L47P_3	V1	I/O
3	IO_L48N_3	T9	I/O
3	IO_L48P_3	T10	I/O
3	IO_L49N_3	V5	I/O
3	IO_L49P_3	U5	I/O
3	IO_L51N_3	U6	I/O
3	IO_L51P_3	T7	I/O

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
3	IO_L52N_3	W4	I/O
3	IO_L52P_3	W3	I/O
3	IO_L53N_3	Y2	I/O
3	IO_L53P_3	Y1	I/O
3	IO_L55N_3	AA3	I/O
3	IO_L55P_3	AA2	I/O
3	IO_L56N_3	U8	I/O
3	IO_L56P_3	U7	I/O
3	IO_L57N_3	Y6	I/O
3	IO_L57P_3	Y5	I/O
3	IO_L59N_3	V6	I/O
3	IO_L59P_3	V7	I/O
3	IO_L60N_3	AC1	I/O
3	IO_L60P_3	AB1	I/O
3	IO_L61N_3	V8	I/O
3	IO_L61P_3	U9	I/O
3	IO_L63N_3	W6	I/O
3	IO_L63P_3	W7	I/O
3	IO_L64N_3	AC3	I/O
3	IO_L64P_3	AC2	I/O
3	IO_L65N_3	AD2	I/O
3	IO_L65P_3	AD1	I/O
3	IP_L04N_3/VREF_3	C1	VREF
3	IP_L04P_3	C2	INPUT
3	IP_L08N_3	D1	INPUT
3	IP_L08P_3	D2	INPUT
3	IP_L12N_3/VREF_3	H4	VREF
3	IP_L12P_3	G5	INPUT
3	IP_L16N_3	G1	INPUT
3	IP_L16P_3	G2	INPUT
3	IP_L20N_3/VREF_3	J2	VREF
3	IP_L20P_3	J3	INPUT
3	IP_L24N_3	K1	INPUT
3	IP_L24P_3	J1	INPUT
3	IP_L46N_3	V4	INPUT
3	IP_L46P_3	U3	INPUT
3	IP_L50N_3/VREF_3	W2	VREF
3	IP_L50P_3	W1	INPUT
3	IP_L54N_3	Y4	INPUT
3	IP_L54P_3	Y3	INPUT

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device. Noted that family is available in Pb-free packages only.
09/12/07	2.0.1	Minor updates to text.
09/24/07	2.1	Update thermal characteristics in Table 67.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that non-Pb-free packages may be available for selected devices. Updated thermal characteristics in Table 67. Updated links.
06/02/08	3.1	Add Package Overview section. Removed VREF and INPUT designations and diamond symbols on unconnected N.C. pins for XC3S700AN FGG484 in Table 78 and Figure 22 and for XC3S1400AN FGG676 in Table 82 and Figure 23.
11/19/09	3.2	Renamed package 'Footprint Area' to 'Body Area' throughout document. Noted in Introduction that references to Pb-free package code also apply to the Pb package. Added Pb packages to Table 65 and Table 66. Changed Body Area of TQ144/TQG144 packages in Table 65. Corrected bank designation for SUSPEND to VCCAUX. Noted that non-Pb-free (Pb) packages are available for selected devices. Updated Table 79 and Figure 22 for I/O vs. Input pin counts.
12/02/10	4.0	Upgraded Notice of Disclaimer.
04/01/11	4.1	Updated the CLK description in Table 62. In Table 64, added device/package combinations for the XC3S50AN and XC3S400AN in the FT(G)256 package and the XC3S1400AN in the FG(G)484 package. In Table 65, updated the maximum I/Os for the FG484/FGG484 packages, removed the Mass column, and updated Note 1. In Table 65, changed the FTG256 link from PK115_FTG256, FGG676 link from PK111_FGG676, and the TQG144 link from PK126_TQG144. Completely replaced the section FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array with new information on the added device/package combinations and new figures and tables. Revised U16, U7, and T8 in Table 78. Added Table 80 and Table 81 and updated Figure 23.