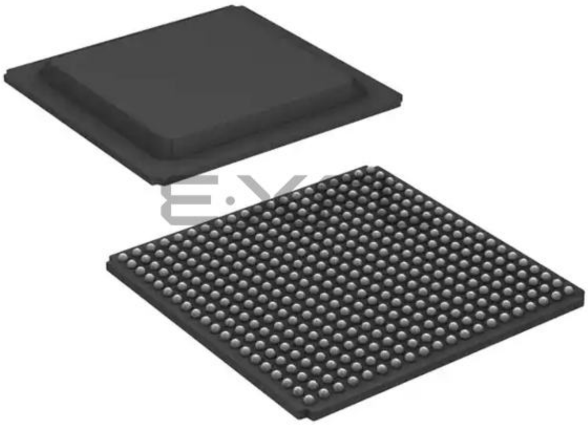

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	368640
Number of I/O	311
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400an-4fgg400c

Introduction

The Spartan®-3AN FPGA family combines the best attributes of a leading edge, low cost FPGA with nonvolatile technology across a broad range of densities. The family combines all the features of the Spartan-3A FPGA family plus leading technology in-system Flash memory for configuration and nonvolatile data storage.

The Spartan-3AN FPGAs are part of the Extended Spartan-3A family, which also includes the Spartan-3A FPGAs and the higher density Spartan-3A DSP FPGAs. The Spartan-3AN FPGA family is excellent for space-constrained applications such as blade servers, medical devices, automotive infotainment, telematics, GPS, and other small consumer products. Combining FPGA and Flash technology minimizes chip count, PCB traces and overall size while increasing system reliability.

The Spartan-3AN FPGA internal configuration interface is completely self-contained, increasing design security. The family maintains full support for external configuration. The Spartan-3AN FPGA is the world's first nonvolatile FPGA with MultiBoot, supporting two or more configuration files in one device, allowing alternative configurations for field upgrades, test modes, or multiple system configurations.

Features

- The new standard for low cost nonvolatile FPGA solutions
- Eliminates traditional nonvolatile FPGA limitations with the advanced 90 nm Spartan-3A device feature set
  - Memory, multipliers, DCMs, SelectIO, hot swap, power management, etc.
- Integrated robust configuration memory
  - Saves board space
  - Improves ease-of-use
  - Simplifies design
  - Reduces support issues
- Plentiful amounts of nonvolatile memory available to the user
  - Up to 11+ Mb available
  - MultiBoot support
  - Embedded processing and code shadowing
  - Scratchpad memory
- Robust 100K Flash memory program/erase cycles
- 20 years Flash memory data retention
- Security features provide bitstream anti-cloning protection
  - Buried configuration interface
  - Unique Device DNA serial number in each device for design Authentication to prevent unauthorized copying
  - Flash memory sector protection and lockdown
- Configuration watchdog timer automatically recovers from configuration errors
- Suspend mode reduces system power consumption
  - Retains all design state and FPGA configuration data
  - Fast response time, typically less than 100 µs
- Full hot-swap compliance
- Multi-voltage, multi-standard SelectIO™ interface pins
  - Up to 502 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTL, HSTL, and SSTL single-ended signal standards
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Up to 24 mA output drive
  - 3.3V ±10% compatibility and hot swap compliance
  - 622+ Mb/s data transfer rate per I/O
  - DDR/DDR2 SDRAM support up to 400 Mb/s
  - LVDS, RSDS, mini-LVDS, PPDS, and HSTL/SSTL differential I/O
- Abundant, flexible logic resources
  - Densities up to 25,344 logic cells
  - Optional shift register or distributed RAM support
  - Enhanced 18 x 18 multipliers with optional pipeline
- Hierarchical SelectRAM™ memory architecture
  - Up to 576 Kbits of dedicated block RAM
  - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
- Eight global clocks and eight additional clocks per each half of device, plus abundant low-skew routing
- Complete Xilinx® ISE® and WebPACK™ software development system support
- MicroBlaze™ and PicoBlaze™ embedded processor cores
- Fully compliant 32-/64-bit 33 MHz PCI™ technology support
- Low-cost QFP and BGA Pb-free (RoHS) packaging options
  - Pin-compatible with the same packages in the Spartan-3A FPGA family

Table 2: **Summary of Spartan-3AN FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLBs	Slices	Distributed RAM Bits(1)	Block RAM Bits(1)	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs	Bitstream Size(1)	In-System Flash Bits
XC3S50AN	50K	1,584	176	704	11K	54K	3	2	144	64	427K	1M
XC3S200AN	200K	4,032	448	1,792	28K	288K	16	4	195	90	1,168K	4M
XC3S400AN	400K	8,064	896	3,584	56K	360K	20	4	311	142	1,842K	4M
XC3S700AN	700K	13,248	1,472	5,888	92K	360K	20	8	372	165	2,669K	8M
XC3S1400AN	1400K	25,344	2,816	11,264	176K	576K	32	8	502	227	4,644K	16M

Notes:
1. By convention, one Kb is equivalent to 1,024 bits and one Mb is equivalent to 1,024 Kb.

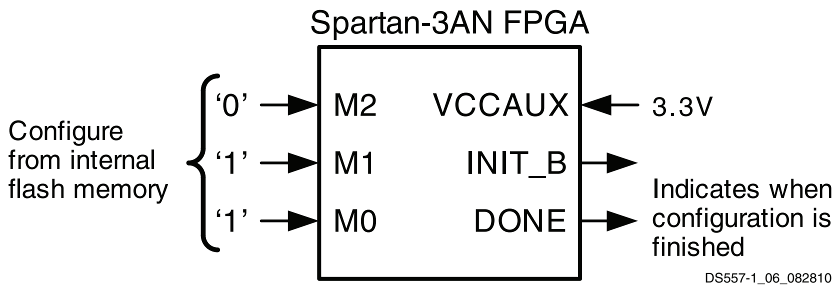

Figure 2: **Spartan-3AN FPGA Configuration Interface from Internal SPI Flash Memory**

Configuration

Spartan-3AN FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored on-chip in nonvolatile Flash memory, or externally in a PROM or some other nonvolatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Configure from internal SPI Flash memory (Figure 2)
  - Completely self-contained
  - Reduced board space
  - Easy-to-use configuration interface
- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an external industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary-Scan (JTAG), typically downloaded from a processor or system tester

The MultiBoot feature stores multiple configuration files in the on-chip Flash, providing extended life with field upgrades. MultiBoot also supports multiple system solutions with a single board to minimize inventory and simplify the addition of new features, even in the field. Flexibility is maintained to do additional MultiBoot configurations via the external configuration method.

The Spartan-3AN device authentication protocol prevents cloning. Design cloning, unauthorized overbuilding, and complete reverse engineering have driven device security requirements to higher and higher levels. Authentication moves the security from bitstream protection to the next generation of design-level security protecting both the design and embedded microcode. The authentication algorithm is entirely user defined, implemented using FPGA logic. Every product, generation, or design can have a different algorithm and functionality to enhance security.

In-System Flash Memory

Each Spartan-3AN FPGA contains abundant integrated SPI serial Flash memory, shown in Table 3, used primarily to store the FPGA's configuration bitstream. However, the Flash memory array is large enough to store at least two MultiBoot FPGA configuration bitstreams or nonvolatile data required by the FPGA application, such as code-shadowed MicroBlaze processor applications.

Table 3: **Spartan-3AN Device In-System Flash Memory**

Part Number	Total Flash Memory (Bits)	FPGA Bitstream (Bits)	Additional Flash Memory (Bits)(1)
XC3S50AN	1,081,344	437,312	642,048
XC3S200AN	4,325,376	1,196,128	3,127,872
XC3S400AN	4,325,376	1,886,560	2,437,248
XC3S700AN	8,650,752	2,732,640	5,917,824
XC3S1400AN	17,301,504	4,755,296	12,545,280

Notes:

1. Aligned to next available page location.

After configuration, the FPGA design has full access to the in-system Flash memory via an internal SPI interface; the control logic is implemented with FPGA logic. Additionally, the FPGA application itself can store nonvolatile data or provide live, in-system Flash updates.

The Spartan-3AN device in-system Flash memory supports leading-edge serial Flash features.

- Small page size (264 or 528 bytes) simplifies nonvolatile data storage
- Randomly accessible, byte addressable
- Up to 66 MHz serial data transfers
- SRAM page buffers
  - Read Flash data while programming another Flash page
  - EEPROM-like byte write functionality
  - Two buffers in most devices, one in XC3S50AN
- Page, Block, and Sector Erase

Spartan-3AN FPGA Design Documentation

The functionality of the Spartan®-3AN FPGA family is described in the following documents. The topics covered in each guide are listed below:

- **DS706: Extended Spartan-3A Family Overview**
- **UG331: Spartan-3 Generation FPGA User Guide**
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash
    - Master SPI Mode using SPI Serial Flash PROM
    - Internal Master SPI Mode
    - Master BPI Mode using Parallel NOR Flash
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA
- **UG333: Spartan-3AN FPGA In-System Flash User Guide**
  - For FPGA applications that write to or read from the In-System Flash memory after configuration
  - SPI_ACCESS interface
  - In-System Flash memory architecture
  - Read, program, and erase commands
  - Status registers
  - Sector Protection and Sector Lockdown features
  - Security Register with Unique Identifier

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Spartan-3AN FPGA Starter Kit

For specific hardware examples, please see the Spartan-3AN FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3AN FPGA Starter Kit Board Page**
  http://www.xilinx.com/s3anstarter
- **UG334: Spartan-3AN FPGA Starter Kit User Guide**

DC Electrical Characteristics

In this section, specifications can be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3AN devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 6: Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 6: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	$V_{CCO} + 0.5$	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$–0.5V < V_{IN} < (V_{CCO} + 0.5V)$[1]	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
1. For soldering guidelines, see UG112: Device Package User Guide and XAPP427: Implementation and Solder Reflow Guidelines for Pb-Free Packages.

Single-Ended I/O Standards

Table 13: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers(2)			V_{REF}			V_{IL}	V_{IH}(3)
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33(4)	3.0	3.3	3.6				0.8	2.0
LVCMOS25(4)(5)	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3(6)	3.0	3.3	3.6				$0.3 \bullet V_{CCO}$	$0.5 \bullet V_{CCO}$
PCI66_3(6)	3.0	3.3	3.6				$0.3 \bullet V_{CCO}$	$0.5 \bullet V_{CCO}$
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III	1.4	1.5	1.6	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL2_I	2.3	2.5	2.7	1.13	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL2_II	2.3	2.5	2.7	1.13	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVCMOS25 inputs and for PCI™ I/O standards.
3. For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 6.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVCMOS33 standard. The Dual-Purpose configuration pins use the LVCMOS standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see www.xilinx.com/pci. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 21: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, with DCM(3)	XC3S50AN	3.18	3.42	ns
			XC3S200AN	3.21	3.27	ns
			XC3S400AN	2.97	3.33	ns
			XC3S700AN	3.39	3.50	ns
			XC3S1400AN	3.51	3.99	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, without DCM	XC3S50AN	4.59	5.02	ns
			XC3S200AN	4.88	5.24	ns
			XC3S400AN	4.68	5.12	ns
			XC3S700AN	4.97	5.34	ns
			XC3S1400AN	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 26. If the latter is true, *add* the appropriate Output adjustment from Table 29.
3. DCM output jitter is included in all measurements.

Table 30: **Test Methods for Timing Measurement at I/Os *(Cont'd)***

Signal Standard (IOSTANDARD)	Inputs			Outputs(2)		Inputs and Outputs
	V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Differential						
LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
MINI_LVDS_33	–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
LVPECL_33	–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
RSDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
RSDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
TMDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	3.3	V_{ICM}
PPDS_25	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
PPDS_33	–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
DIFF_HSTL_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.75	V_{ICM}
DIFF_HSTL_III	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}
DIFF_HSTL_I_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_II_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_HSTL_III_18	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.8	V_{ICM}
DIFF_SSTL18_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL18_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	0.9	V_{ICM}
DIFF_SSTL2_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL2_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.25	V_{ICM}
DIFF_SSTL3_I	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}
DIFF_SSTL3_II	–	V_{ICM} – 0.5	V_{ICM} + 0.5	50	1.5	V_{ICM}

Notes:

1. Descriptions of the relevant symbols are as follows:
   V_{REF} – The reference voltage for setting the input switching threshold
   V_{ICM} – The common mode input voltage
   V_M – Voltage of measurement point on signal transition
   V_L – Low-level test voltage at Input pin
   V_H – High-level test voltage at Input pin
   R_T – Effective termination resistance, which takes on a value of 1 MΩ when no parallel termination is required
   V_T – Termination voltage
2. The load capacitance (C_L) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification. For information on PCI IP solutions, see www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

The capacitive load (C_L) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a C_L value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

Block RAM Timing

Table 38: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{RCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.06	–	2.49	ns
Setup Times						
T_{RCCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.32	–	0.36	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.28	–	0.31	–	ns
T_{RCCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.69	–	0.77	–	ns
T_{RCCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.12	–	1.26	–	ns
Hold Times						
T_{RCKC_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCKD_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCKC_ENB}	Hold time on the EN input after the active transition at the CLK input	0	–	0	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0	–	0	–	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.56	–	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.56	–	1.79	–	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency	0	320	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10.

DNA Port Timing

Table 46: **DNA_PORT Interface Timing**

Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, the maximum READ pulse width is 10 µs.

Internal SPI Access Port Timing

Table 47: **SPI_ACCESS Interface Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
T_{SPICCK_MOSI}	Setup time on MOSI before the active edge of CLK	4.47	–	5.0	–	ns
T_{SPICKC_MOSI}	Hold time on MOSI after the active edge of CLK	4.03	–	4.5	–	ns
T_{CSB}	CSB High time	50	–	50	–	ns
T_{SPICCK_CSB}	Setup time on CSB before the active edge of CLK	7.15	–	8.0	–	ns
T_{SPICCK_CSB}	Hold time on CSB after the active edge of CLK	7.15	–	8.0	–	ns
T_{SPICKO_MISO}	Clock-to-output delay on MISO after active edge of CLK	–	14.3	–	16.0	ns
F_{SPICLK}	CLK frequency	–	50	–	50	MHz
$F_{SPICAR1}$	CLK frequency for Continuous Array Read command	–	50	–	50	MHz
$F_{SPICAR1}$	CLK frequency for Continuous Array Read command, reduced initial latency	–	33	–	33	MHz
$T_{SPICLKL}$	CLK High time	–	∞	–	∞	ns
$T_{SPICLKH}$	CLK Low time	6.8	∞	6.8	∞	ns

Notes:

1. For details on using SPI_ACCESS and the In-System Flash memory, see UG333 *Spartan-3AN FPGA In-System Flash User Guide*.

Table 54: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Master Serial and Slave Serial Mode Timing

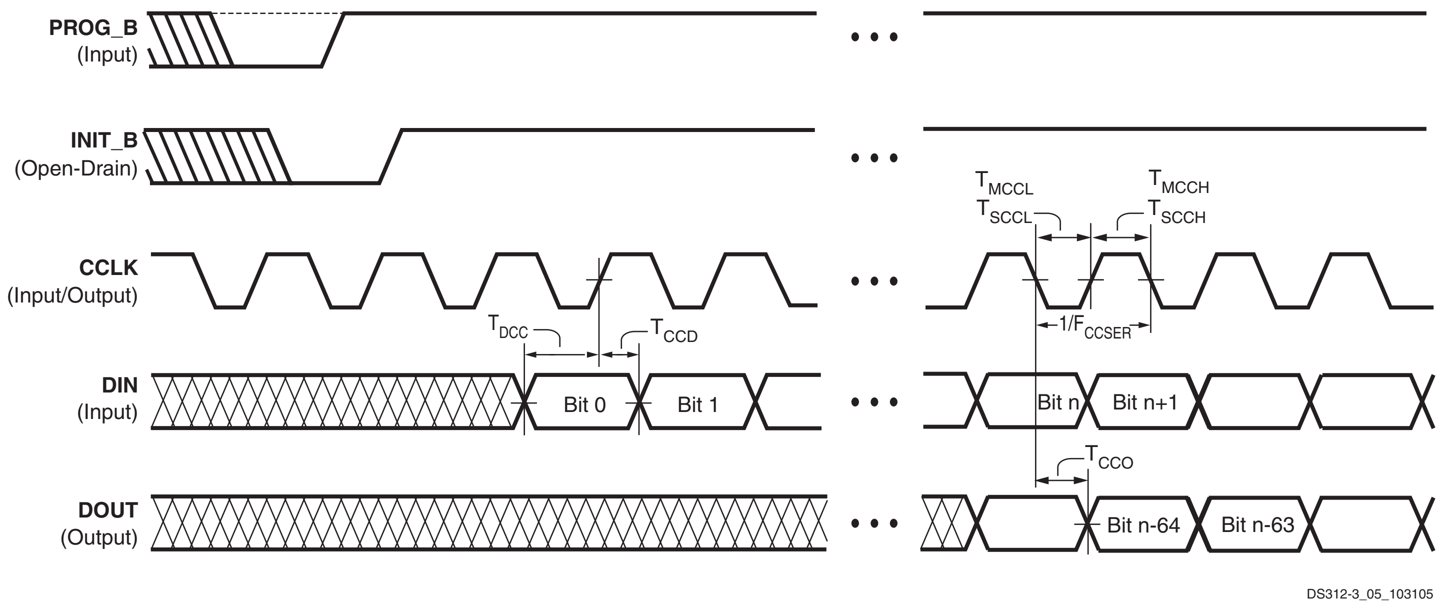

Figure 14: **Waveforms for Master Serial and Slave Serial Configuration**

Table 55: **Timing for the Master Serial and Slave Serial Configuration Modes**

Symbol	Description		Slave/ Master	All Speed Grades		Units
				Min	Max	
Clock-to-Output Times						
T_{CCO}	The time from the falling transition on the CCLK pin to data appearing at the DOUT pin		Both	1.5	10	ns
Setup Times						
T_{DCC}	The time from the setup of data at the DIN pin to the rising transition at the CCLK pin		Both	7	–	ns
Hold Times						
T_{CCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the DIN pin		Master	0	–	ns
			Slave	1.0		
Clock Timing						
T_{CCH}	High pulse width at the CCLK input pin		Master	See Table 53		
			Slave	See Table 54		
T_{CCL}	Low pulse width at the CCLK input pin		Master	See Table 53		
			Slave	See Table 54		
F_{CCSER}	Frequency of the clock signal at the CCLK input pin(2)	No bitstream compression	Slave	0	100	MHz
		With bitstream compression		0	100	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10.
2. For serial configuration with a daisy-chain of multiple FPGAs, the maximum limit is 25 MHz.

Table 58: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:
1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Byte Peripheral Interface (BPI) Configuration Timing

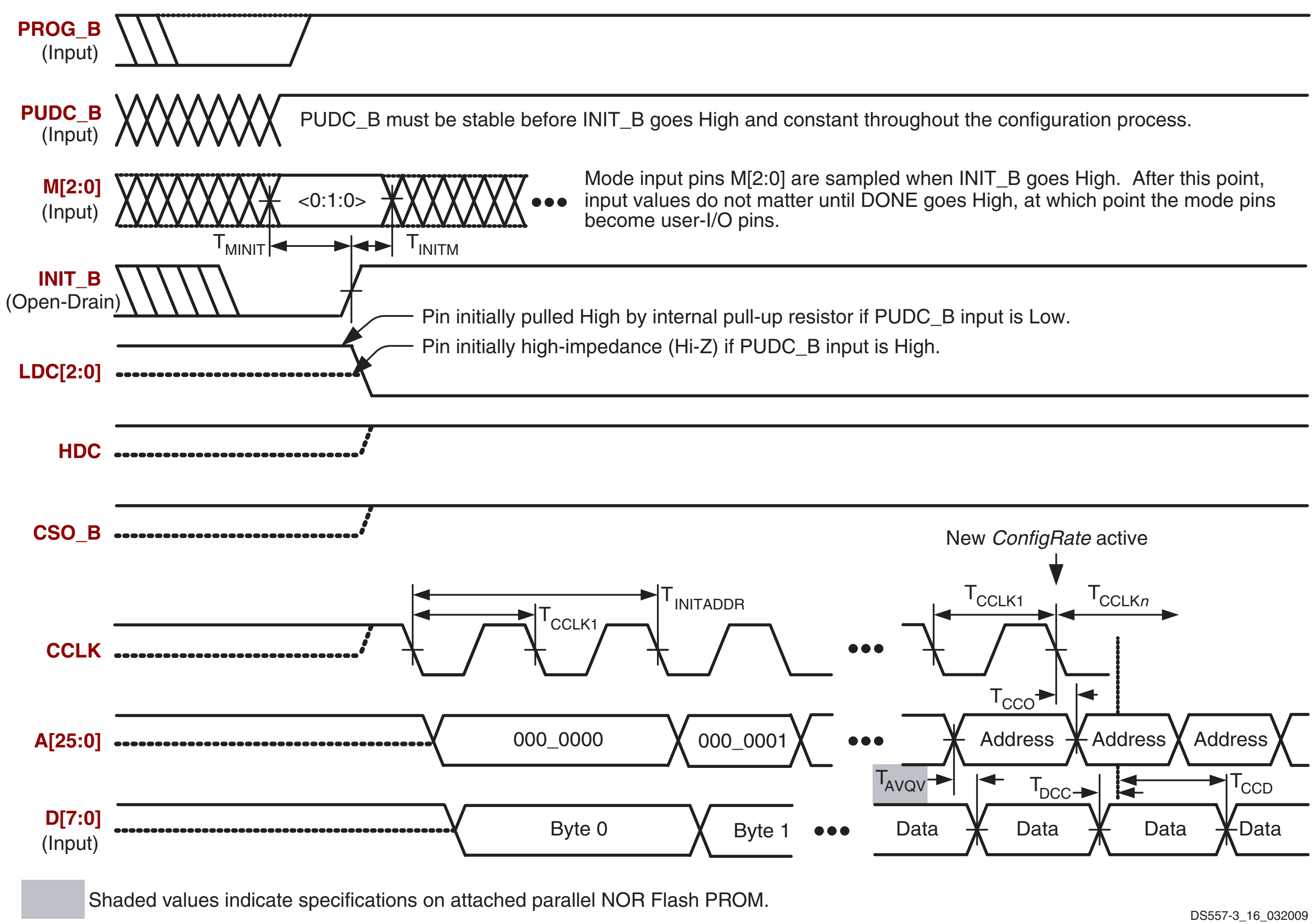

Figure 17: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration**

Table 62: **Types of Pins on Spartan-3AN FPGAs *(Cont'd)***

Type with Color Code	Description	Pin Name(s) in Type[1]
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a dual-purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. The In-System Flash memory is powered by VCCAUX. All must be connected to +3.3V.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 63.

Table 63: **Power and Ground Supply Pins by Package**

Package	VCCINT	VCCAUX	VCCO	GND
TQG144	4	4	8	13
FTG256	6	4	16	28
FGG400	9	8	22	43
FGG484	15	10	24	53
FGG676	23	14	36	77

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/Os depend on the device type and the package in which it is available, as shown in Table 64. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. AWAKE is counted here as a dual-purpose I/O pin. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—N.C.—pins on the device.

Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in the top or bottom banks (I/O banks 0 and 2). Inputs are unrestricted. For more details, see the "Using I/O Resources" chapter in UG331.

TQG144: 144-lead Thin Quad Flat Package

The XC3S50AN is available in the 144-lead thin quad flat package, TQG144.

Table 68 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type (as defined in Table 62). The XC3S50AN does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 68: **Spartan-3AN TQG144 Pinout**

Bank	Pin Name	Pin	Type
0	IO_0	P142	I/O
0	IO_L01N_0	P111	I/O
0	IO_L01P_0	P110	I/O
0	IO_L02N_0	P113	I/O
0	IO_L02P_0/VREF_0	P112	VREF
0	IO_L03N_0	P117	I/O
0	IO_L03P_0	P115	I/O
0	IO_L04N_0	P116	I/O
0	IO_L04P_0	P114	I/O
0	IO_L05N_0	P121	I/O
0	IO_L05P_0	P120	I/O
0	IO_L06N_0/GCLK5	P126	GCLK
0	IO_L06P_0/GCLK4	P124	GCLK
0	IO_L07N_0/GCLK7	P127	GCLK
0	IO_L07P_0/GCLK6	P125	GCLK
0	IO_L08N_0/GCLK9	P131	GCLK
0	IO_L08P_0/GCLK8	P129	GCLK
0	IO_L09N_0/GCLK11	P132	GCLK
0	IO_L09P_0/GCLK10	P130	GCLK
0	IO_L10N_0	P135	I/O
0	IO_L10P_0	P134	I/O
0	IO_L11N_0	P139	I/O
0	IO_L11P_0	P138	I/O
0	IO_L12N_0/PUDC_B	P143	DUAL
0	IO_L12P_0/VREF_0	P141	VREF
0	IP_0	P140	INPUT
0	IP_0/VREF_0	P123	VREF
0	VCCO_0	P119	VCCO
0	VCCO_0	P136	VCCO
1	IO_1	P79	I/O
1	IO_L01N_1/LDC2	P78	DUAL
1	IO_L01P_1/HDC	P76	DUAL
1	IO_L02N_1/LDC0	P77	DUAL

Table 68: **Spartan-3AN TQG144 Pinout *(Cont'd)***

Bank	Pin Name	Pin	Type
1	IO_L02P_1/LDC1	P75	DUAL
1	IO_L03N_1	P84	I/O
1	IO_L03P_1	P82	I/O
1	IO_L04N_1/RHCLK1	P85	RHCLK
1	IO_L04P_1/RHCLK0	P83	RHCLK
1	IO_L05N_1/TRDY1/RHCLK3	P88	RHCLK
1	IO_L05P_1/RHCLK2	P87	RHCLK
1	IO_L06N_1/RHCLK5	P92	RHCLK
1	IO_L06P_1/RHCLK4	P90	RHCLK
1	IO_L07N_1/RHCLK7	P93	RHCLK
1	IO_L07P_1/IRDY1/RHCLK6	P91	RHCLK
1	IO_L08N_1	P98	I/O
1	IO_L08P_1	P96	I/O
1	IO_L09N_1	P101	I/O
1	IO_L09P_1	P99	I/O
1	IO_L10N_1	P104	I/O
1	IO_L10P_1	P102	I/O
1	IO_L11N_1	P105	I/O
1	IO_L11P_1	P103	I/O
1	IP_1/VREF_1	P80	VREF
1	IP_1/VREF_1	P97	VREF
1	VCCO_1	P86	VCCO
1	VCCO_1	P95	VCCO
2	IO_2/MOSI/CSI_B	P62	DUAL
2	IO_L01N_2/M0	P38	DUAL
2	IO_L01P_2/M1	P37	DUAL
2	IO_L02N_2/CSO_B	P41	DUAL
2	IO_L02P_2/M2	P39	DUAL
2	IO_L03N_2/VS1	P44	DUAL
2	IO_L03P_2/RDWR_B	P42	DUAL
2	IO_L04N_2/VS0	P45	DUAL
2	IO_L04P_2/VS2	P43	DUAL
2	IO_L05N_2/D7	P48	DUAL

Right Half of FGG400 Package (Top View)

Bank 0 (top, columns 11–18) · Bank 1 (right, rows B–W) · Bank 2 (bottom, columns 11–19)

	11	12	13	14	15	16	17	18	19	20
A	GND	I/O L13N_0	VCCAUX	I/O L07N_0	I/O L08N_0	I/O L05N_0	I/O L04N_0	I/O L01N_0	TCK	GND
B	I/O L14P_0	I/O L13P_0	I/O L11P_0	GND	I/O L08P_0	VCCO_0	I/O L04P_0 VREF_0	I/O L01P_0	I/O L38N_1 A25	I/O L38P_1 A24
C	I/O L14N_0	I/O L11N_0	I/O L10N_0 VREF_0	I/O L07P_0	I/O L06N_0	I/O L05P_0	I/O L02N_0	GND	I/O L37N_1 A23	I/O L37P_1 A22
D	I/O L15P_0 GCLK4	I/O L12P_0	VCCO_0	I/O L10P_0	I/O L06P_0	I/O L03P_0	I/O L02P_0 VREF_0	I/O L34N_1	VCCO_1	I/O L34P_1
E	I/O L15N_0 GCLK5	GND	I/O L09P_0	INPUT	I/O L03N_0	VCCAUX	TDO	I/O L33P_1	I/O L32N_1	I/O L32P_1
F	INPUT	I/O L12N_0	I/O L09N_0	INPUT	GND	I/O L36N_1 A21	I/O L33N_1	I/O L30N_1 A19	I/O L29N_1 A17	I/O L29P_1 A16
G	INPUT VREF_0	INPUT	INPUT	INPUT L39N_1	INPUT L39P_1 VREF_1	I/O L36P_1 A20	I/O L30P_1 A18	I/O L28P_1	GND	I/O L26N_1 A15
H	INPUT	INPUT	GND	INPUT L35N_1	INPUT L35P_1	VCCO_1	I/O L28N_1	I/O L25N_1 A13	I/O L25P_1 A12	I/O L26P_1 A14
J	GND	VCCINT	INPUT L31N_1	INPUT L31P_1 VREF_1	INPUT L27N_1	INPUT L27P_1	I/O L24P_1	I/O L22N_1 A11	I/O L22P_1 A10	I/O L21N_1 RHCLK7
K	VCCINT	GND	VCCAUX	INPUT L23N_1	INPUT L23P_1 VREF_1	I/O L24N_1	GND	I/O L20P_1 RHCLK4	VCCO_1	I/O L21P_1 IRDY1 RHCLK6
L	GND	VCCINT	INPUT L19N_1	INPUT L19P_1	I/O L16P_1 A8	I/O L16N_1 A9	I/O L20N_1 RHCLK5	I/O L18N_1 TRDY1 RHCLK3	I/O L18P_1 RHCLK2	GND
M	VCCINT	GND	INPUT L15N_1	INPUT L15P_1 VREF_1	INPUT L11N_1 VREF_1	INPUT L11P_1	I/O L14P_1 A6	I/O L14N_1 A7	I/O L17P_1 RHCLK0	I/O L17N_1 RHCLK1
N	GND	INPUT VREF_2	GND	INPUT VREF_1	I/O L12P_1 A2	VCCO_1	I/O L12N_1 A3	I/O L13P_1 A4	I/O L13N_1 A5	VCCAUX
P	INPUT VREF_2	INPUT	INPUT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L07P_1	I/O L07N_1	I/O L10P_1	GND	I/O L10N_1 VREF_1
R	VCCO_2	I/O L19N_2	I/O L23N_2	INPUT VREF_2	SUSPEND	I/O L03N_1 A1	I/O L08N_1	I/O L08P_1	I/O L09P_1	I/O L09N_1
T	INPUT	I/O L19P_2	I/O L23P_2	I/O L25N_2	I/O L27N_2	GND	I/O L03P_1 A0	I/O L05P_1	VCCO_1	I/O L05N_1
U	I/O L18P_2 GCLK2	GND	I/O L22P_2 AWAKE	VCCO_2	I/O L27P_2	I/O L29N_2	I/O L31N_2	I/O L02N_1 LDC0	I/O L06P_1	I/O L06N_1
V	I/O L17N_2 GCLK1	I/O L18N_2 GCLK3	I/O L22N_2 DOUT	I/O L25P_2	I/O L26N_2 D1	I/O L29P_2	I/O L31P_2	GND	I/O L02P_1 LDC1	I/O L01N_1 LDC2
W	VCCO_2	I/O L20N_2 MOSI CSI_B	I/O L21N_2	I/O L24N_2 D3	GND	I/O L28N_2	VCCO_2	I/O L32P_2 D0 DIN/MISO	DONE	I/O L01P_1 HDC
Y	I/O L17P_2 GCLK0	I/O L20P_2	I/O L21P_2	I/O L24P_2 INIT_B	I/O L26P_2 D2	I/O L28P_2	I/O L30P_2	I/O L30N_2	I/O L32N_2 CCLK	GND

DS557_4_22_030911

Figure 22: **FGG400 Package Footprint (Top View)**

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
2	IO_L10N_2	AB7	I/O
2	IO_L10P_2	Y7	I/O
2	IO_L11N_2/VS0	Y8	DUAL
2	IO_L11P_2/VS1	W8	DUAL
2	IO_L12N_2	AB8	I/O
2	IO_L12P_2	AA8	I/O
2	IO_L13N_2	Y10	I/O
2	IO_L13P_2	V10	I/O
2	IO_L14N_2/D6	AB9	DUAL
2	IO_L14P_2/D7	Y9	DUAL
2	IO_L15N_2	AB10	I/O
2	IO_L15P_2	AA10	I/O
2	IO_L16N_2/D4	AB11	DUAL
2	IO_L16P_2/D5	Y11	DUAL
2	IO_L17N_2/GCLK13	V11	GCLK
2	IO_L17P_2/GCLK12	U11	GCLK
2	IO_L18N_2/GCLK15	Y12	GCLK
2	IO_L18P_2/GCLK14	W12	GCLK
2	IO_L19N_2/GCLK1	AB12	GCLK
2	IO_L19P_2/GCLK0	AA12	GCLK
2	IO_L20N_2/GCLK3	U12	GCLK
2	IO_L20P_2/GCLK2	V12	GCLK
2	IO_L21N_2	Y13	I/O
2	IO_L21P_2	AB13	I/O
2	IO_L22N_2/MOSI/CSI_B	AB14	DUAL
2	IO_L22P_2	AA14	I/O
2	IO_L23N_2	Y14	I/O
2	IO_L23P_2	W13	I/O
2	IO_L24N_2/DOUT	AA15	DUAL
2	IO_L24P_2/AWAKE	AB15	PWR MGMT
2	IO_L25N_2	Y15	I/O
2	IO_L25P_2	W15	I/O
2	IO_L26N_2/D3	U13	DUAL
2	IO_L26P_2/INIT_B	V13	DUAL
2	IO_L27N_2	Y16	I/O
2	IO_L27P_2	AB16	I/O
2	IO_L28N_2/D1	Y17	DUAL
2	IO_L28P_2/D2	AA17	DUAL
2	IO_L29N_2	AB18	I/O
2	IO_L29P_2	AB17	I/O

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
2	IO_L30N_2	V15	I/O
2	IO_L30P_2	V14	I/O
2	IO_L31N_2	V16	I/O
2	IO_L31P_2	W16	I/O
2	IO_L32N_2	AA19	I/O
2	IO_L32P_2	AB19	I/O
2	IO_L33N_2	V17	I/O
2	IO_L33P_2	W18	I/O
2	IO_L34N_2	W17	I/O
2	IO_L34P_2	Y18	I/O
2	IO_L35N_2	AA21	I/O
2	IO_L35P_2	AB21	I/O
2	IO_L36N_2/CCLK	AA20	DUAL
2	IO_L36P_2/D0/DIN/MISO	AB20	DUAL
2	IP_2	P12	INPUT
2	IP_2	R10	INPUT
2	IP_2	R11	INPUT
2	IP_2	R9	INPUT
2	IP_2	T13	INPUT
2	IP_2	T14	INPUT
2	IP_2	T9	INPUT
2	IP_2	U10	INPUT
2	IP_2	U15	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ◆	U16	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ◆	U7	INPUT
2	IP_2	U8	INPUT
2	IP_2	V7	INPUT
2	IP_2/VREF_2	R12	VREF
2	IP_2/VREF_2	R13	VREF
2	IP_2/VREF_2	R14	VREF
2	IP_2/VREF_2	T10	VREF
2	IP_2/VREF_2	T11	VREF
2	IP_2/VREF_2	T15	VREF
2	IP_2/VREF_2	T16	VREF
2	IP_2/VREF_2	T7	VREF
2	XC3S1400AN: IP_2/VREF_2 XC3S700AN: N.C. ◆	T8	VREF
2	IP_2/VREF_2	V8	VREF

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
VCCAUX	DONE	Y19	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A21	JTAG
VCCAUX	TDI	F5	JTAG
VCCAUX	TDO	E19	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	H11	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	P11	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P13	VCCINT

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L04N_1	W21	I/O
1	IO_L04P_1	W20	I/O
1	IO_L05N_1	AC25	I/O
1	IO_L05P_1	AD26	I/O
1	IO_L06N_1	AB26	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L07P_1	AB23	I/O
1	IO_L08N_1	V19	I/O
1	IO_L08P_1	V18	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L10N_1	U20	I/O
1	IO_L10P_1	V21	I/O
1	IO_L11N_1	AA25	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L13P_1	Y22	I/O
1	IO_L14N_1	T20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L15N_1	Y25	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L18N_1	V22	I/O
1	IO_L18P_1	W23	I/O
1	IO_L19N_1	V25	I/O
1	IO_L19P_1	V24	I/O
1	IO_L21N_1	U22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L22N_1	R20	I/O
1	IO_L22P_1	R19	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IO_L23P_1	U23	I/O
1	IO_L25N_1/A3	R22	DUAL

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
1	IO_L25P_1/A2	R21	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L26P_1/A4	T23	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L29P_1/A8	R25	DUAL
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L37N_1	N21	I/O
1	IO_L37P_1	P22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IO_L38P_1/A12	L24	DUAL
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L41N_1	K26	I/O
1	IO_L41P_1	K25	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L42P_1/A16	N20	DUAL
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L45N_1	M22	I/O
1	IO_L45P_1	M21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L50N_1	K21	I/O
1	IO_L50P_1	L22	I/O
1	IO_L51N_1	G24	I/O

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IP_2	AD16	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AF7	INPUT
2	IP_2	Y11	INPUT
2	IP_2/VREF_2	AA9	VREF
2	IP_2/VREF_2	AA20	VREF
2	IP_2/VREF_2	AB6	VREF
2	IP_2/VREF_2	AB10	VREF
2	IP_2/VREF_2	AC10	VREF
2	IP_2/VREF_2	AD12	VREF
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IP_2/VREF_2	AF22	VREF
2	IP_2/VREF_2	Y16	VREF
2	N.C.	AA8	N.C.
2	N.C.	AC5	N.C.
2	N.C.	AC22	N.C.
2	N.C.	AD5	N.C.
2	N.C.	Y18	N.C.
2	N.C.	Y19	N.C.
2	N.C.	AD23	N.C.
2	N.C.	W18	N.C.
2	N.C.	Y8	N.C.
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
3	IO_L01N_3	J9	I/O
3	IO_L01P_3	J8	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	H7	I/O
3	IO_L03P_3	G6	I/O

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L07P_3	E3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L11N_3	F2	I/O
3	IO_L11P_3	E1	I/O
3	IO_L13N_3	J6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L14N_3	F3	I/O
3	IO_L14P_3	G3	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IO_L18N_3	L7	I/O
3	IO_L18P_3	K6	I/O
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28N_3	M6	I/O
3	IO_L28P_3	M5	I/O
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O

Right Half of FGG676 Package (Top View)

Bank 0

	14	15	16	17	18	19	20	21	22	23	24	25	26
A	I/O L26N_0 GCLK7	I/O L23N_0	GND	INPUT	I/O L18N_0	I/O L15N_0	I/O L14N_0	GND	I/O L07N_0	INPUT	N.C.	TCK	GND
B	I/O L26P_0 GCLK6	I/O L23P_0	VCCO_0	I/O L19N_0	I/O L18P_0	I/O L15P_0	I/O L14P_0 VREF_0	I/O L09N_0	VCCO_0	I/O L07P_0	N.C.	INPUT L65N_1	INPUT L65P_1 VREF_1
C	GND	I/O L22N_0	I/O L21N_0	I/O L19P_0	I/O L17N_0	GND	I/O L11N_0	I/O L09P_0	I/O L05N_0	I/O L06N_0	GND	I/O L63N_1 A23	I/O L63P_1 A22
D	INPUT VREF_0	INPUT	I/O L22P_0	I/O L21P_0	I/O L17P_0	INPUT	I/O L11P_0	I/O L10N_0	I/O L05P_0	I/O L06P_0	I/O L61N_1	I/O L61P_1	I/O L60N_1
E	I/O L24P_0	I/O L20N_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1
F	I/O L24N_0	I/O L20P_0	GND	I/O L13P_0	N.C.	I/O L02N_0	I/O L01N_0	GND	I/O L58P_1 VREF_1	I/O L56N_1	I/O L54N_1	I/O L54P_1	GND
G	INPUT	I/O L16P_0	INPUT	I/O L08N_0	N.C.	I/O L02P_0 VREF_0	I/O L01P_0	I/O L64N_1 A25	I/O L58N_1	I/O L51P_1	I/O L51N_1	INPUT L52N_1 VREF_1	INPUT L52P_1
H	GND	I/O L16N_0	VCCO_0	I/O L08P_0	INPUT	GND	I/O L64P_1 A24	I/O L62N_1 A21	VCCO_1	INPUT L48P_1	INPUT L48N_1	INPUT L44N_1	INPUT L44P_1 VREF_1
J	I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L59P_1	I/O L59N_1	I/O L62P_1 A20	I/O L49N_1	I/O L49P_1	GND	I/O L43N_1 A19	I/O L43P_1 A18
K	I/O L25P_0 GCLK4	VCCINT	I/O L12N_0	GND	I/O L57N_1	I/O L57P_1	I/O L53N_1	I/O L50N_1	I/O L46N_1	I/O L46P_1	INPUT L40P_1	I/O L41P_1	I/O L41N_1
L	VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND
M	GND	VCCINT	GND	VCCINT	I/O L47N_1	I/O L47P_1	I/O L42N_1 A17	I/O L45P_1	I/O L45N_1	I/O L38N_1 A13	INPUT L36P_1 VREF_1	I/O L35N_1 A11	I/O L35P_1 A10
N	VCCINT	GND	VCCINT	I/O L39N_1 A15	I/O L39P_1 A14	I/O L34N_1 RHCLK7	I/O L42P_1 A16	I/O L37N_1	VCCO_1	INPUT L36N_1	I/O L33N_1 RHCLK5	INPUT L32N_1	INPUT L32P_1
P	VCCINT	VCCINT	GND	VCCAUX	I/O L34P_1 IRDY1 RHCLK6	GND	I/O L30N_1 RHCLK1	I/O L30P_1 RHCLK0	I/O L37P_1	I/O L33P_1 RHCLK4	GND	I/O L31N_1 TRDY1 RHCLK3	I/O L31P_1 RHCLK2
R	VCCINT	GND	VCCINT	I/O L27N_1 A7	I/O L27P_1 A6	I/O L22P_1	I/O L22N_1	I/O L25P_1 A2	I/O L25N_1 A3	INPUT L28P_1 VREF_1	INPUT L28N_1	I/O L29P_1 A8	I/O L29N_1 A9
T	GND	VCCINT	GND	I/O L17N_1	I/O L17P_1	VCCO_1	I/O L14N_1	GND	VCCAUX	I/O L26P_1 A4	I/O L26N_1 A5	VCCO_1	GND
U	VCCAUX	I/O L35N_2	I/O L42N_2	GND	I/O L12N_1	I/O L12P_1	I/O L10N_1	I/O L14P_1	I/O L21N_1	I/O L23P_1	I/O L23N_1 VREF_1	INPUT L24P_1	INPUT L24N_1 VREF_1
V	I/O L31P_2	I/O L35P_2	I/O L42P_2	I/O L46N_2	I/O L08P_1	I/O L08N_1	SUSPEND	I/O L10P_1	I/O L18N_1	I/O L21P_1	I/O L19P_1	I/O L19N_1	INPUT L20N_1 VREF_1
W	GND	I/O L31N_2	VCCO_2	I/O L46P_2	N.C.	GND	I/O L04P_1	I/O L04N_1	VCCO_1	I/O L18P_1	GND	INPUT L16P_1	INPUT L20P_1
Y	I/O L27P_2 GCLK0	I/O L34N_2 D3	INPUT VREF_2	I/O L43N_2	N.C.	N.C.	I/O L01P_1 HDC	I/O L01N_1 LDC2	I/O L13P_1	I/O L13N_1	I/O L15P_1	I/O L15N_1	INPUT L16N_1
AA	I/O L27N_2 GCLK1	I/O L34P_2 INIT_B	GND	I/O L43P_2	I/O L47N_2	INPUT	INPUT VREF_2	GND	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	GND
AB	VCCO_2	I/O L30N_2 MOSI CSI_B	I/O L38N_2	INPUT	I/O L47P_2	VCCO_2	INPUT	DONE	VCCAUX	I/O L07P_1	I/O L07N_1 VREF_1	VCCO_1	I/O L06N_1
AC	I/O L29N_2	I/O L30P_2	I/O L38P_2	INPUT	INPUT	I/O L40N_2	I/O L41N_2	I/O L45N_2	N.C.	I/O L03P_1 A0	I/O L03N_1 A1	I/O L05N_1	I/O L06P_1
AD	I/O L29P_2	I/O L32P_2 AWAKE	INPUT	I/O L33N_2	GND	I/O L40P_2	I/O L41P_2	I/O L44N_2	I/O L45P_2	N.C.	GND	I/O L02N_1 LDC0	I/O L05P_1
AE	I/O L28N_2 GCLK3	I/O L32N_2 DOUT	VCCO_2	I/O L33P_2	I/O L36N_2 D1	I/O L37N_2	I/O L39N_2	I/O L44P_2	VCCO_2	I/O L48N_2	I/O L52N_2 CCLK	I/O L51N_2	I/O L02P_1 LDC1
AF	I/O L28P_2 GCLK2	INPUT VREF_2	GND	INPUT VREF_2	I/O L36P_2 D2	I/O L37P_2	I/O L39P_2	GND	INPUT VREF_2	I/O L48P_2	I/O L52P_2 D0 DIN/MISO	I/O L51P_2	GND

Bank 1

Bank 2

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Figure 24: **FGG676 Package Footprint (Top View)**

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