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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 896 |
| Number of Logic Elements/Cells | 8064 |
| Total RAM Bits | 368640 |
| Number of I/O | 195 |
| Number of Gates | 400000 |
| Voltage - Supply | 1.14V ~ 1.26V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FTBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc3s400an-4ft256i |

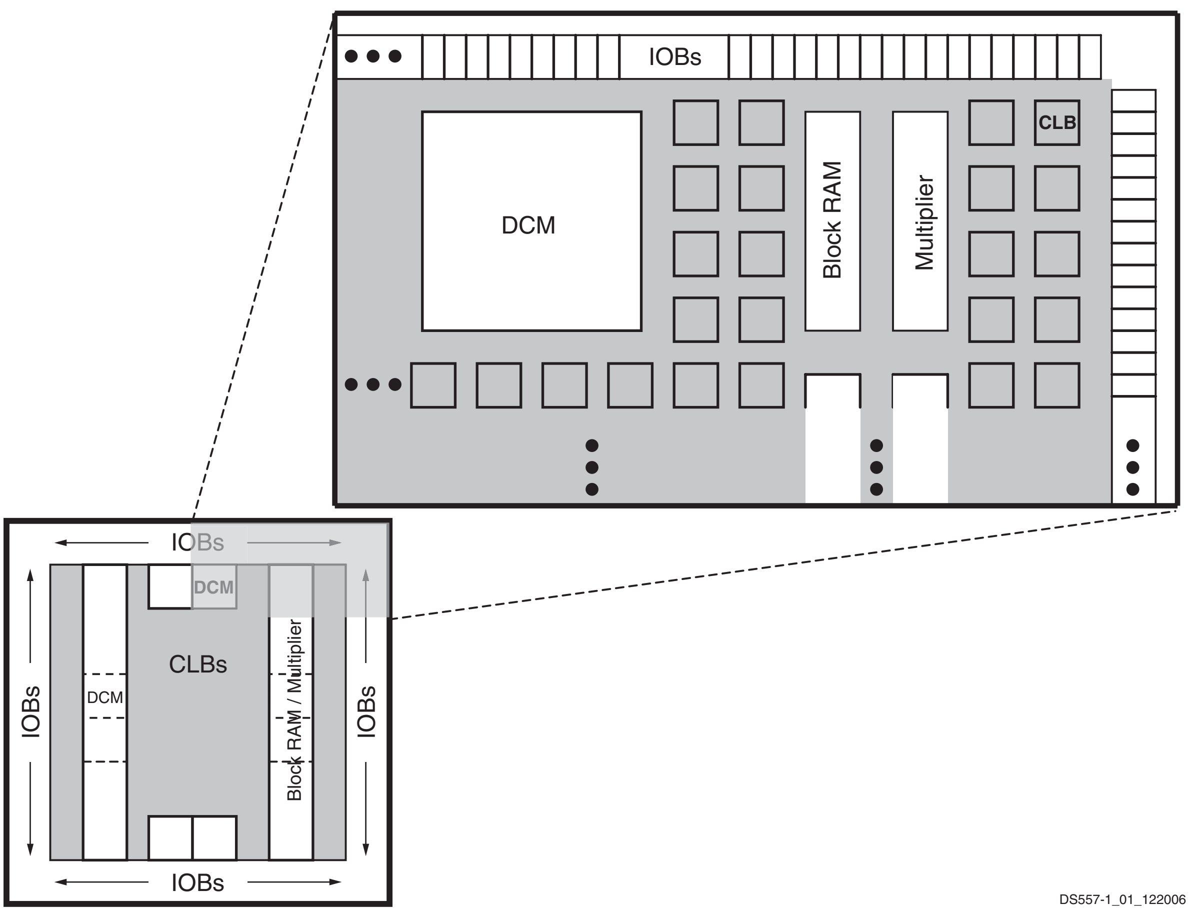
## Architectural Overview

The Spartan-3AN FPGA architecture is compatible with that of the Spartan-3A FPGA. The architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. They support a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S50AN, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S50AN has DCMs only at the top, while the XC3S700AN and XC3S1400AN add two DCMs in the middle of the two columns of block RAM and multipliers.

The Spartan-3AN FPGA features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.




**Notes:**

1. The XC3S700AN and XC3S1400AN have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S50AN has only two DCMs at the top and only one Block RAM/Multiplier column.

*Figure 1:* **Spartan-3AN Family Architecture**

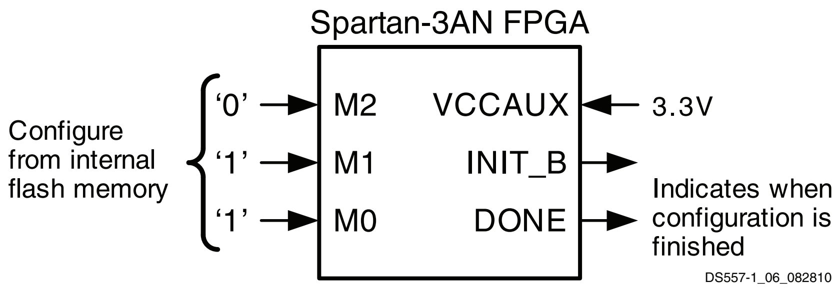



*Figure 2:* **Spartan-3AN FPGA Configuration Interface from Internal SPI Flash Memory**

## Configuration

Spartan-3AN FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored on-chip in nonvolatile Flash memory, or externally in a PROM or some other nonvolatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Configure from internal SPI Flash memory (Figure 2)
  - Completely self-contained
  - Reduced board space
  - Easy-to-use configuration interface
- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an external industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary-Scan (JTAG), typically downloaded from a processor or system tester

The MultiBoot feature stores multiple configuration files in the on-chip Flash, providing extended life with field upgrades. MultiBoot also supports multiple system solutions with a single board to minimize inventory and simplify the addition of new features, even in the field. Flexibility is maintained to do additional MultiBoot configurations via the external configuration method.

The Spartan-3AN device authentication protocol prevents cloning. Design cloning, unauthorized overbuilding, and complete reverse engineering have driven device security requirements to higher and higher levels. Authentication moves the security from bitstream protection to the next generation of design-level security protecting both the design and embedded microcode. The authentication algorithm is entirely user defined, implemented using FPGA logic. Every product, generation, or design can have a different algorithm and functionality to enhance security.

## In-System Flash Memory

Each Spartan-3AN FPGA contains abundant integrated SPI serial Flash memory, shown in Table 3, used primarily to store the FPGA's configuration bitstream. However, the Flash memory array is large enough to store at least two MultiBoot FPGA configuration bitstreams or nonvolatile data required by the FPGA application, such as code-shadowed MicroBlaze processor applications.

*Table 3:* **Spartan-3AN Device In-System Flash Memory**

| Part Number | Total Flash Memory (Bits) | FPGA Bitstream (Bits) | Additional Flash Memory (Bits)[1] |
|---|---|---|---|
| XC3S50AN | 1,081,344 | 437,312 | 642,048 |
| XC3S200AN | 4,325,376 | 1,196,128 | 3,127,872 |
| XC3S400AN | 4,325,376 | 1,886,560 | 2,437,248 |
| XC3S700AN | 8,650,752 | 2,732,640 | 5,917,824 |
| XC3S1400AN | 17,301,504 | 4,755,296 | 12,545,280 |

**Notes:**

1. Aligned to next available page location.

After configuration, the FPGA design has full access to the in-system Flash memory via an internal SPI interface; the control logic is implemented with FPGA logic. Additionally, the FPGA application itself can store nonvolatile data or provide live, in-system Flash updates.

The Spartan-3AN device in-system Flash memory supports leading-edge serial Flash features.

- Small page size (264 or 528 bytes) simplifies nonvolatile data storage
- Randomly accessible, byte addressable
- Up to 66 MHz serial data transfers
- SRAM page buffers
  - Read Flash data while programming another Flash page
  - EEPROM-like byte write functionality
  - Two buffers in most devices, one in XC3S50AN
- Page, Block, and Sector Erase

## Spartan-3AN FPGA Design Documentation

The functionality of the Spartan®-3AN FPGA family is described in the following documents. The topics covered in each guide are listed below:

- **DS706: Extended Spartan-3A Family Overview**
- **UG331: Spartan-3 Generation FPGA User Guide**
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash
    - Master SPI Mode using SPI Serial Flash PROM
    - Internal Master SPI Mode
    - Master BPI Mode using Parallel NOR Flash
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA
- **UG333: Spartan-3AN FPGA In-System Flash User Guide**
  - For FPGA applications that write to or read from the In-System Flash memory after configuration
  - SPI_ACCESS interface
  - In-System Flash memory architecture
  - Read, program, and erase commands
  - Status registers
  - Sector Protection and Sector Lockdown features
  - Security Register with Unique Identifier

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## Spartan-3AN FPGA Starter Kit

For specific hardware examples, please see the Spartan-3AN FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3AN FPGA Starter Kit Board Page**
  http://www.xilinx.com/s3anstarter
- **UG334: Spartan-3AN FPGA Starter Kit User Guide**

## General DC Characteristics for I/O Pins

*Table 11:* **General DC Characteristics of User I/O, Dual-Purpose, and Dedicated Pins**

| Symbol | Description | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $I_L$ [(2)] | Leakage current at User I/O, Input-only, Dual-Purpose, and Dedicated pins, FPGA powered | Driver is in a high-impedance state, $V_{IN}$ = 0V or $V_{CCO}$ max, sample-tested | | –10 | – | +10 | µA |
| $I_{HS}$ | Leakage current on pins during hot socketing, FPGA unpowered | All pins except INIT_B, PROG_B, DONE, and JTAG pins when PUDC_B = 1. | | –10 | – | +10 | µA |
| | | INIT_B, PROG_B, DONE, and JTAG pins or other pins when PUDC_B = 0. | | Add $I_{HS}$ + $I_{RPU}$ | | | µA |
| $I_{RPU}$ [(3)] | Current through pull-up resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins. Dedicated pins are powered by $V_{CCAUX}$. [(4)] | $V_{IN}$ = GND | $V_{CCO}$ or $V_{CCAUX}$ = 3.0V to 3.6V | –151 | –315 | –710 | µA |
| | | | $V_{CCO}$ = 2.3V to 2.7V | –82 | –182 | –437 | µA |
| | | | $V_{CCO}$ = 1.7V to 1.9V | –36 | –88 | –226 | µA |
| | | | $V_{CCO}$ = 1.4V to 1.6V | –22 | –56 | –148 | µA |
| | | | $V_{CCO}$ = 1.14V to 1.26V | –11 | –31 | –83 | µA |
| $R_{PU}$ [(3)] | Equivalent pull-up resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on $I_{RPU}$ per Note 3) | $V_{IN}$ = GND | $V_{CCO}$ = 3.0V to 3.6V | 5.1 | 11.4 | 23.9 | kΩ |
| | | | $V_{CCO}$ = 2.3V to 2.7V | 6.2 | 14.8 | 33.1 | kΩ |
| | | | $V_{CCO}$ = 1.7V to 1.9V | 8.4 | 21.6 | 52.6 | kΩ |
| | | | $V_{CCO}$ = 1.4V to 1.6V | 10.8 | 28.4 | 74.0 | kΩ |
| | | | $V_{CCO}$ = 1.14V to 1.26V | 15.3 | 41.1 | 119.4 | kΩ |
| $I_{RPD}$ [(3)] | Current through pull-down resistor at User I/O, Dual-Purpose, Input-only, and Dedicated pins | $V_{IN}$ = $V_{CCO}$ | $V_{CCAUX}$ = 3.0V to 3.6V | 167 | 346 | 659 | µA |
| $R_{PD}$ [(3)] | Equivalent pull-down resistor value at User I/O, Dual-Purpose, Input-only, and Dedicated pins (based on $I_{RPD}$ per Note 3) | $V_{CCAUX}$ = 3.0V to 3.6V | $V_{IN}$ = 3.0V to 3.6V | 5.5 | 10.4 | 20.8 | kΩ |
| | | | $V_{IN}$ = 2.3V to 2.7V | 4.1 | 7.8 | 15.7 | kΩ |
| | | | $V_{IN}$ = 1.7V to 1.9V | 3.0 | 5.7 | 11.1 | kΩ |
| | | | $V_{IN}$ = 1.4V to 1.6V | 2.7 | 5.1 | 9.6 | kΩ |
| | | | $V_{IN}$ = 1.14V to 1.26V | 2.4 | 4.5 | 8.1 | kΩ |
| $I_{REF}$ | $V_{REF}$ current per pin | All $V_{CCO}$ levels | | –10 | – | +10 | µA |
| $C_{IN}$ | Input capacitance | – | | – | – | 10 | pF |
| $R_{DT}$ | Resistance of optional differential termination circuit within a differential I/O pair. Not available on Input-only pairs. | $V_{CCO}$ = 3.3V ± 10% | LVDS_33, MINI_LVDS_33, RSDS_33 | 90 | 100 | 115 | Ω |
| | | $V_{CCO}$ = 2.5V ± 10% | LVDS_25, MINI_LVDS_25, RSDS_25 | 90 | 110 | – | Ω |

**Notes:**

1. The numbers in this table are based on the conditions set forth in Table 10.
2. For single-ended signals that are placed on a differential-capable I/O, $V_{IN}$ of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
3. This parameter is based on characterization. The pull-up resistance $R_{PU} = V_{CCO} / I_{RPU}$. The pull-down resistance $R_{PD} = V_{IN} / I_{RPD}$.
4. $V_{CCAUX}$ must be 3.3V on Spartan-3AN FPGAs. $V_{CCAUX}$ for Spartan-3A FPGAs can be either 3.3V or 2.5V.

## Quiescent Current Requirements

*Table 12:* **Spartan-3AN FPGA Quiescent Supply Current Characteristics**

| Symbol | Description | Device | Typical(2) | Commercial Maximum(2) | Industrial Maximum(2) | Units |
|---|---|---|---|---|---|---|
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC3S50AN | 2 | 20 | 30 | mA |
| | | XC3S200AN | 7 | 50 | 70 | mA |
| | | XC3S400AN | 10 | 85 | 125 | mA |
| | | XC3S700AN | 13 | 120 | 185 | mA |
| | | XC3S1400AN | 24 | 220 | 310 | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC3S50AN | 0.2 | 2 | 3 | mA |
| | | XC3S200AN | 0.2 | 2 | 3 | mA |
| | | XC3S400AN | 0.3 | 3 | 4 | mA |
| | | XC3S700AN | 0.3 | 3 | 4 | mA |
| | | XC3S1400AN | 0.3 | 3 | 4 | mA |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC3S50AN | 3.1 | 8.1 | 10.1 | mA |
| | | XC3S200AN | 5.1 | 12.1 | 15.1 | mA |
| | | XC3S400AN | 5.1 | 18.1 | 24.1 | mA |
| | | XC3S700AN | 6.1 | 28.1 | 34.1 | mA |
| | | XC3S1400AN | 10.1 | 50.1 | 58.1 | mA |

**Notes:**

1. The numbers in this table are based on the conditions set forth in Table 10.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. The internal SPI Flash is deselected (CSB = High); the internal SPI Flash current is consumed on the $V_{CCAUX}$ supply rail. Typical values are characterized using typical devices at room temperature ($T_J$ of 25°C at $V_{CCINT}$ = 1.2V, $V_{CCO}$ = 3.3V, and $V_{CCAUX}$ = 3.3V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with $V_{CCINT}$ = 1.26V, $V_{CCO}$ = 3.6V, and $V_{CCAUX}$ = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3AN FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design, and b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates. For more information on power for the In-System Flash memory, see the Power Management chapter of UG333.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

# Differential I/O Standards

## Differential Input Pairs

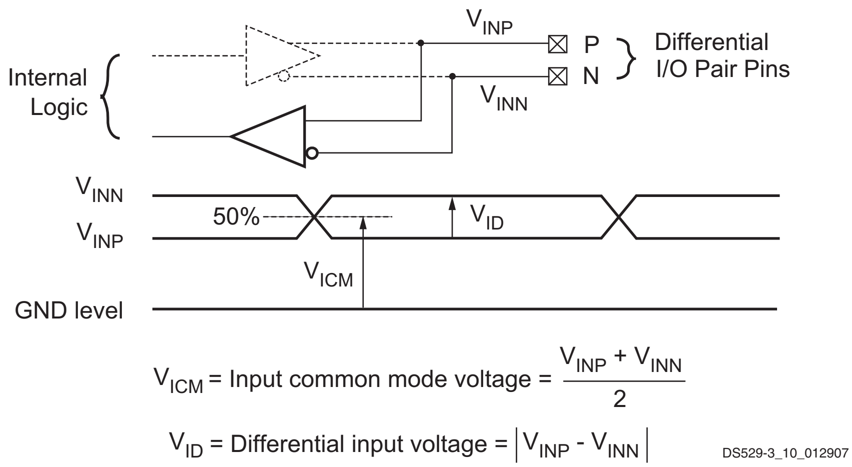



*Figure 6:* **Differential Input Voltages**

*Table 15:* **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

| IOSTANDARD Attribute | $V_{CCO}$ for Drivers(1) | | | $V_{ID}$ | | | $V_{ICM}$(2) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min (V) | Nom (V) | Max (V) | Min (mV) | Nom (mV) | Max (mV) | Min (V) | Nom (V) | Max (V) |
| LVDS_25(3) | 2.25 | 2.5 | 2.75 | 100 | 350 | 600 | 0.3 | 1.25 | 2.35 |
| LVDS_33(3) | 3.0 | 3.3 | 3.6 | 100 | 350 | 600 | 0.3 | 1.25 | 2.35 |
| BLVDS_25(4) | 2.25 | 2.5 | 2.75 | 100 | 300 | – | 0.3 | 1.3 | 2.35 |
| MINI_LVDS_25(3) | 2.25 | 2.5 | 2.75 | 200 | – | 600 | 0.3 | 1.2 | 1.95 |
| MINI_LVDS_33(3) | 3.0 | 3.3 | 3.6 | 200 | – | 600 | 0.3 | 1.2 | 1.95 |
| LVPECL_25(5) | Inputs Only | | | 100 | 800 | 1000 | 0.3 | 1.2 | 1.95 |
| LVPECL_33(5) | Inputs Only | | | 100 | 800 | 1000 | 0.3 | 1.2 | 2.8(6) |
| RSDS_25(3) | 2.25 | 2.5 | 2.75 | 100 | 200 | – | 0.3 | 1.2 | 1.5 |
| RSDS_33(3) | 3.0 | 3.3 | 3.6 | 100 | 200 | – | 0.3 | 1.2 | 1.5 |
| TMDS_33(3,4,7) | 3.14 | 3.3 | 3.47 | 150 | – | 1200 | 2.7 | – | 3.23 |
| PPDS_25(3) | 2.25 | 2.5 | 2.75 | 100 | – | 400 | 0.2 | – | 2.3 |
| PPDS_33(3) | 3.0 | 3.3 | 3.6 | 100 | – | 400 | 0.2 | – | 2.3 |
| DIFF_HSTL_I_18(8) | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.8 | – | 1.1 |
| DIFF_HSTL_II_18(8,9) | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.8 | – | 1.1 |
| DIFF_HSTL_III_18(8) | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.8 | – | 1.1 |
| DIFF_HSTL_I(8) | 1.4 | 1.5 | 1.6 | 100 | – | – | 0.68 | | 0.9 |
| DIFF_HSTL_III(8) | 1.4 | 1.5 | 1.6 | 100 | – | – | – | 0.9 | – |
| DIFF_SSTL18_I(8) | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.7 | – | 1.1 |
| DIFF_SSTL18_II(8,9) | 1.7 | 1.8 | 1.9 | 100 | – | – | 0.7 | – | 1.1 |
| DIFF_SSTL2_I(8) | 2.3 | 2.5 | 2.7 | 100 | – | – | 1.0 | – | 1.5 |
| DIFF_SSTL2_II(8,9) | 2.3 | 2.5 | 2.7 | 100 | – | – | 1.0 | – | 1.5 |
| DIFF_SSTL3_I(8) | 3.0 | 3.3 | 3.6 | 100 | – | – | 1.1 | – | 1.9 |

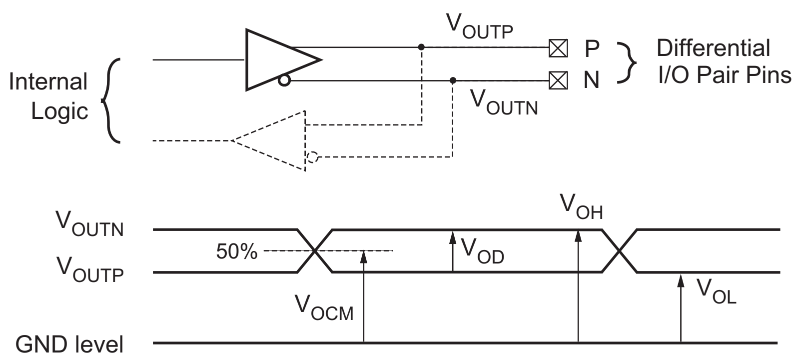
*Table 15:* **Recommended Operating Conditions for User I/Os Using Differential Signal Standards *(Cont'd)***

| IOSTANDARD Attribute | $V_{CCO}$ for Drivers[(1)] | | | $V_{ID}$ | | | $V_{ICM}$[(2)] | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min (V) | Nom (V) | Max (V) | Min (mV) | Nom (mV) | Max (mV) | Min (V) | Nom (V) | Max (V) |
| DIFF_SSTL3_II[(8)] | 3.0 | 3.3 | 3.6 | 100 | – | – | 1.1 | – | 1.9 |

**Notes:**

1. The $V_{CCO}$ rails supply only differential output drivers, not input circuits.
2. $V_{ICM}$ must be less than $V_{CCAUX}$.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the "Using I/O Resources" chapter in UG331.
4. See External Termination Requirements for Differential I/O, page 22.
5. LVPECL is supported on inputs only, not outputs. Requires $V_{CCAUX} = 3.3V \pm 10\%$.
6. LVPECL_33 maximum $V_{ICM} = V_{CCAUX} – (V_{ID} / 2)$
7. Requires $V_{CCAUX} = 3.3V \pm 10\%$ for inputs. $(V_{CCAUX} – 300 \text{ mV}) \leq V_{ICM} \leq (V_{CCAUX} – 37 \text{ mV})$
8. $V_{REF}$ inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The $V_{REF}$ settings are the same as for the single-ended versions in Table 13. Other differential standards do not use $V_{REF}$.
9. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the "Using I/O Resources" chapter in UG331.

## Differential Output Pairs




$$V_{OCM} = \text{Output common mode voltage} = \frac{V_{OUTP} + V_{OUTN}}{2}$$

$$V_{OD} = \text{Output differential voltage} = \left| V_{OUTP} - V_{OUTN} \right|$$

$$V_{OH} = \text{Output voltage indicating a High logic level}$$

$$V_{OL} = \text{Output voltage indicating a Low logic level}$$

DS529-3_11_082810

*Figure 7:* **Differential Output Voltages**

## Output Propagation Times

*Table 27:* **Timing for the IOB Output Path**

| Symbol | Description | Conditions | Device | Speed Grade | | Units |
|---|---|---|---|---|---|---|
| | | | | -5 | -4 | |
| | | | | Max | Max | |
| **Clock-to-Output Times** | | | | | | |
| $T_{IOCKP}$ | When reading from the Output Flip-Flop (OFF), the time from the active transition at the OCLK input to data appearing at the Output pin | LVCMOS25(2), 12 mA output drive, Fast slew rate | All | 2.87 | 3.13 | ns |
| **Propagation Times** | | | | | | |
| $T_{IOOP}$ | The time it takes for data to travel from the IOB's O input to the Output pin | LVCMOS25(2), 12 mA output drive, Fast slew rate | All | 2.78 | 2.91 | ns |
| **Set/Reset Times** | | | | | | |
| $T_{IOSRP}$ | Time from asserting the OFF's SR input to setting/resetting data at the Output pin | LVCMOS25(2), 12 mA output drive, Fast slew rate | All | 3.63 | 3.89 | ns |
| $T_{IOGSRQ}$ | Time from asserting the Global Set Reset (GSR) input on the STARTUP_SPARTAN3A primitive to setting/resetting data at the Output pin | | | 8.62 | 9.65 | ns |

**Notes:**

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 29.

*Table 30:* **Test Methods for Timing Measurement at I/Os *(Cont'd)***

| Signal Standard (IOSTANDARD) | Inputs | | | Outputs[2] | | Inputs and Outputs |
|---|---|---|---|---|---|---|
| | $V_{REF}$ (V) | $V_L$ (V) | $V_H$ (V) | $R_T$ (Ω) | $V_T$ (V) | $V_M$ (V) |
| **Differential** | | | | | | |
| LVDS_25 | – | $V_{ICM}$ – 0.125 | $V_{ICM}$ + 0.125 | 50 | 1.2 | $V_{ICM}$ |
| LVDS_33 | – | $V_{ICM}$ – 0.125 | $V_{ICM}$ + 0.125 | 50 | 1.2 | $V_{ICM}$ |
| BLVDS_25 | – | $V_{ICM}$ – 0.125 | $V_{ICM}$ + 0.125 | 1M | 0 | $V_{ICM}$ |
| MINI_LVDS_25 | – | $V_{ICM}$ – 0.125 | $V_{ICM}$ + 0.125 | 50 | 1.2 | $V_{ICM}$ |
| MINI_LVDS_33 | – | $V_{ICM}$ – 0.125 | $V_{ICM}$ + 0.125 | 50 | 1.2 | $V_{ICM}$ |
| LVPECL_25 | – | $V_{ICM}$ – 0.3 | $V_{ICM}$ + 0.3 | N/A | N/A | $V_{ICM}$ |
| LVPECL_33 | – | $V_{ICM}$ – 0.3 | $V_{ICM}$ + 0.3 | N/A | N/A | $V_{ICM}$ |
| RSDS_25 | – | $V_{ICM}$ – 0.1 | $V_{ICM}$ + 0.1 | 50 | 1.2 | $V_{ICM}$ |
| RSDS_33 | – | $V_{ICM}$ – 0.1 | $V_{ICM}$ + 0.1 | 50 | 1.2 | $V_{ICM}$ |
| TMDS_33 | – | $V_{ICM}$ – 0.1 | $V_{ICM}$ + 0.1 | 50 | 3.3 | $V_{ICM}$ |
| PPDS_25 | – | $V_{ICM}$ – 0.1 | $V_{ICM}$ + 0.1 | 50 | 0.8 | $V_{ICM}$ |
| PPDS_33 | – | $V_{ICM}$ – 0.1 | $V_{ICM}$ + 0.1 | 50 | 0.8 | $V_{ICM}$ |
| DIFF_HSTL_I | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 0.75 | $V_{ICM}$ |
| DIFF_HSTL_III | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 1.5 | $V_{ICM}$ |
| DIFF_HSTL_I_18 | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 0.9 | $V_{ICM}$ |
| DIFF_HSTL_II_18 | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 0.9 | $V_{ICM}$ |
| DIFF_HSTL_III_18 | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 1.8 | $V_{ICM}$ |
| DIFF_SSTL18_I | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 0.9 | $V_{ICM}$ |
| DIFF_SSTL18_II | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 0.9 | $V_{ICM}$ |
| DIFF_SSTL2_I | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 1.25 | $V_{ICM}$ |
| DIFF_SSTL2_II | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 1.25 | $V_{ICM}$ |
| DIFF_SSTL3_I | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 1.5 | $V_{ICM}$ |
| DIFF_SSTL3_II | – | $V_{ICM}$ – 0.5 | $V_{ICM}$ + 0.5 | 50 | 1.5 | $V_{ICM}$ |

**Notes:**

1. Descriptions of the relevant symbols are as follows:
   $V_{REF}$ – The reference voltage for setting the input switching threshold
   $V_{ICM}$ – The common mode input voltage
   $V_M$ – Voltage of measurement point on signal transition
   $V_L$ – Low-level test voltage at Input pin
   $V_H$ – High-level test voltage at Input pin
   $R_T$ – Effective termination resistance, which takes on a value of 1 MΩ when no parallel termination is required
   $V_T$ – Termination voltage
2. The load capacitance ($C_L$) at the Output pin is 0 pF for all signal standards.
3. According to the PCI specification. For information on PCI IP solutions, see www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.

The capacitive load ($C_L$) is connected between the output and GND. *The Output timing for all standards, as published in the speed files and the data sheet, is always based on a $C_L$ value of zero.* High-impedance probes (less than 1 pF) are used for all measurements. Any delay that the test fixture might contribute to test measurements is subtracted from those measurements to produce the final timing numbers as published in the speed files and data sheet.

*Table 40:* **Switching Characteristics for the DLL *(Cont'd)***

| Symbol | Description | Device | Speed Grade -5 Min | Speed Grade -5 Max | Speed Grade -4 Min | Speed Grade -4 Max | Units |
|---|---|---|---|---|---|---|---|
| **Delay Lines** | | | | | | | |
| DCM_DELAY_STEP(5) | Finest delay resolution, average over all taps | All | 15 | 35 | 15 | 35 | ps |

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 10 and Table 39.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps.
5. The typical delay step size is 23 ps.

## Digital Frequency Synthesizer (DFS)

*Table 41:* **Recommended Operating Conditions for the DFS**

| Symbol | | Description | | Speed Grade -5 Min | Speed Grade -5 Max | Speed Grade -4 Min | Speed Grade -4 Max | Units |
|---|---|---|---|---|---|---|---|---|
| **Input Frequency Ranges(2)** | | | | | | | | |
| $F_{CLKIN}$ | CLKIN_FREQ_FX | Frequency for the CLKIN input | | 0.200 | 333(3) | 0.200 | 333(3) | MHz |
| **Input Clock Jitter Tolerance(4)** | | | | | | | | |
| CLKIN_CYC_JITT_FX_LF | | Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency | $F_{CLKFX} \leq 150$ MHz | – | ±300 | – | ±300 | ps |
| CLKIN_CYC_JITT_FX_HF | | | $F_{CLKFX} > 150$ MHz | – | ±150 | – | ±150 | ps |
| CLKIN_PER_JITT_FX | | Period jitter at the CLKIN input | | – | ±1 | – | ±1 | ns |

**Notes:**

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 39.
3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.
4. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

## Suspend Mode Timing

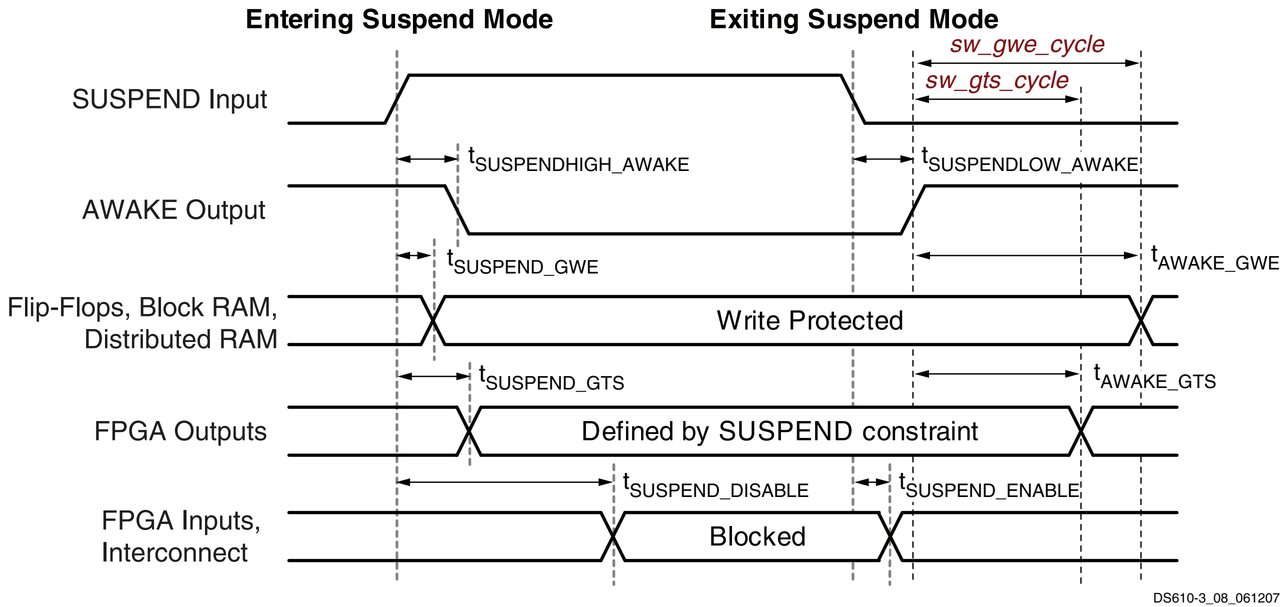



*Figure 12:* **Suspend Mode Timing**

*Table 49:* **Suspend Mode Timing Parameters**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **Entering Suspend Mode** | | | | | |
| $T_{SUSPENDHIGH\_AWAKE}$ | Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***) | – | 7 | – | ns |
| $T_{SUSPENDFILTER}$ | Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***) | +160 | +300 | +600 | ns |
| $T_{SUSPEND\_GTS}$ | Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior | – | 10 | – | ns |
| $T_{SUSPEND\_GWE}$ | Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements | – | < 5 | – | ns |
| $T_{SUSPEND\_DISABLE}$ | Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled | – | 340 | – | ns |
| **Exiting Suspend Mode** | | | | | |
| $T_{SUSPENDLOW\_AWAKE}$ | Falling edge of the SUSPEND pin to rising edge of the AWAKE pin Does not include DCM lock time | – | 4 to 108 | – | μs |
| $T_{SUSPEND\_ENABLE}$ | Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled | – | 3.7 to 109 | – | μs |
| $T_{AWAKE\_GWE1}$ | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1*** | – | 67 | – | ns |
| $T_{AWAKE\_GWE512}$ | Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512*** | – | 14 | – | μs |
| $T_{AWAKE\_GTS1}$ | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1*** | – | 57 | – | ns |
| $T_{AWAKE\_GTS512}$ | Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512*** | – | 14 | – | μs |

**Notes:**

1. These parameters based on characterization.
2. For information on using the Spartan-3AN Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

*Table 52:* **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

| Symbol | Description | *ConfigRate* Setting | Temperature Range | Minimum | Maximum | Units |
|---|---|---|---|---|---|---|
| $F_{CCLK1}$ | Equivalent CCLK clock frequency by ***ConfigRate*** setting | 1 *(power-on value)* | Commercial | 0.400 | 0.797 | MHz |
| | | | Industrial | | 0.847 | MHz |
| $F_{CCLK3}$ | | 3 | Commercial | 1.20 | 2.42 | MHz |
| | | | Industrial | | 2.57 | MHz |
| $F_{CCLK6}$ | | 6 (*default*) | Commercial | 2.40 | 4.83 | MHz |
| | | | Industrial | | 5.13 | MHz |
| $F_{CCLK7}$ | | 7 | Commercial | 2.80 | 5.61 | MHz |
| | | | Industrial | | 5.96 | MHz |
| $F_{CCLK8}$ | | 8 | Commercial | 3.20 | 6.41 | MHz |
| | | | Industrial | | 6.81 | MHz |
| $F_{CCLK10}$ | | 10 | Commercial | 4.00 | 8.12 | MHz |
| | | | Industrial | | 8.63 | MHz |
| $F_{CCLK12}$ | | 12 | Commercial | 4.80 | 9.70 | MHz |
| | | | Industrial | | 10.31 | MHz |
| $F_{CCLK13}$ | | 13 | Commercial | 5.20 | 10.69 | MHz |
| | | | Industrial | | 11.37 | MHz |
| $F_{CCLK17}$ | | 17 | Commercial | 6.80 | 13.74 | MHz |
| | | | Industrial | | 14.61 | MHz |
| $F_{CCLK22}$ | | 22 | Commercial | 8.80 | 18.44 | MHz |
| | | | Industrial | | 19.61 | MHz |
| $F_{CCLK25}$ | | 25 | Commercial | 10.00 | 20.90 | MHz |
| | | | Industrial | | 22.23 | MHz |
| $F_{CCLK27}$ | | 27 | Commercial | 10.80 | 22.39 | MHz |
| | | | Industrial | | 23.81 | MHz |
| $F_{CCLK33}$ | | 33 | Commercial | 13.20 | 27.48 | MHz |
| | | | Industrial | | 29.23 | MHz |
| $F_{CCLK44}$ | | 44 | Commercial | 17.60 | 37.60 | MHz |
| | | | Industrial | | 40.00 | MHz |
| $F_{CCLK50}$ | | 50 | Commercial | 20.00 | 44.80 | MHz |
| | | | Industrial | | 47.66 | MHz |
| $F_{CCLK100}$ | | 100 | Commercial | 40.00 | 88.68 | MHz |
| | | | Industrial | | 94.34 | MHz |

*Table 53:* **Master Mode CCLK Output Minimum Low and High Time**

| Symbol | Description | | *ConfigRate* Setting | | | | | | | | | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1 | 3 | 6 | 7 | 8 | 10 | 12 | 13 | 17 | 22 | 25 | 27 | 33 | 44 | 50 | 100 | |
| $T_{MCCL}$, $T_{MCCH}$ | Master Mode CCLK Minimum Low and High Time | Commercial | 595 | 196 | 98.3 | 84.5 | 74.1 | 58.4 | 48.9 | 44.1 | 34.2 | 25.6 | 22.3 | 20.9 | 17.1 | 12.3 | 10.4 | 5.3 | ns |
| | | Industrial | 560 | 185 | 92.6 | 79.8 | 69.8 | 55.0 | 46.0 | 41.8 | 32.3 | 24.2 | 21.4 | 20.0 | 16.2 | 11.9 | 10.0 | 5.0 | ns |

*Table 59:* **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

| Symbol | Description | Minimum | Maximum | Units |
|---|---|---|---|---|
| $T_{CCLK1}$ | Initial CCLK clock period | See Table 51 | | |
| $T_{CCLKn}$ | CCLK clock period after FPGA loads ConfigRate setting | See Table 51 | | |
| $T_{MINIT}$ | Setup time on M[2:0] mode pins before the rising edge of INIT_B | 50 | – | ns |
| $T_{INITM}$ | Hold time on M[2:0] mode pins after the rising edge of INIT_B | 0 | – | ns |
| $T_{INITADDR}$ | Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid | 5 | 5 | $T_{CCLK1}$ cycles |
| $T_{CCO}$ | Address A[25:0] outputs valid after CCLK falling edge | See Table 55 | | |
| $T_{DCC}$ | Setup time on D[7:0] data inputs before CCLK rising edge | See $T_{SMDCC}$ in Table 56 | | |
| $T_{CCD}$ | Hold time on D[7:0] data inputs after CCLK rising edge | 0 | – | ns |

*Table 60:* **Configuration Timing Requirements for Attached Parallel NOR Flash**

| Symbol | Description | Requirement | Units |
|---|---|---|---|
| $T_{CE}$ ($t_{ELQV}$) | Parallel NOR Flash PROM chip-select time | $T_{CE} \leq T_{INITADDR}$ | ns |
| $T_{OE}$ ($t_{GLQV}$) | Parallel NOR Flash PROM output-enable time | $T_{OE} \leq T_{INITADDR}$ | ns |
| $T_{ACC}$ ($t_{AVQV}$) | Parallel NOR Flash PROM read access time | $T_{ACC} \leq 0.5 T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$ | ns |
| $T_{BYTE}$ ($t_{FLQV}$, $t_{FHQV}$) | For x8/x16 PROMs only: BYTE# to output valid time[3] | $T_{BYTE} \leq T_{INITADDR}$ | ns |

**Notes:**

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

## IEEE 1149.1/1532 JTAG Test Access Port Timing

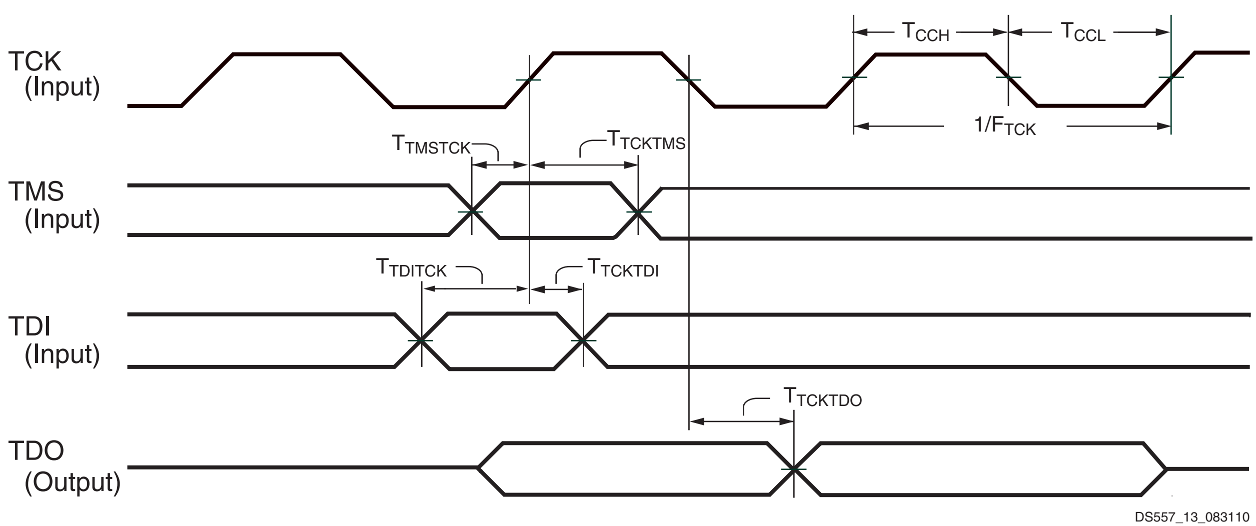



*Figure 18:* **JTAG Waveforms**

## FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FTG256, supports the XC3S50AN, XC3S200AN, and XC3S400AN devices. Table 70 lists all the package pins for these devices. They are sorted by bank number and then by the pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The differential I/O pairs that have different assignments between the XC3S50AN and the XC3S200AN or XC3S400AN are highlighted in light blue in Table 70. See Footprint Migration Differences, page 87 for additional information. The table also shows the pin number for each pin and the pin type (as defined in Table 62).

The footprints for the XC3S200AN and XC3S400AN in the FTG256 are identical. Figure 21 shows the common footprint for the XC3S200AN and XC3S400AN. The XC3S50AN footprint is compatible with the XC3S200AN and XC3S400AN, however, there are 51 unconnected balls (indicated as N.C. in Table 70).

Table 73 summarizes the XC3S50AN FPGA footprint migration differences for the FTG256 package.

The XC3S50AN does not support the address output pins for the byte-wide peripheral interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

### Pinout Table

*Table 70:* **Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN)**

| Bank | XC3S50AN Pin Name | XC3S200AN/XC3S400AN Pin Name | FTG256 Ball | Type |
|---|---|---|---|---|
| 0 | IO_L01N_0 | IO_L01N_0 | C13 | I/O |
| 0 | IO_L01P_0 | IO_L01P_0 | D13 | I/O |
| 0 | IO_L02N_0 | IO_L02N_0 | B14 | I/O |
| 0 | IO_L02P_0/VREF_0 | IO_L02P_0/VREF_0 | B15 | VREF |
| 0 | IO_L03N_0 | IO_L03N_0 | D11 | I/O |
| 0 | IO_L03P_0 | IO_L03P_0 | C12 | I/O |
| 0 | IO_L04N_0 | IO_L04N_0 | A13 | I/O |
| 0 | IO_L04P_0 | IO_L04P_0 | A14 | I/O |
| 0 | N.C. | IO_L05N_0 | A12 | I/O |
| 0 | IP_0 | IO_L05P_0 | B12 | I/O |
| 0 | N.C. | IO_L06N_0/VREF_0 | E10 | VREF |
| 0 | N.C. | IO_L06P_0 | D10 | I/O |
| 0 | IO_L07N_0 | IO_L07N_0 | A11 | I/O |
| 0 | IO_L07P_0 | IO_L07P_0 | C11 | I/O |
| 0 | IO_L08N_0 | IO_L08N_0 | A10 | I/O |
| 0 | IO_L08P_0 | IO_L08P_0 | B10 | I/O |
| 0 | IO_L09N_0/GCLK5 | IO_L09N_0/GCLK5 | D9 | GCLK |
| 0 | IO_L09P_0/GCLK4 | IO_L09P_0/GCLK4 | C10 | GCLK |
| 0 | IO_L10N_0/GCLK7 | IO_L10N_0/GCLK7 | A9 | GCLK |
| 0 | IO_L10P_0/GCLK6 | IO_L10P_0/GCLK6 | C9 | GCLK |
| 0 | IO_L11N_0/GCLK9 | IO_L11N_0/GCLK9 | D8 | GCLK |
| 0 | IO_L11P_0/GCLK8 | IO_L11P_0/GCLK8 | C8 | GCLK |
| 0 | IO_L12N_0/GCLK11 | IO_L12N_0/GCLK11 | B8 | GCLK |
| 0 | IO_L12P_0/GCLK10 | IO_L12P_0/GCLK10 | A8 | GCLK |
| 0 | N.C. | IO_L13N_0 | C7 | I/O |
| 0 | N.C. | IO_L13P_0 | A7 | I/O |

*Table 70:* **Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN)** ***(Cont'd)***

| Bank | XC3S50AN Pin Name | XC3S200AN/XC3S400AN Pin Name | FTG256 Ball | Type |
|---|---|---|---|---|
| GND | GND | GND | J8 | GND |
| GND | GND | GND | K2 | GND |
| GND | GND | GND | K7 | GND |
| GND | GND | GND | K9 | GND |
| GND | GND | GND | L11 | GND |
| GND | GND | GND | L15 | GND |
| GND | GND | GND | M5 | GND |
| GND | GND | GND | M12 | GND |
| GND | GND | GND | P3 | GND |
| GND | GND | GND | P14 | GND |
| GND | GND | GND | R6 | GND |
| GND | GND | GND | R10 | GND |
| GND | GND | GND | T1 | GND |
| GND | GND | GND | T16 | GND |
| VCCAUX | SUSPEND | SUSPEND | R16 | PWR MGMT |
| VCCAUX | DONE | DONE | T15 | CONFIG |
| VCCAUX | PROG_B | PROG_B | A2 | CONFIG |
| VCCAUX | TCK | TCK | A15 | JTAG |
| VCCAUX | TDI | TDI | B1 | JTAG |
| VCCAUX | TDO | TDO | B16 | JTAG |
| VCCAUX | TMS | TMS | B2 | JTAG |
| VCCAUX | VCCAUX | VCCAUX | E11 | VCCAUX |
| VCCAUX | VCCAUX | VCCAUX | F5 | VCCAUX |
| VCCAUX | VCCAUX | VCCAUX | L12 | VCCAUX |
| VCCAUX | VCCAUX | VCCAUX | M6 | VCCAUX |
| VCCINT | VCCINT | VCCINT | G7 | VCCINT |
| VCCINT | VCCINT | VCCINT | G9 | VCCINT |
| VCCINT | VCCINT | VCCINT | H8 | VCCINT |
| VCCINT | VCCINT | VCCINT | J9 | VCCINT |
| VCCINT | VCCINT | VCCINT | K8 | VCCINT |
| VCCINT | VCCINT | VCCINT | K10 | VCCINT |

*Table 76:* **Spartan-3AN FGG400 Pinout *(Cont'd)***

| Bank | Pin Name | FGG400 Ball | Type |
|---|---|---|---|
| 0 | IO_L32N_0/PUDC_B | B2 | DUAL |
| 0 | IO_L32P_0/VREF_0 | A2 | VREF |
| 0 | IP_0 | E14 | INPUT |
| 0 | IP_0 | F11 | INPUT |
| 0 | IP_0 | F14 | INPUT |
| 0 | IP_0 | G8 | INPUT |
| 0 | IP_0 | G9 | INPUT |
| 0 | IP_0 | G10 | INPUT |
| 0 | IP_0 | G12 | INPUT |
| 0 | IP_0 | G13 | INPUT |
| 0 | IP_0 | H9 | INPUT |
| 0 | IP_0 | H10 | INPUT |
| 0 | IP_0 | H11 | INPUT |
| 0 | IP_0 | H12 | INPUT |
| 0 | IP_0/VREF_0 | G11 | VREF |
| 0 | VCCO_0 | B4 | VCCO |
| 0 | VCCO_0 | B10 | VCCO |
| 0 | VCCO_0 | B16 | VCCO |
| 0 | VCCO_0 | D7 | VCCO |
| 0 | VCCO_0 | D13 | VCCO |
| 0 | VCCO_0 | F10 | VCCO |
| 1 | IO_L01N_1/LDC2 | V20 | DUAL |
| 1 | IO_L01P_1/HDC | W20 | DUAL |
| 1 | IO_L02N_1/LDC0 | U18 | DUAL |
| 1 | IO_L02P_1/LDC1 | V19 | DUAL |
| 1 | IO_L03N_1/A1 | R16 | DUAL |
| 1 | IO_L03P_1/A0 | T17 | DUAL |
| 1 | IO_L05N_1 | T20 | I/O |
| 1 | IO_L05P_1 | T18 | I/O |
| 1 | IO_L06N_1 | U20 | I/O |
| 1 | IO_L06P_1 | U19 | I/O |
| 1 | IO_L07N_1 | P17 | I/O |
| 1 | IO_L07P_1 | P16 | I/O |
| 1 | IO_L08N_1 | R17 | I/O |
| 1 | IO_L08P_1 | R18 | I/O |
| 1 | IO_L09N_1 | R20 | I/O |
| 1 | IO_L09P_1 | R19 | I/O |
| 1 | IO_L10N_1/VREF_1 | P20 | VREF |
| 1 | IO_L10P_1 | P18 | I/O |
| 1 | IO_L12N_1/A3 | N17 | DUAL |

*Table 76:* **Spartan-3AN FGG400 Pinout *(Cont'd)***

| Bank | Pin Name | FGG400 Ball | Type |
|---|---|---|---|
| 1 | IO_L12P_1/A2 | N15 | DUAL |
| 1 | IO_L13N_1/A5 | N19 | DUAL |
| 1 | IO_L13P_1/A4 | N18 | DUAL |
| 1 | IO_L14N_1/A7 | M18 | DUAL |
| 1 | IO_L14P_1/A6 | M17 | DUAL |
| 1 | IO_L16N_1/A9 | L16 | DUAL |
| 1 | IO_L16P_1/A8 | L15 | DUAL |
| 1 | IO_L17N_1/RHCLK1 | M20 | RHCLK |
| 1 | IO_L17P_1/RHCLK0 | M19 | RHCLK |
| 1 | IO_L18N_1/TRDY1/RHCLK3 | L18 | RHCLK |
| 1 | IO_L18P_1/RHCLK2 | L19 | RHCLK |
| 1 | IO_L20N_1/RHCLK5 | L17 | RHCLK |
| 1 | IO_L20P_1/RHCLK4 | K18 | RHCLK |
| 1 | IO_L21N_1/RHCLK7 | J20 | RHCLK |
| 1 | IO_L21P_1/IRDY1/RHCLK6 | K20 | RHCLK |
| 1 | IO_L22N_1/A11 | J18 | DUAL |
| 1 | IO_L22P_1/A10 | J19 | DUAL |
| 1 | IO_L24N_1 | K16 | I/O |
| 1 | IO_L24P_1 | J17 | I/O |
| 1 | IO_L25N_1/A13 | H18 | DUAL |
| 1 | IO_L25P_1/A12 | H19 | DUAL |
| 1 | IO_L26N_1/A15 | G20 | DUAL |
| 1 | IO_L26P_1/A14 | H20 | DUAL |
| 1 | IO_L28N_1 | H17 | I/O |
| 1 | IO_L28P_1 | G18 | I/O |
| 1 | IO_L29N_1/A17 | F19 | DUAL |
| 1 | IO_L29P_1/A16 | F20 | DUAL |
| 1 | IO_L30N_1/A19 | F18 | DUAL |
| 1 | IO_L30P_1/A18 | G17 | DUAL |
| 1 | IO_L32N_1 | E19 | I/O |
| 1 | IO_L32P_1 | E20 | I/O |
| 1 | IO_L33N_1 | F17 | I/O |
| 1 | IO_L33P_1 | E18 | I/O |
| 1 | IO_L34N_1 | D18 | I/O |
| 1 | IO_L34P_1 | D20 | I/O |
| 1 | IO_L36N_1/A21 | F16 | DUAL |
| 1 | IO_L36P_1/A20 | G16 | DUAL |
| 1 | IO_L37N_1/A23 | C19 | DUAL |
| 1 | IO_L37P_1/A22 | C20 | DUAL |
| 1 | IO_L38N_1/A25 | B19 | DUAL |

*Table 76:* **Spartan-3AN FGG400 Pinout *(Cont'd)***

| Bank | Pin Name | FGG400 Ball | Type |
|---|---|---|---|
| 3 | IO_L34P_3 | U1 | I/O |
| 3 | IO_L36N_3 | T4 | I/O |
| 3 | IO_L36P_3 | R5 | I/O |
| 3 | IO_L37N_3 | V2 | I/O |
| 3 | IO_L37P_3 | V1 | I/O |
| 3 | IO_L38N_3 | W2 | I/O |
| 3 | IO_L38P_3 | W1 | I/O |
| 3 | IP_3 | H7 | INPUT |
| 3 | IP_L04N_3/VREF_3 | G6 | VREF |
| 3 | IP_L04P_3 | G7 | INPUT |
| 3 | IP_L11N_3/VREF_3 | J7 | VREF |
| 3 | IP_L11P_3 | J8 | INPUT |
| 3 | IP_L15N_3 | K7 | INPUT |
| 3 | IP_L15P_3 | K8 | INPUT |
| 3 | IP_L19N_3 | K5 | INPUT |
| 3 | IP_L19P_3 | K6 | INPUT |
| 3 | IP_L23N_3 | L6 | INPUT |
| 3 | IP_L23P_3 | L7 | INPUT |
| 3 | IP_L27N_3 | M7 | INPUT |
| 3 | IP_L27P_3 | M8 | INPUT |
| 3 | IP_L31N_3 | N7 | INPUT |
| 3 | IP_L31P_3 | M6 | INPUT |
| 3 | IP_L35N_3 | N6 | INPUT |
| 3 | IP_L35P_3 | P5 | INPUT |
| 3 | IP_L39N_3/VREF_3 | P7 | VREF |
| 3 | IP_L39P_3 | P6 | INPUT |
| 3 | VCCO_3 | E2 | VCCO |
| 3 | VCCO_3 | H5 | VCCO |
| 3 | VCCO_3 | L2 | VCCO |
| 3 | VCCO_3 | N5 | VCCO |
| 3 | VCCO_3 | U2 | VCCO |
| GND | GND | A1 | GND |
| GND | GND | A11 | GND |
| GND | GND | A20 | GND |
| GND | GND | B6 | GND |
| GND | GND | B14 | GND |
| GND | GND | C3 | GND |
| GND | GND | C18 | GND |
| GND | GND | D9 | GND |
| GND | GND | E5 | GND |

*Table 76:* **Spartan-3AN FGG400 Pinout *(Cont'd)***

| Bank | Pin Name | FGG400 Ball | Type |
|---|---|---|---|
| GND | GND | E12 | GND |
| GND | GND | F15 | GND |
| GND | GND | G2 | GND |
| GND | GND | G19 | GND |
| GND | GND | H8 | GND |
| GND | GND | H13 | GND |
| GND | GND | J9 | GND |
| GND | GND | J11 | GND |
| GND | GND | K1 | GND |
| GND | GND | K10 | GND |
| GND | GND | K12 | GND |
| GND | GND | K17 | GND |
| GND | GND | L4 | GND |
| GND | GND | L9 | GND |
| GND | GND | L11 | GND |
| GND | GND | L20 | GND |
| GND | GND | M10 | GND |
| GND | GND | M12 | GND |
| GND | GND | N8 | GND |
| GND | GND | N11 | GND |
| GND | GND | N13 | GND |
| GND | GND | P2 | GND |
| GND | GND | P19 | GND |
| GND | GND | R6 | GND |
| GND | GND | R9 | GND |
| GND | GND | T16 | GND |
| GND | GND | U12 | GND |
| GND | GND | V3 | GND |
| GND | GND | V18 | GND |
| GND | GND | W7 | GND |
| GND | GND | W15 | GND |
| GND | GND | Y1 | GND |
| GND | GND | Y10 | GND |
| GND | GND | Y20 | GND |
| VCCAUX | SUSPEND | R15 | PWR MGMT |
| VCCAUX | DONE | W19 | CONFIG |
| VCCAUX | PROG_B | D5 | CONFIG |
| VCCAUX | TCK | A19 | JTAG |
| VCCAUX | TDI | F5 | JTAG |
| VCCAUX | TDO | E17 | JTAG |

*Table 78:* **Spartan-3AN FGG484 Pinout *(Cont'd)***

| Bank | Pin Name | FGG484 Ball | Type |
|---|---|---|---|
| 1 | IO_L25N_1/RHCLK7 | K19 | RHCLK |
| 1 | IO_L25P_1/IRDY1/RHCLK6 | K20 | RHCLK |
| 1 | IO_L26N_1/A11 | J22 | DUAL |
| 1 | IO_L26P_1/A10 | K22 | DUAL |
| 1 | IO_L28N_1 | L19 | I/O |
| 1 | IO_L28P_1 | L18 | I/O |
| 1 | IO_L29N_1/A13 | J20 | DUAL |
| 1 | IO_L29P_1/A12 | J21 | DUAL |
| 1 | IO_L30N_1/A15 | G22 | DUAL |
| 1 | IO_L30P_1/A14 | H22 | DUAL |
| 1 | IO_L32N_1 | K18 | I/O |
| 1 | IO_L32P_1 | K17 | I/O |
| 1 | IO_L33N_1/A17 | H20 | DUAL |
| 1 | IO_L33P_1/A16 | H21 | DUAL |
| 1 | IO_L34N_1/A19 | F21 | DUAL |
| 1 | IO_L34P_1/A18 | F22 | DUAL |
| 1 | IO_L36N_1 | G20 | I/O |
| 1 | IO_L36P_1 | G19 | I/O |
| 1 | IO_L37N_1 | H19 | I/O |
| 1 | IO_L37P_1 | J18 | I/O |
| 1 | IO_L38N_1 | F20 | I/O |
| 1 | IO_L38P_1 | E20 | I/O |
| 1 | IO_L40N_1 | F18 | I/O |
| 1 | IO_L40P_1 | F19 | I/O |
| 1 | IO_L41N_1 | D22 | I/O |
| 1 | IO_L41P_1 | E22 | I/O |
| 1 | IO_L42N_1 | D20 | I/O |
| 1 | IO_L42P_1 | D21 | I/O |
| 1 | IO_L44N_1/A21 | C21 | DUAL |
| 1 | IO_L44P_1/A20 | C22 | DUAL |
| 1 | IO_L45N_1/A23 | B21 | DUAL |
| 1 | IO_L45P_1/A22 | B22 | DUAL |
| 1 | IO_L46N_1/A25 | G17 | DUAL |
| 1 | IO_L46P_1/A24 | G18 | DUAL |
| 1 | IP_L04N_1/VREF_1 | R16 | VREF |
| 1 | IP_L04P_1 | R15 | INPUT |
| 1 | IP_L08N_1 | P16 | INPUT |
| 1 | IP_L08P_1 | P15 | INPUT |
| 1 | IP_L12N_1/VREF_1 | R18 | VREF |
| 1 | IP_L12P_1 | R17 | INPUT |

*Table 78:* **Spartan-3AN FGG484 Pinout *(Cont'd)***

| Bank | Pin Name | FGG484 Ball | Type |
|---|---|---|---|
| 1 | IP_L16N_1/VREF_1 | N16 | VREF |
| 1 | IP_L16P_1 | N15 | INPUT |
| 1 | IP_L23N_1 | M16 | INPUT |
| 1 | IP_L23P_1 | M17 | INPUT |
| 1 | IP_L27N_1 | L16 | INPUT |
| 1 | IP_L27P_1/VREF_1 | M15 | VREF |
| 1 | IP_L31N_1 | K16 | INPUT |
| 1 | IP_L31P_1 | L15 | INPUT |
| 1 | IP_L35N_1 | K15 | INPUT |
| 1 | IP_L35P_1/VREF_1 | K14 | VREF |
| 1 | IP_L39N_1 | H18 | INPUT |
| 1 | IP_L39P_1 | H17 | INPUT |
| 1 | IP_L43N_1/VREF_1 | J15 | VREF |
| 1 | IP_L43P_1 | J16 | INPUT |
| 1 | IP_L47N_1 | H15 | INPUT |
| 1 | IP_L47P_1/VREF_1 | H16 | VREF |
| 1 | VCCO_1 | E21 | VCCO |
| 1 | VCCO_1 | J17 | VCCO |
| 1 | VCCO_1 | K21 | VCCO |
| 1 | VCCO_1 | P17 | VCCO |
| 1 | VCCO_1 | P21 | VCCO |
| 1 | VCCO_1 | V21 | VCCO |
| 2 | IO_L01N_2/M0 | W5 | DUAL |
| 2 | IO_L01P_2/M1 | V6 | DUAL |
| 2 | IO_L02N_2/CSO_B | Y4 | DUAL |
| 2 | IO_L02P_2/M2 | W4 | DUAL |
| 2 | IO_L03N_2 | AA3 | I/O |
| 2 | IO_L03P_2 | AB2 | I/O |
| 2 | IO_L04N_2 | AA4 | I/O |
| 2 | IO_L04P_2 | AB3 | I/O |
| 2 | IO_L05N_2 | Y5 | I/O |
| 2 | IO_L05P_2 | W6 | I/O |
| 2 | IO_L06N_2 | AB5 | I/O |
| 2 | IO_L06P_2 | AB4 | I/O |
| 2 | IO_L07N_2 | Y6 | I/O |
| 2 | IO_L07P_2 | W7 | I/O |
| 2 | IO_L08N_2 | AB6 | I/O |
| 2 | IO_L08P_2 | AA6 | I/O |
| 2 | IO_L09N_2/VS2 | W9 | DUAL |
| 2 | IO_L09P_2/RDWR_B | V9 | DUAL |

## User I/Os by Bank

Table 79 and Table 80 indicate how the user-I/O pins are distributed between the four I/O banks on the FGG484 package. The AWAKE pin is counted as a dual-purpose I/O.

*Table 79:* **User I/Os Per Bank for the XC3S700AN in the FGG484 Package**

| Package Edge | I/O Bank | Maximum I/Os | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF | CLK |
| Top | 0 | 92 | 58 | 17 | 1 | 8 | 8 |
| Right | 1 | 94 | 33 | 15 | 30 | 8 | 8 |
| Bottom | 2 | 92 | 43 | 11 | 21 | 9 | 8 |
| Left | 3 | 94 | 61 | 17 | 0 | 8 | 8 |
| **Total** | | **372** | **195** | **60** | **52** | **33** | **32** |

*Table 80:* **User I/Os Per Bank for the XC3S1400AN in the FGG484 Package**

| Package Edge | I/O Bank | Maximum I/Os | All Possible I/O Pins by Type | | | | |
|---|---|---|---|---|---|---|---|
| | | | I/O | INPUT | DUAL | VREF | CLK |
| Top | 0 | 92 | 58 | 17 | 1 | 8 | 8 |
| Right | 1 | 94 | 33 | 15 | 30 | 8 | 8 |
| Bottom | 2 | 95 | 43 | 13 | 21 | 10 | 8 |
| Left | 3 | 94 | 61 | 17 | 0 | 8 | 8 |
| **Total** | | **375** | **195** | **62** | **52** | **34** | **32** |

## Footprint Migration Differences

Table 81 summarizes the three footprint and functionality differences between the XC3S700AN and the XC3S1400AN FPGAs that can affect migration between devices available in the FGG484 package. All other pins unconditionally migrate between the Spartan-3AN devices available in the FGG484 package.

Spartan-3AN FPGAs are pin compatible with the same density Spartan-3A FPGAs in the FG(G)484 package, although the Spartan-3A FPGAs require an external configuration source.

In Table 81, the arrow (→) indicates that this pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

*Table 81:* **FGG484 XC3S700AN to XC3S1400AN Footprint Migration/Differences**

| FGG484 Ball | Bank | XC3S700AN | Migration | XC3S1400AN |
|---|---|---|---|---|
| T8 | 2 | N.C. | → | INPUT/VREF |
| U7 | 2 | N.C. | → | INPUT |
| U16 | 2 | N.C. | → | INPUT |
| **Number of Differences:** | | | 3 | |

*Table 82:* **Spartan-3AN FGG676 Pinout *(Cont'd)***

| Bank | Pin Name | FGG676 Ball | Type |
|---|---|---|---|
| 2 | IO_L15N_2 | AC9 | I/O |
| 2 | IO_L15P_2 | AB9 | I/O |
| 2 | IO_L16N_2 | W12 | I/O |
| 2 | IO_L16P_2 | V12 | I/O |
| 2 | IO_L17N_2/VS2 | AA12 | DUAL |
| 2 | IO_L17P_2/RDWR_B | Y12 | DUAL |
| 2 | IO_L18N_2 | AF8 | I/O |
| 2 | IO_L18P_2 | AE8 | I/O |
| 2 | IO_L19N_2/VS0 | AF9 | DUAL |
| 2 | IO_L19P_2/VS1 | AE9 | DUAL |
| 2 | IO_L20N_2 | W13 | I/O |
| 2 | IO_L20P_2 | V13 | I/O |
| 2 | IO_L21N_2 | AC12 | I/O |
| 2 | IO_L21P_2 | AB12 | I/O |
| 2 | IO_L22N_2/D6 | AF10 | DUAL |
| 2 | IO_L22P_2/D7 | AE10 | DUAL |
| 2 | IO_L23N_2 | AC11 | I/O |
| 2 | IO_L23P_2 | AD11 | I/O |
| 2 | IO_L24N_2/D4 | AE12 | DUAL |
| 2 | IO_L24P_2/D5 | AF12 | DUAL |
| 2 | IO_L25N_2/GCLK13 | Y13 | GCLK |
| 2 | IO_L25P_2/GCLK12 | AA13 | GCLK |
| 2 | IO_L26N_2/GCLK15 | AE13 | GCLK |
| 2 | IO_L26P_2/GCLK14 | AF13 | GCLK |
| 2 | IO_L27N_2/GCLK1 | AA14 | GCLK |
| 2 | IO_L27P_2/GCLK0 | Y14 | GCLK |
| 2 | IO_L28N_2/GCLK3 | AE14 | GCLK |
| 2 | IO_L28P_2/GCLK2 | AF14 | GCLK |
| 2 | IO_L29N_2 | AC14 | I/O |
| 2 | IO_L29P_2 | AD14 | I/O |
| 2 | IO_L30N_2/MOSI/CSI_B | AB15 | DUAL |
| 2 | IO_L30P_2 | AC15 | I/O |
| 2 | IO_L31N_2 | W15 | I/O |
| 2 | IO_L31P_2 | V14 | I/O |
| 2 | IO_L32N_2/DOUT | AE15 | DUAL |
| 2 | IO_L32P_2/AWAKE | AD15 | PWR MGMT |
| 2 | IO_L33N_2 | AD17 | I/O |
| 2 | IO_L33P_2 | AE17 | I/O |
| 2 | IO_L34N_2/D3 | Y15 | DUAL |
| 2 | IO_L34P_2/INIT_B | AA15 | DUAL |

*Table 82:* **Spartan-3AN FGG676 Pinout *(Cont'd)***

| Bank | Pin Name | FGG676 Ball | Type |
|---|---|---|---|
| 2 | IO_L35N_2 | U15 | I/O |
| 2 | IO_L35P_2 | V15 | I/O |
| 2 | IO_L36N_2/D1 | AE18 | DUAL |
| 2 | IO_L36P_2/D2 | AF18 | DUAL |
| 2 | IO_L37N_2 | AE19 | I/O |
| 2 | IO_L37P_2 | AF19 | I/O |
| 2 | IO_L38N_2 | AB16 | I/O |
| 2 | IO_L38P_2 | AC16 | I/O |
| 2 | IO_L39N_2 | AE20 | I/O |
| 2 | IO_L39P_2 | AF20 | I/O |
| 2 | IO_L40N_2 | AC19 | I/O |
| 2 | IO_L40P_2 | AD19 | I/O |
| 2 | IO_L41N_2 | AC20 | I/O |
| 2 | IO_L41P_2 | AD20 | I/O |
| 2 | IO_L42N_2 | U16 | I/O |
| 2 | IO_L42P_2 | V16 | I/O |
| 2 | IO_L43N_2 | Y17 | I/O |
| 2 | IO_L43P_2 | AA17 | I/O |
| 2 | IO_L44N_2 | AD21 | I/O |
| 2 | IO_L44P_2 | AE21 | I/O |
| 2 | IO_L45N_2 | AC21 | I/O |
| 2 | IO_L45P_2 | AD22 | I/O |
| 2 | IO_L46N_2 | V17 | I/O |
| 2 | IO_L46P_2 | W17 | I/O |
| 2 | IO_L47N_2 | AA18 | I/O |
| 2 | IO_L47P_2 | AB18 | I/O |
| 2 | IO_L48N_2 | AE23 | I/O |
| 2 | IO_L48P_2 | AF23 | I/O |
| 2 | IO_L51N_2 | AE25 | I/O |
| 2 | IO_L51P_2 | AF25 | I/O |
| 2 | IO_L52N_2/CCLK | AE24 | DUAL |
| 2 | IO_L52P_2/D0/DIN/MISO | AF24 | DUAL |
| 2 | IP_2 | AA19 | INPUT |
| 2 | IP_2 | AB13 | INPUT |
| 2 | IP_2 | AB17 | INPUT |
| 2 | IP_2 | AB20 | INPUT |
| 2 | IP_2 | AC7 | INPUT |
| 2 | IP_2 | AC13 | INPUT |
| 2 | IP_2 | AC17 | INPUT |
| 2 | IP_2 | AC18 | INPUT |