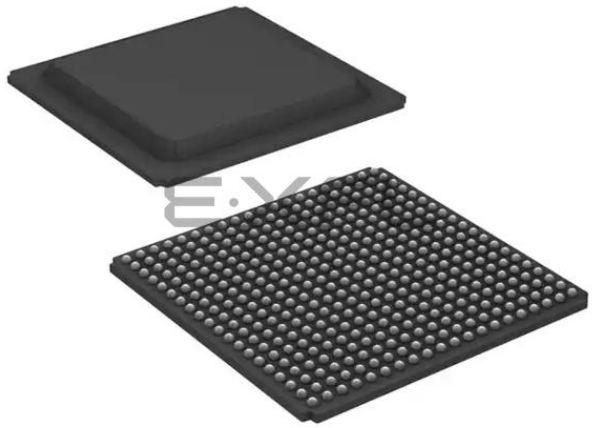
AMD Xilinx - XC3S400AN-5FGG400C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	368640
Number of I/O	311
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400an-5fgg400c

- Sector-based data protection and security features
  - Sector Protect: Write- and erase-protect a sector (changeable)
  - Sector Lockdown: Sector data is unchangeable (permanent)
- 128-byte Security Register
  - Separate from FPGA's unique Device DNA identifier
  - 64-byte factory-programmed identifier unique to the in-system Flash memory
  - 64-byte one-time programmable, user-programmable field
- 100,000 Program/Erase cycles
- 20-year data retention
- Comprehensive programming support
  - In-system prototype programming via JTAG using Xilinx Platform Cable USB and iMPACT software
  - Product programming support using BPM Microsystems programmers with appropriate programming adapter
  - Design examples demonstrating in-system programming from a Spartan-3AN FPGA application

I/O Capabilities

The Spartan-3AN FPGA SelectIO interface supports many popular single-ended and differential standards. Table 4 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional, input-only pins as indicated in Table 4.

Spartan-3AN FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3AN FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 4: **Available User I/Os and Differential (Diff) I/O Pairs**

Package(1)	**TQ144 TQG144**		**FT256 FTG256**		**FG400 FGG400**		**FG484 FGG484**		**FG676 FGG676**	
Body Size (mm)	**20 x 20**(2)		**17 x 17**		**21 x 21**		**23 x 23**		**27 x 27**	
Device(3)	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**
XC3S50AN	**108**(4) *(7)*	**50** *(24)*	**144** *(32)*	**64** *(32)*	–	–	–	–	–	–
XC3S200AN	–	–	**195** *(35)*	**90** *(50)*	–	–	–	–	–	–
XC3S400AN	–	–	**195** *(35)*	**90** *(50)*	**311** *(63)*	**142** *(78)*	–	–	–	–
XC3S700AN	–	–	–	–	–	–	**372** *(84)*	**165** *(93)*	–	–
XC3S1400AN	–	–	–	–	–	–	**375** *(87)*	**165** *(93)*	**502** *(94)*	**227** *(131)*

Notes:

1. See Pb and Pb-Free Packaging, page 7 for details on Pb and Pb-free packaging options.
2. The footprint for the TQ(G)144 (22 mm x 22 mm) package is larger than the package body.
3. Each Spartan-3AN FPGA has a pin-compatible Spartan-3A FPGA equivalent, although Spartan-3A FPGAs do not have internal SPI flash and offer more part/package combinations.
4. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

Ordering Information

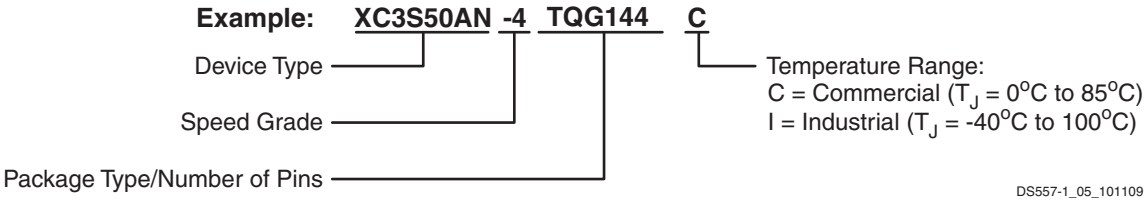


Figure 5: **Device Numbering Format**

Device	Speed Grade		Package Type / Number of Pins		Temperature Range (T_J)	
XC3S50AN	-4	Standard Performance	TQ144/ TQG144	144-pin Thin Quad Flat Pack (TQFP)	C	Commercial (0°C to 85°C)
XC3S200AN	-5	High Performance(1)	FT256/ FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)	I	Industrial (–40°C to 100°C)
XC3S400AN			FG400/ FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3S700AN			FG484/ FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)		
XC3S1400AN			FG676/ FGG676	676-ball Fine-Pitch Ball Grid Array (FBGA)		

Notes:

1. The -5 speed grade is exclusively available in the Commercial temperature range.
2. See Table 4 and Table 5 for available package combinations.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device.
09/12/07	2.0.1	Noted that only dual-mark devices are guaranteed for both -4I and -5C.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that non-Pb-free packages may be available for selected devices.
06/02/08	3.1	Minor updates.
11/19/09	3.2	Updated document throughout to reflect availability of Pb package options. Added references to the Extended Spartan-3A family. Removed table note 2 from Table 2. In Table 4, added Pb packages, added table note 4, and updated table note 2. Added Table 5.
12/02/10	4.0	Updated Notice of Disclaimer.
04/01/11	4.1	In Table 2, revised the Maximum Differential I/O Pairs and Maximum User I/O values for the XC3S50AN. In Table 4, added packages to the XC3S50AN, XC3S400AN, and XC3S1400AN. Updated Pb and Pb-Free Packaging section and Table 5 to include the new device/package combinations for the XC3S50AN, XC3S400AN, and XC3S1400AN.

Pin-to-Pin Setup and Hold Times

Table 22: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50AN	2.45	2.68	ns
			XC3S200AN	2.59	2.84	ns
			XC3S400AN	2.38	2.68	ns
			XC3S700AN	2.38	2.57	ns
			XC3S1400AN	1.91	2.17	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 5, without DCM	XC3S50AN	2.55	2.76	ns
			XC3S200AN	2.32	2.76	ns
			XC3S400AN	2.21	2.60	ns
			XC3S700AN	2.28	2.63	ns
			XC3S1400AN	2.33	2.41	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50AN	–0.36	–0.36	ns
			XC3S200AN	–0.52	–0.52	ns
			XC3S400AN	–0.33	–0.29	ns
			XC3S700AN	–0.17	–0.12	ns
			XC3S1400AN	–0.07	0.00	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 5, without DCM	XC3S50AN	–0.63	–0.58	ns
			XC3S200AN	–0.56	–0.56	ns
			XC3S400AN	–0.42	–0.42	ns
			XC3S700AN	–0.80	–0.75	ns
			XC3S1400AN	–0.69	–0.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 26. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 26. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Setup and Hold Times

Table 23: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25[2]	0	XC3S50AN	1.56	1.58	ns
				XC3S200AN	1.71	1.81	ns
				XC3S400AN	1.30	1.51	ns
				XC3S700AN	1.34	1.51	ns
				XC3S1400AN	1.36	1.74	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25[2]	1	XC3S50AN	2.16	2.18	ns
			2		3.10	3.12	ns
			3		3.51	3.76	ns
			4		4.04	4.32	ns
			5		3.88	4.24	ns
			6		4.72	5.09	ns
			7		5.47	5.94	ns
			8		5.97	6.52	ns
			1	XC3S200AN	2.05	2.20	ns
			2		2.72	2.93	ns
			3		3.38	3.78	ns
			4		3.88	4.37	ns
			5		3.69	4.20	ns
			6		4.56	5.23	ns
			7		5.34	6.11	ns
			8		5.85	6.71	ns
			1	XC3S400AN	1.79	2.02	ns
			2		2.43	2.67	ns
			3		3.02	3.43	ns
			4		3.49	3.96	ns
			5		3.41	3.95	ns
			6		4.20	4.81	ns
			7		4.96	5.66	ns
			8		5.44	6.19	ns

Table 23: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25(3)	1	XC3S400AN	–1.12	–1.12	ns
			2		–1.70	–1.70	ns
			3		–2.08	–2.08	ns
			4		–2.38	–2.38	ns
			5		–2.23	–2.23	ns
			6		–2.69	–2.69	ns
			7		–3.08	–3.08	ns
			8		–3.35	–3.35	ns
			1	XC3S700AN	–1.67	–1.67	ns
			2		–2.27	–2.27	ns
			3		–2.59	–2.59	ns
			4		–2.92	–2.92	ns
			5		–2.89	–2.89	ns
			6		–3.22	–3.22	ns
			7		–3.52	–3.52	ns
			8		–3.81	–3.81	ns
			1	XC3S1400AN	–1.60	–1.60	ns
			2		–2.06	–2.06	ns
			3		–2.46	–2.46	ns
			4		–2.86	–2.86	ns
			5		–2.88	–2.88	ns
			6		–3.24	–3.24	ns
			7		–3.55	–3.55	ns
			8		–3.89	–3.89	ns
Set/Reset Pulse Width							
T_{RPW_IOB}	Minimum pulse width to SR control input on IOB	–	–	All	1.33	1.61	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 26.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 26. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 24: **Sample Window (Source Synchronous)**

Symbol	Description	Maximum	Units
T_{SAMP}	Setup and hold capture window of an IOB flip-flop.	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. • Answer Record 30879	ps

Output Timing Adjustments

Table 29: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
Single-Ended Standards					
LVTTL	Slow	2 mA	5.58	5.58	ns
		4 mA	3.16	3.16	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.62	1.62	ns
		16 mA	1.24	1.24	ns
		24 mA	2.74(3)	2.74(3)	ns
	Fast	2 mA	3.03	3.03	ns
		4 mA	1.71	1.71	ns
		6 mA	1.71	1.71	ns
		8 mA	0.53	0.53	ns
		12 mA	0.53	0.53	ns
		16 mA	0.59	0.59	ns
		24 mA	0.60	0.60	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.67	16.67	ns
		16 mA	16.22	16.22	ns
		24 mA	12.11	12.11	ns

Table 29: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS33	Slow	2 mA	5.58	5.58	ns
		4 mA	3.17	3.17	ns
		6 mA	3.17	3.17	ns
		8 mA	2.09	2.09	ns
		12 mA	1.24	1.24	ns
		16 mA	1.15	1.15	ns
		24 mA	2.55(3)	2.55(3)	ns
	Fast	2 mA	3.02	3.02	ns
		4 mA	1.71	1.71	ns
		6 mA	1.72	1.72	ns
		8 mA	0.53	0.53	ns
		12 mA	0.59	0.59	ns
		16 mA	0.59	0.59	ns
		24 mA	0.51	0.51	ns
	QuietIO	2 mA	27.67	27.67	ns
		4 mA	27.67	27.67	ns
		6 mA	27.67	27.67	ns
		8 mA	16.71	16.71	ns
		12 mA	16.29	16.29	ns
		16 mA	16.18	16.18	ns
		24 mA	12.11	12.11	ns

Table 29: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26(3)	2.26(3)	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns

Table 29: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns

Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type			
			TQG144		FTG256, FGG400, FGG484, FGG676	
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
LVCMOS25	Slow	2	16	16	76	76
		4	10	10	46	46
		6	8	8	33	33
		8	7	7	24	24
		12	6	6	18	18
		16	–	6	–	11
		24	–	5	–	7
	Fast	2	12	12	18	18
		4	10	10	14	14
		6	8	8	6	6
		8	6	6	6	6
		12	3	3	3	3
		16	–	3	–	3
		24	–	2	–	2
	QuietIO	2	36	36	76	76
		4	30	30	60	60
		6	24	24	48	48
		8	20	20	36	36
		12	12	12	36	36
		16	–	12	–	36
		24	–	8	–	8

Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type			
			TQG144		FTG256, FGG400, FGG484, FGG676	
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
LVCMOS18	Slow	2	13	13	64	64
		4	8	8	34	34
		6	8	8	22	22
		8	7	7	18	18
		12	–	5	–	13
		16	–	5	–	10
	Fast	2	13	13	18	18
		4	8	8	9	9
		6	7	7	7	7
		8	4	4	4	4
		12	–	4	–	4
		16	–	3	–	3
	QuietIO	2	30	30	64	64
		4	24	24	64	64
		6	20	20	48	48
		8	16	16	36	36
		12	–	12	–	36
		16	–	12	–	24
LVCMOS15	Slow	2	12	12	55	55
		4	7	7	31	31
		6	7	7	18	18
		8	–	6	–	15
		12	–	5	–	10
	Fast	2	10	10	25	25
		4	7	7	10	10
		6	6	6	6	6
		8	–	4	–	4
		12	–	3	–	3
	QuietIO	2	30	30	70	70
		4	21	21	40	40
		6	18	18	31	31
		8	–	12	–	31
		12	–	12	–	20

Configurable Logic Block (CLB) Timing

Table 33: **CLB (SLICEM) Timing**

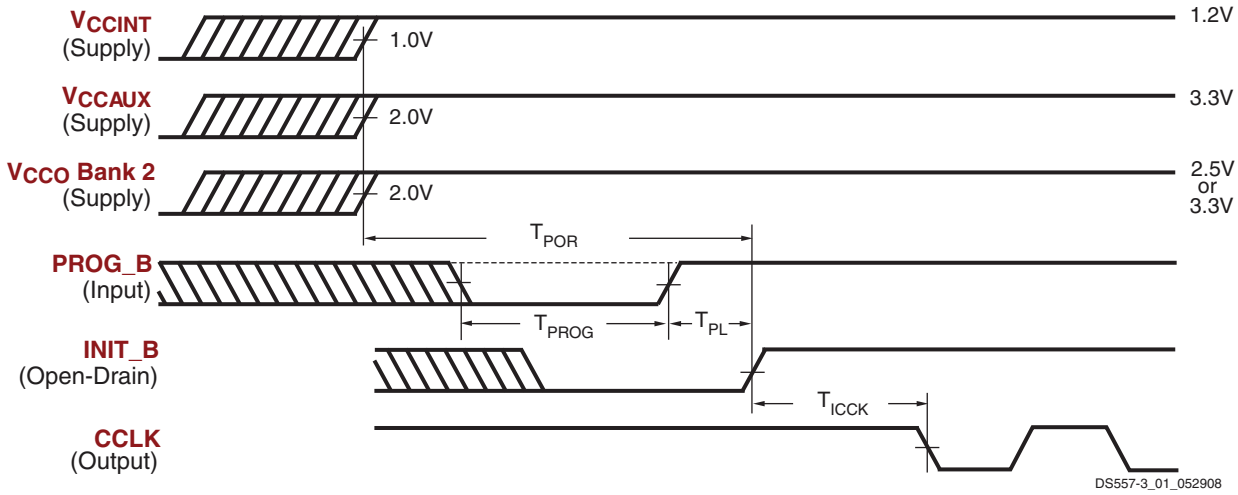
Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	0	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	–	0	–	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10.

Configuration and JTAG Timing

General Configuration Power-On/Reconfigure Timing



Notes:

1. When configuring from the In-System Flash, V_{CCAUX} must be in the recommended operating range; on power-up make sure V_{CCAUX} reaches at least 3.0V before INIT_B goes High to indicate the start of configuration. V_{CCINT}, V_{CCAUX}, and V_{CCO} supplies to the FPGA can be applied in any order if this requirement is met.
2. The Low-going pulse on PROG_B is optional after power-on but necessary for reconfiguration without a power cycle.
3. The rising edge of INIT_B samples the voltage levels applied to the mode pins (M0 - M2).

Figure 13: **Waveforms for Power-On and the Beginning of Configuration**

Table 50: **Power-On Timing and the Beginning of Configuration**

Symbol	Description	Device	All Speed Grades		Units
			Min	Max	
T_{POR}(2)	The time from the application of V_{CCINT}, V_{CCAUX}, and V_{CCO} Bank 2 supply voltage ramps (whichever occurs last) to the rising transition of the INIT_B pin	All	–	18	ms
T_{PROG}	The width of the low-going pulse on the PROG_B pin	All	0.5	–	µs
T_{PL}(2)	The time from the rising edge of the PROG_B pin to the rising transition on the INIT_B pin	XC3S50AN	–	0.5	ms
		XC3S200AN	–	0.5	ms
		XC3S400AN	–	1	ms
		XC3S700AN	–	2	ms
		XC3S1400AN	–	2	ms
T_{INIT}	Minimum Low pulse width on INIT_B output	All	250	–	ns
T_{ICCK}(3)	The time from the rising edge of the INIT_B pin to the generation of the configuration clock signal at the CCLK output pin	All	0.5	4	µs

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10. This means power must be applied to all V_{CCINT}, V_{CCO}, and V_{CCAUX} lines.
2. Power-on reset and the clearing of configuration memory occurs during this period.
3. This specification applies only to the Master Serial, SPI, and BPI modes.
4. For details on configuration, see UG332 *Spartan-3 Generation Configuration User Guide*.

Table 52: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F_{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F_{CCLK6}		6 (*default*)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F_{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F_{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F_{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F_{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F_{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F_{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F_{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F_{CCLK25}		25	Commercial	10.00	20.90	MHz
			Industrial		22.23	MHz
F_{CCLK27}		27	Commercial	10.80	22.39	MHz
			Industrial		23.81	MHz
F_{CCLK33}		33	Commercial	13.20	27.48	MHz
			Industrial		29.23	MHz
F_{CCLK44}		44	Commercial	17.60	37.60	MHz
			Industrial		40.00	MHz
F_{CCLK50}		50	Commercial	20.00	44.80	MHz
			Industrial		47.66	MHz
$F_{CCLK100}$		100	Commercial	40.00	88.68	MHz
			Industrial		94.34	MHz

Table 53: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting															Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T_{MCCL}, T_{MCCH}	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 68: **Spartan-3AN TQG144 Pinout *(Cont'd)***

Bank	Pin Name	Pin	Type
2	IO_L05P_2	P46	I/O
2	IO_L06N_2/D6	P49	DUAL
2	IO_L06P_2	P47	I/O
2	IO_L07N_2/D4	P51	DUAL
2	IO_L07P_2/D5	P50	DUAL
2	IO_L08N_2/GCLK15	P55	GCLK
2	IO_L08P_2/GCLK14	P54	GCLK
2	IO_L09N_2/GCLK1	P59	GCLK
2	IO_L09P_2/GCLK0	P57	GCLK
2	IO_L10N_2/GCLK3	P60	GCLK
2	IO_L10P_2/GCLK2	P58	GCLK
2	IO_L11N_2/DOUT	P64	DUAL
2	IO_L11P_2/AWAKE	P63	PWR MGMT
2	IO_L12N_2/D3	P68	DUAL
2	IO_L12P_2/INIT_B	P67	DUAL
2	IO_L13N_2/D0/DIN/MISO	P71	DUAL
2	IO_L13P_2/D2	P69	DUAL
2	IO_L14N_2/CCLK	P72	DUAL
2	IO_L14P_2/D1	P70	DUAL
2	IP_2/VREF_2	P53	VREF
2	VCCO_2	P40	VCCO
2	VCCO_2	P61	VCCO
3	IO_L01N_3	P6	I/O
3	IO_L01P_3	P4	I/O
3	IO_L02N_3	P5	I/O
3	IO_L02P_3	P3	I/O
3	IO_L03N_3	P8	I/O
3	IO_L03P_3	P7	I/O
3	IO_L04N_3/VREF_3	P11	VREF
3	IO_L04P_3	P10	I/O
3	IO_L05N_3/LHCLK1	P13	LHCLK
3	IO_L05P_3/LHCLK0	P12	LHCLK
3	IO_L06N_3/IRDY2/LHCLK3	P16	LHCLK
3	IO_L06P_3/LHCLK2	P15	LHCLK
3	IO_L07N_3/LHCLK5	P20	LHCLK
3	IO_L07P_3/LHCLK4	P18	LHCLK
3	IO_L08N_3/LHCLK7	P21	LHCLK
3	IO_L08P_3/TRDY2/LHCLK6	P19	LHCLK
3	IO_L09N_3	P25	I/O
3	IO_L09P_3	P24	I/O
3	IO_L10N_3	P29	I/O
3	IO_L10P_3	P27	I/O

Table 68: **Spartan-3AN TQG144 Pinout *(Cont'd)***

Bank	Pin Name	Pin	Type
3	IO_L11N_3	P30	I/O
3	IO_L11P_3	P28	I/O
3	IO_L12N_3	P32	I/O
3	IO_L12P_3	P31	I/O
3	IP_L13N_3/VREF_3	P35	VREF
3	IP_L13P_3	P33	INPUT
3	VCCO_3	P14	VCCO
3	VCCO_3	P23	VCCO
GND	GND	P9	GND
GND	GND	P17	GND
GND	GND	P26	GND
GND	GND	P34	GND
GND	GND	P56	GND
GND	GND	P65	GND
GND	GND	P81	GND
GND	GND	P89	GND
GND	GND	P100	GND
GND	GND	P106	GND
GND	GND	P118	GND
GND	GND	P128	GND
GND	GND	P137	GND
VCCAUX	SUSPEND	P74	PWR MGMT
VCCAUX	DONE	P73	CONFIG
VCCAUX	PROG_B	P144	CONFIG
VCCAUX	TCK	P109	JTAG
VCCAUX	TDI	P2	JTAG
VCCAUX	TDO	P107	JTAG
VCCAUX	TMS	P1	JTAG
VCCAUX	VCCAUX	P36	VCCAUX
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P108	VCCAUX
VCCAUX	VCCAUX	P133	VCCAUX
VCCINT	VCCINT	P22	VCCINT
VCCINT	VCCINT	P52	VCCINT
VCCINT	VCCINT	P94	VCCINT
VCCINT	VCCINT	P122	VCCINT

Table 70: **Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN) *(Cont'd)***

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
1	IO_L10P_1	IO_L10P_1/A8	J12	DUAL
1	IO_L11N_1/RHCLK1	IO_L11N_1/RHCLK1	K14	RHCLK
1	IO_L11P_1/RHCLK0	IO_L11P_1/RHCLK0	K15	RHCLK
1	IO_L12N_1/TRDY1/RHCLK3	IO_L12N_1/TRDY1/RHCLK3	J16	RHCLK
1	IO_L12P_1/RHCLK2	IO_L12P_1/RHCLK2	K16	RHCLK
1	IO_L14N_1/RHCLK5	IO_L14N_1/RHCLK5	H14	RHCLK
1	IO_L14P_1/RHCLK4	IO_L14P_1/RHCLK4	J14	RHCLK
1	IO_L15N_1/RHCLK7	IO_L15N_1/RHCLK7	H16	RHCLK
1	IO_L15P_1/IRDY1/RHCLK6	IO_L15P_1/IRDY1/RHCLK6	H15	RHCLK
1	N.C.	IO_L16N_1/A11	F16	DUAL
1	N.C.	IO_L16P_1/A10	G16	DUAL
1	N.C.	IO_L17N_1/A13	G14	DUAL
1	N.C.	IO_L17P_1/A12	H13	DUAL
1	N.C.	IO_L18N_1/A15	F15	DUAL
1	N.C.	IO_L18P_1/A14	E16	DUAL
1	N.C.	IO_L19N_1/A17	F14	DUAL
1	N.C.	IO_L19P_1/A16	G13	DUAL
1	IO_L20N_1	IO_L20N_1/A19	F13	DUAL
1	IO_L20P_1	IO_L20P_1/A18	E14	DUAL
1	IO_L22N_1	IO_L22N_1/A21	D15	DUAL
1	IO_L22P_1	IO_L22P_1/A20	D16	DUAL
1	IO_L23N_1	IO_L23N_1/A23	D14	DUAL
1	IO_L23P_1	IO_L23P_1/A22	E13	DUAL
1	IO_L24N_1	IO_L24N_1/A25	C15	DUAL
1	IO_L24P_1	IO_L24P_1/A24	C16	DUAL
1	IP_L04N_1/VREF_1	IP_L04N_1/VREF_1	K12	VREF
1	IP_L04P_1	IP_L04P_1	K11	INPUT
1	N.C.	IP_L09N_1	J11	INPUT
1	N.C.	IP_L09P_1/VREF_1	J10	VREF
1	IP_L13N_1	IP_L13N_1	H11	INPUT
1	IP_L13P_1	IP_L13P_1	H10	INPUT
1	IP_L21N_1	IP_L21N_1	G11	INPUT
1	IP_L21P_1/VREF_1	IP_L21P_1/VREF_1	G12	VREF
1	IP_L25N_1	IP_L25N_1	F11	INPUT
1	IP_L25P_1/VREF_1	IP_L25P_1/VREF_1	F12	VREF
1	VCCO_1	VCCO_1	E15	VCCO
1	VCCO_1	VCCO_1	H12	VCCO
1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	N15	VCCO

Table 70: **Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN) *(Cont'd)***

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
2	IP_2	IP_2	L7	INPUT
2	IP_2	IP_2	L8	INPUT
2	IP_2/VREF_2	IP_2/VREF_2	L9	VREF
2	IP_2/VREF_2	IP_2/VREF_2	L10	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M8	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	IP_2/VREF_2	N5	VREF
2	VCCO_2	VCCO_2	M9	VCCO
2	VCCO_2	VCCO_2	R4	VCCO
2	VCCO_2	VCCO_2	R8	VCCO
2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	C1	I/O
3	IO_L01P_3	IO_L01P_3	C2	I/O
3	IO_L02N_3	IO_L02N_3	D3	I/O
3	IO_L02P_3	IO_L02P_3	D4	I/O
3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	D1	I/O
3	N.C.	IO_L05N_3	E2	I/O
3	N.C.	IO_L05P_3	E3	I/O
3	N.C.	IO_L07N_3	G4	I/O
3	N.C.	IO_L07P_3	F3	I/O
3	IO_L08N_3/VREF_3	IO_L08N_3/VREF_3	G1	VREF
3	IO_L08P_3	IO_L08P_3	F1	I/O
3	N.C.	IO_L09N_3	H4	I/O
3	N.C.	IO_L09P_3	G3	I/O
3	N.C.	IO_L10N_3	H5	I/O
3	N.C.	IO_L10P_3	H6	I/O
3	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	H1	LHCLK
3	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	G2	LHCLK
3	IO_L12N_3/IRDY2/LHCLK3	IO_L12N_3/IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	H3	LHCLK
3	IO_L14N_3/LHCLK5	IO_L14N_3/LHCLK5	J1	LHCLK
3	IO_L14P_3/LHCLK4	IO_L14P_3/LHCLK4	J2	LHCLK
3	IO_L15N_3/LHCLK7	IO_L15N_3/LHCLK7	K1	LHCLK
3	IO_L15P_3/TRDY2/LHCLK6	IO_L15P_3/TRDY2/LHCLK6	K3	LHCLK
3	N.C.	IO_L16N_3	L2	I/O
3	N.C.	IO_L16P_3/VREF_3	L1	VREF
3	N.C.	IO_L17N_3	J6	I/O
3	N.C.	IO_L17P_3	J4	I/O

Table 76: **Spartan-3AN FGG400 Pinout *(Cont'd)***

Bank	Pin Name	FGG400 Ball	Type
2	IO_L28P_2	Y16	I/O
2	IO_L29N_2	U16	I/O
2	IO_L29P_2	V16	I/O
2	IO_L30N_2	Y18	I/O
2	IO_L30P_2	Y17	I/O
2	IO_L31N_2	U17	I/O
2	IO_L31P_2	V17	I/O
2	IO_L32N_2/CCLK	Y19	DUAL
2	IO_L32P_2/D0/DIN/MISO	W18	DUAL
2	IP_2	P9	INPUT
2	IP_2	P12	INPUT
2	IP_2	P13	INPUT
2	IP_2	R8	INPUT
2	IP_2	R10	INPUT
2	IP_2	T11	INPUT
2	IP_2/VREF_2	N9	VREF
2	IP_2/VREF_2	N12	VREF
2	IP_2/VREF_2	P8	VREF
2	IP_2/VREF_2	P10	VREF
2	IP_2/VREF_2	P11	VREF
2	IP_2/VREF_2	R14	VREF
2	VCCO_2	R11	VCCO
2	VCCO_2	U8	VCCO
2	VCCO_2	U14	VCCO
2	VCCO_2	W5	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W17	VCCO
3	IO_L01N_3	D3	I/O
3	IO_L01P_3	D4	I/O
3	IO_L02N_3	C2	I/O
3	IO_L02P_3	B1	I/O
3	IO_L03N_3	D2	I/O
3	IO_L03P_3	C1	I/O
3	IO_L05N_3	E1	I/O
3	IO_L05P_3	D1	I/O
3	IO_L06N_3	G5	I/O
3	IO_L06P_3	F4	I/O
3	IO_L07N_3	J5	I/O
3	IO_L07P_3	J6	I/O
3	IO_L08N_3	H4	I/O

Table 76: **Spartan-3AN FGG400 Pinout *(Cont'd)***

Bank	Pin Name	FGG400 Ball	Type
3	IO_L08P_3	H6	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F3	I/O
3	IO_L10N_3	F2	I/O
3	IO_L10P_3	E3	I/O
3	IO_L12N_3	H2	I/O
3	IO_L12P_3	G3	I/O
3	IO_L13N_3/VREF_3	G1	VREF
3	IO_L13P_3	F1	I/O
3	IO_L14N_3	H3	I/O
3	IO_L14P_3	J4	I/O
3	IO_L16N_3	J2	I/O
3	IO_L16P_3	J3	I/O
3	IO_L17N_3/LHCLK1	K2	LHCLK
3	IO_L17P_3/LHCLK0	J1	LHCLK
3	IO_L18N_3/IRDY2/LHCLK3	L3	LHCLK
3	IO_L18P_3/LHCLK2	K3	LHCLK
3	IO_L20N_3/LHCLK5	L5	LHCLK
3	IO_L20P_3/LHCLK4	K4	LHCLK
3	IO_L21N_3/LHCLK7	M1	LHCLK
3	IO_L21P_3/TRDY2/LHCLK6	L1	LHCLK
3	IO_L22N_3	M3	I/O
3	IO_L22P_3/VREF_3	M2	VREF
3	IO_L24N_3	M5	I/O
3	IO_L24P_3	M4	I/O
3	IO_L25N_3	N2	I/O
3	IO_L25P_3	N1	I/O
3	IO_L26N_3	N4	I/O
3	IO_L26P_3	N3	I/O
3	IO_L28N_3	R1	I/O
3	IO_L28P_3	P1	I/O
3	IO_L29N_3	P4	I/O
3	IO_L29P_3	P3	I/O
3	IO_L30N_3	R3	I/O
3	IO_L30P_3	R2	I/O
3	IO_L32N_3	T2	I/O
3	IO_L32P_3/VREF_3	T1	VREF
3	IO_L33N_3	R4	I/O
3	IO_L33P_3	T3	I/O
3	IO_L34N_3	U3	I/O

Table 76: **Spartan-3AN FGG400 Pinout *(Cont'd)***

Bank	Pin Name	FGG400 Ball	Type
3	IO_L34P_3	U1	I/O
3	IO_L36N_3	T4	I/O
3	IO_L36P_3	R5	I/O
3	IO_L37N_3	V2	I/O
3	IO_L37P_3	V1	I/O
3	IO_L38N_3	W2	I/O
3	IO_L38P_3	W1	I/O
3	IP_3	H7	INPUT
3	IP_L04N_3/VREF_3	G6	VREF
3	IP_L04P_3	G7	INPUT
3	IP_L11N_3/VREF_3	J7	VREF
3	IP_L11P_3	J8	INPUT
3	IP_L15N_3	K7	INPUT
3	IP_L15P_3	K8	INPUT
3	IP_L19N_3	K5	INPUT
3	IP_L19P_3	K6	INPUT
3	IP_L23N_3	L6	INPUT
3	IP_L23P_3	L7	INPUT
3	IP_L27N_3	M7	INPUT
3	IP_L27P_3	M8	INPUT
3	IP_L31N_3	N7	INPUT
3	IP_L31P_3	M6	INPUT
3	IP_L35N_3	N6	INPUT
3	IP_L35P_3	P5	INPUT
3	IP_L39N_3/VREF_3	P7	VREF
3	IP_L39P_3	P6	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	N5	VCCO
3	VCCO_3	U2	VCCO
GND	GND	A1	GND
GND	GND	A11	GND
GND	GND	A20	GND
GND	GND	B6	GND
GND	GND	B14	GND
GND	GND	C3	GND
GND	GND	C18	GND
GND	GND	D9	GND
GND	GND	E5	GND

Table 76: **Spartan-3AN FGG400 Pinout *(Cont'd)***

Bank	Pin Name	FGG400 Ball	Type
GND	GND	E12	GND
GND	GND	F15	GND
GND	GND	G2	GND
GND	GND	G19	GND
GND	GND	H8	GND
GND	GND	H13	GND
GND	GND	J9	GND
GND	GND	J11	GND
GND	GND	K1	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	K17	GND
GND	GND	L4	GND
GND	GND	L9	GND
GND	GND	L11	GND
GND	GND	L20	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P2	GND
GND	GND	P19	GND
GND	GND	R6	GND
GND	GND	R9	GND
GND	GND	T16	GND
GND	GND	U12	GND
GND	GND	V3	GND
GND	GND	V18	GND
GND	GND	W7	GND
GND	GND	W15	GND
GND	GND	Y1	GND
GND	GND	Y10	GND
GND	GND	Y20	GND
VCCAUX	SUSPEND	R15	PWR MGMT
VCCAUX	DONE	W19	CONFIG
VCCAUX	PROG_B	D5	CONFIG
VCCAUX	TCK	A19	JTAG
VCCAUX	TDI	F5	JTAG
VCCAUX	TDO	E17	JTAG

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
1	IO_L25N_1/RHCLK7	K19	RHCLK
1	IO_L25P_1/IRDY1/RHCLK6	K20	RHCLK
1	IO_L26N_1/A11	J22	DUAL
1	IO_L26P_1/A10	K22	DUAL
1	IO_L28N_1	L19	I/O
1	IO_L28P_1	L18	I/O
1	IO_L29N_1/A13	J20	DUAL
1	IO_L29P_1/A12	J21	DUAL
1	IO_L30N_1/A15	G22	DUAL
1	IO_L30P_1/A14	H22	DUAL
1	IO_L32N_1	K18	I/O
1	IO_L32P_1	K17	I/O
1	IO_L33N_1/A17	H20	DUAL
1	IO_L33P_1/A16	H21	DUAL
1	IO_L34N_1/A19	F21	DUAL
1	IO_L34P_1/A18	F22	DUAL
1	IO_L36N_1	G20	I/O
1	IO_L36P_1	G19	I/O
1	IO_L37N_1	H19	I/O
1	IO_L37P_1	J18	I/O
1	IO_L38N_1	F20	I/O
1	IO_L38P_1	E20	I/O
1	IO_L40N_1	F18	I/O
1	IO_L40P_1	F19	I/O
1	IO_L41N_1	D22	I/O
1	IO_L41P_1	E22	I/O
1	IO_L42N_1	D20	I/O
1	IO_L42P_1	D21	I/O
1	IO_L44N_1/A21	C21	DUAL
1	IO_L44P_1/A20	C22	DUAL
1	IO_L45N_1/A23	B21	DUAL
1	IO_L45P_1/A22	B22	DUAL
1	IO_L46N_1/A25	G17	DUAL
1	IO_L46P_1/A24	G18	DUAL
1	IP_L04N_1/VREF_1	R16	VREF
1	IP_L04P_1	R15	INPUT
1	IP_L08N_1	P16	INPUT
1	IP_L08P_1	P15	INPUT
1	IP_L12N_1/VREF_1	R18	VREF
1	IP_L12P_1	R17	INPUT

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
1	IP_L16N_1/VREF_1	N16	VREF
1	IP_L16P_1	N15	INPUT
1	IP_L23N_1	M16	INPUT
1	IP_L23P_1	M17	INPUT
1	IP_L27N_1	L16	INPUT
1	IP_L27P_1/VREF_1	M15	VREF
1	IP_L31N_1	K16	INPUT
1	IP_L31P_1	L15	INPUT
1	IP_L35N_1	K15	INPUT
1	IP_L35P_1/VREF_1	K14	VREF
1	IP_L39N_1	H18	INPUT
1	IP_L39P_1	H17	INPUT
1	IP_L43N_1/VREF_1	J15	VREF
1	IP_L43P_1	J16	INPUT
1	IP_L47N_1	H15	INPUT
1	IP_L47P_1/VREF_1	H16	VREF
1	VCCO_1	E21	VCCO
1	VCCO_1	J17	VCCO
1	VCCO_1	K21	VCCO
1	VCCO_1	P17	VCCO
1	VCCO_1	P21	VCCO
1	VCCO_1	V21	VCCO
2	IO_L01N_2/M0	W5	DUAL
2	IO_L01P_2/M1	V6	DUAL
2	IO_L02N_2/CSO_B	Y4	DUAL
2	IO_L02P_2/M2	W4	DUAL
2	IO_L03N_2	AA3	I/O
2	IO_L03P_2	AB2	I/O
2	IO_L04N_2	AA4	I/O
2	IO_L04P_2	AB3	I/O
2	IO_L05N_2	Y5	I/O
2	IO_L05P_2	W6	I/O
2	IO_L06N_2	AB5	I/O
2	IO_L06P_2	AB4	I/O
2	IO_L07N_2	Y6	I/O
2	IO_L07P_2	W7	I/O
2	IO_L08N_2	AB6	I/O
2	IO_L08P_2	AA6	I/O
2	IO_L09N_2/VS2	W9	DUAL
2	IO_L09P_2/RDWR_B	V9	DUAL

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
3	IP_L04N_3/VREF_3	H7	VREF
3	IP_L04P_3	H8	INPUT
3	IP_L11N_3	K8	INPUT
3	IP_L11P_3	J7	INPUT
3	IP_L15N_3/VREF_3	L8	VREF
3	IP_L15P_3	K7	INPUT
3	IP_L19N_3	M8	INPUT
3	IP_L19P_3	L7	INPUT
3	IP_L23N_3	M6	INPUT
3	IP_L23P_3	M7	INPUT
3	IP_L27N_3	N9	INPUT
3	IP_L27P_3	N8	INPUT
3	IP_L31N_3	N5	INPUT
3	IP_L31P_3	N6	INPUT
3	IP_L35N_3	P8	INPUT
3	IP_L35P_3	N7	INPUT
3	IP_L39N_3	R8	INPUT
3	IP_L39P_3	P7	INPUT
3	IP_L46N_3/VREF_3	T6	VREF
3	IP_L46P_3	R7	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J6	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P6	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA7	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	B7	GND
GND	GND	C20	GND
GND	GND	C3	GND
GND	GND	D14	GND
GND	GND	D9	GND

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
GND	GND	F11	GND
GND	GND	F17	GND
GND	GND	F6	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L17	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P10	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	T12	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U17	GND
GND	GND	U6	GND
GND	GND	W10	GND
GND	GND	W14	GND
GND	GND	Y20	GND
GND	GND	Y3	GND
VCCAUX	SUSPEND	U18	PWR MGMT

FGG676: 676-Ball Fine-Pitch Ball Grid Array

The 676-ball fine-pitch ball grid array, FGG676, supports the XC3S1400AN FPGA.

Table 82 lists all the FGG676 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type (as defined in Table 62).

The XC3S1400AN has 17 unconnected balls, indicated as N.C. in Table 82 and Figure 24.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 82: **Spartan-3AN FGG676 Pinout**

Bank	Pin Name	FGG676 Ball	Type
0	IO_L01N_0	F20	I/O
0	IO_L01P_0	G20	I/O
0	IO_L02N_0	F19	I/O
0	IO_L02P_0/VREF_0	G19	VREF
0	IO_L05N_0	C22	I/O
0	IO_L05P_0	D22	I/O
0	IO_L06N_0	C23	I/O
0	IO_L06P_0	D23	I/O
0	IO_L07N_0	A22	I/O
0	IO_L07P_0	B23	I/O
0	IO_L08N_0	G17	I/O
0	IO_L08P_0	H17	I/O
0	IO_L09N_0	B21	I/O
0	IO_L09P_0	C21	I/O
0	IO_L10N_0	D21	I/O
0	IO_L10P_0	E21	I/O
0	IO_L11N_0	C20	I/O
0	IO_L11P_0	D20	I/O
0	IO_L12N_0	K16	I/O
0	IO_L12P_0	J16	I/O
0	IO_L13N_0	E17	I/O
0	IO_L13P_0	F17	I/O
0	IO_L14N_0	A20	I/O
0	IO_L14P_0/VREF_0	B20	VREF
0	IO_L15N_0	A19	I/O
0	IO_L15P_0	B19	I/O
0	IO_L16N_0	H15	I/O
0	IO_L16P_0	G15	I/O
0	IO_L17N_0	C18	I/O
0	IO_L17P_0	D18	I/O

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
0	IO_L18N_0	A18	I/O
0	IO_L18P_0	B18	I/O
0	IO_L19N_0	B17	I/O
0	IO_L19P_0	C17	I/O
0	IO_L20N_0/VREF_0	E15	VREF
0	IO_L20P_0	F15	I/O
0	IO_L21N_0	C16	I/O
0	IO_L21P_0	D17	I/O
0	IO_L22N_0	C15	I/O
0	IO_L22P_0	D16	I/O
0	IO_L23N_0	A15	I/O
0	IO_L23P_0	B15	I/O
0	IO_L24N_0	F14	I/O
0	IO_L24P_0	E14	I/O
0	IO_L25N_0/GCLK5	J14	GCLK
0	IO_L25P_0/GCLK4	K14	GCLK
0	IO_L26N_0/GCLK7	A14	GCLK
0	IO_L26P_0/GCLK6	B14	GCLK
0	IO_L27N_0/GCLK9	G13	GCLK
0	IO_L27P_0/GCLK8	F13	GCLK
0	IO_L28N_0/GCLK11	C13	GCLK
0	IO_L28P_0/GCLK10	B13	GCLK
0	IO_L29N_0	B12	I/O
0	IO_L29P_0	A12	I/O
0	IO_L30N_0	C12	I/O
0	IO_L30P_0	D13	I/O
0	IO_L31N_0	F12	I/O
0	IO_L31P_0	E12	I/O
0	IO_L32N_0/VREF_0	D11	VREF
0	IO_L32P_0	C11	I/O

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
1	IO_L51P_1	G23	I/O
1	IO_L53N_1	K20	I/O
1	IO_L53P_1	L20	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L56N_1	F23	I/O
1	IO_L56P_1	E24	I/O
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L58N_1	G22	I/O
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L59N_1	J20	I/O
1	IO_L59P_1	J19	I/O
1	IO_L60N_1	D26	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L62N_1/A21	H21	DUAL
1	IO_L62P_1/A20	J21	DUAL
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IO_L64N_1/A25	G21	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IP_L16N_1	Y26	INPUT
1	IP_L16P_1	W25	INPUT
1	IP_L20N_1/VREF_1	V26	VREF
1	IP_L20P_1	W26	INPUT
1	IP_L24N_1/VREF_1	U26	VREF
1	IP_L24P_1	U25	INPUT
1	IP_L28N_1	R24	INPUT
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT
1	IP_L36N_1	N23	INPUT
1	IP_L36P_1/VREF_1	M24	VREF
1	IP_L40N_1	L23	INPUT
1	IP_L40P_1	K24	INPUT
1	IP_L44N_1	H25	INPUT

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
1	IP_L44P_1/VREF_1	H26	VREF
1	IP_L48N_1	H24	INPUT
1	IP_L48P_1	H23	INPUT
1	IP_L52N_1/VREF_1	G25	VREF
1	IP_L52P_1	G26	INPUT
1	IP_L65N_1	B25	INPUT
1	IP_L65P_1/VREF_1	B26	VREF
1	VCCO_1	AB25	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	W22	VCCO
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O
2	IO_L05P_2	W9	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L08N_2	AD6	I/O
2	IO_L08P_2	AC6	I/O
2	IO_L09N_2	W10	I/O
2	IO_L09P_2	V10	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L10P_2	AF5	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L11P_2	AD7	I/O
2	IO_L12N_2	AA10	I/O
2	IO_L12P_2	Y10	I/O
2	IO_L13N_2	U11	I/O
2	IO_L13P_2	V11	I/O
2	IO_L14N_2	AB7	I/O
2	IO_L14P_2	AC8	I/O