AMD Xilinx - XC3S400AN-5FTG256C Datasheet

Welcome to **E-XFL.COM**

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	368640
Number of I/O	195
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s400an-5ftg256c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Related Product Families

The Spartan-3AN FPGA family is generally compatible with the Spartan-3A FPGA family.

- **DS529: Spartan-3A FPGA Family Data Sheet**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device.
09/12/07	2.0.1	Minor updates to text.
09/24/07	2.1	Added note that In-System Flash commands were not supported by simulation until ISE 10.1 software.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that SPI_ACCESS simulation is supported in ISE 10.1 software. Updated links.
06/02/08	3.1	Minor updates.
11/19/09	3.2	In the Spartan-3AN FPGA Design Documentation section, added link to DS706, *Extended Spartan-3A Family Overview* and removed references to older software versions.
12/02/10	4.0	Updated link to sign up for Alerts and updated Notice of Disclaimer.
04/01/11	4.1	Added the FT(G)256 package selection for the XC3S50AN and XC3S400AN devices and the FG(G)484 package selection for the XC3S1400AN device throughout this data sheet.

Notice of Disclaimer

THE XILINX HARDWARE FPGA AND CPLD DEVICES REFERRED TO HEREIN ("PRODUCTS") ARE SUBJECT TO THE TERMS AND CONDITIONS OF THE XILINX LIMITED WARRANTY WHICH CAN BE VIEWED AT http://www.xilinx.com/warranty.htm. THIS LIMITED WARRANTY DOES NOT EXTEND TO ANY USE OF PRODUCTS IN AN APPLICATION OR ENVIRONMENT THAT IS NOT WITHIN THE SPECIFICATIONS STATED IN THE XILINX DATA SHEET. ALL SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE. PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, OR ANY OTHER APPLICATION THAT INVOKES THE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). USE OF PRODUCTS IN CRITICAL APPLICATIONS IS AT THE SOLE RISK OF CUSTOMER, SUBJECT TO APPLICABLE LAWS AND REGULATIONS.

CRITICAL APPLICATIONS DISCLAIMER

XILINX PRODUCTS (INCLUDING HARDWARE, SOFTWARE AND/OR IP CORES) ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS IN LIFE-SUPPORT OR SAFETY DEVICES OR SYSTEMS, CLASS III MEDICAL DEVICES, NUCLEAR FACILITIES, APPLICATIONS RELATED TO THE DEPLOYMENT OF AIRBAGS, OR ANY OTHER APPLICATIONS THAT COULD LEAD TO DEATH, PERSONAL INJURY OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE (INDIVIDUALLY AND COLLECTIVELY, "CRITICAL APPLICATIONS"). FURTHERMORE, XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED FOR USE IN ANY APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE OR AIRCRAFT, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR. CUSTOMER AGREES, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE XILINX PRODUCTS, TO THOROUGHLY TEST THE SAME FOR SAFETY PURPOSES. TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN CRITICAL APPLICATIONS.

AUTOMOTIVE APPLICATIONS DISCLAIMER

XILINX PRODUCTS ARE NOT DESIGNED OR INTENDED TO BE FAIL-SAFE, OR FOR USE IN ANY APPLICATION REQUIRING FAIL-SAFE PERFORMANCE, SUCH AS APPLICATIONS RELATED TO: (I) THE DEPLOYMENT OF AIRBAGS, (II) CONTROL OF A VEHICLE, UNLESS THERE IS A FAIL-SAFE OR REDUNDANCY FEATURE (WHICH DOES NOT INCLUDE USE OF SOFTWARE IN THE XILINX DEVICE TO IMPLEMENT THE REDUNDANCY) AND A WARNING SIGNAL UPON FAILURE TO THE OPERATOR, OR (III) USES THAT COULD LEAD TO DEATH OR PERSONAL INJURY. CUSTOMER ASSUMES THE SOLE RISK AND LIABILITY OF ANY USE OF XILINX PRODUCTS IN SUCH APPLICATIONS.

Spartan-3AN FPGA Family: DC and Switching Characteristics

DS557 (v4.1) April 1, 2011

Product Specification

DC Electrical Characteristics

In this section, specifications can be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3AN devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 6: Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 6: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	$V_{CCO} + 0.5$	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$–0.5V < V_{IN} < (V_{CCO} + 0.5V)$[1]	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
1. For soldering guidelines, see UG112: Device Package User Guide and XAPP427: Implementation and Solder Reflow Guidelines for Pb-Free Packages.

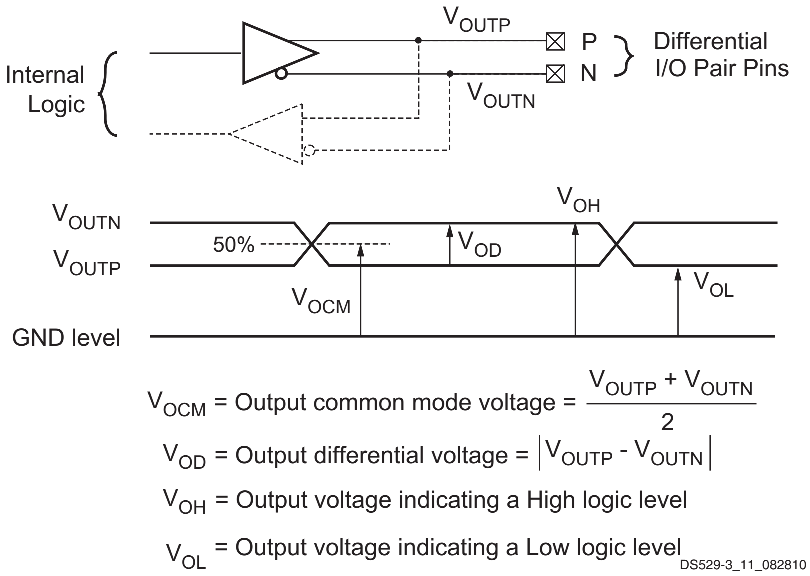
Table 15: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards *(Cont'd)***

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}[2]		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
DIFF_SSTL3_II[8]	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the "Using I/O Resources" chapter in UG331.
4. See External Termination Requirements for Differential I/O, page 22.
5. LVPECL is supported on inputs only, not outputs. Requires $V_{CCAUX} = 3.3V \pm 10\%$.
6. LVPECL_33 maximum $V_{ICM} = V_{CCAUX} - (V_{ID} / 2)$
7. Requires $V_{CCAUX} = 3.3V \pm 10\%$ for inputs. $(V_{CCAUX} - 300\ mV) \leq V_{ICM} \leq (V_{CCAUX} - 37\ mV)$
8. V_{REF} inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The V_{REF} settings are the same as for the single-ended versions in Table 13. Other differential standards do not use V_{REF}.
9. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the "Using I/O Resources" chapter in UG331.

Differential Output Pairs



$$V_{OCM} = \text{Output common mode voltage} = \frac{V_{OUTP} + V_{OUTN}}{2}$$

$$V_{OD} = \text{Output differential voltage} = \left| V_{OUTP} - V_{OUTN} \right|$$

$$V_{OH} = \text{Output voltage indicating a High logic level}$$

$$V_{OL} = \text{Output voltage indicating a Low logic level}$$

Figure 7: **Differential Output Voltages**

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

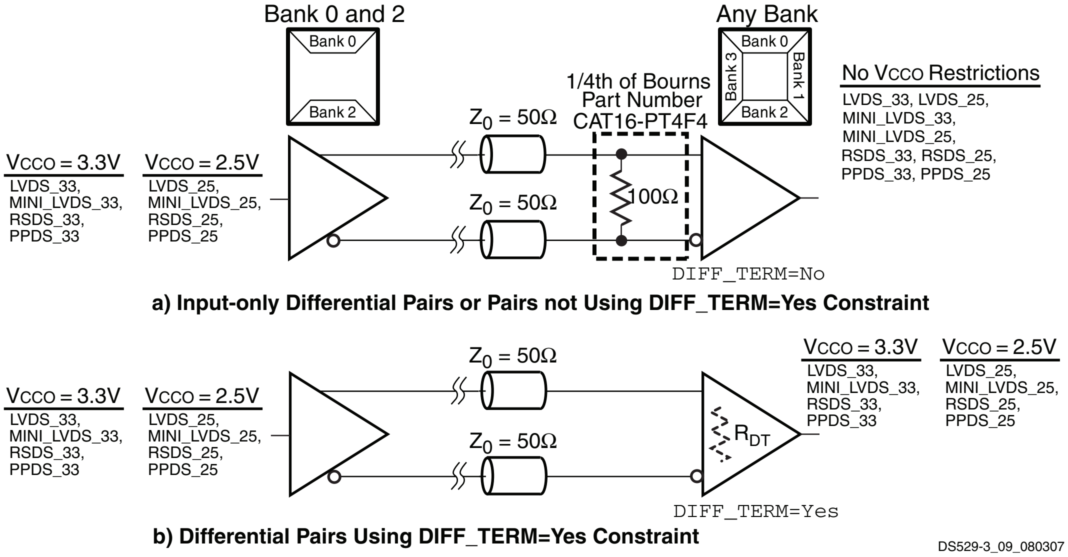


Figure 8: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

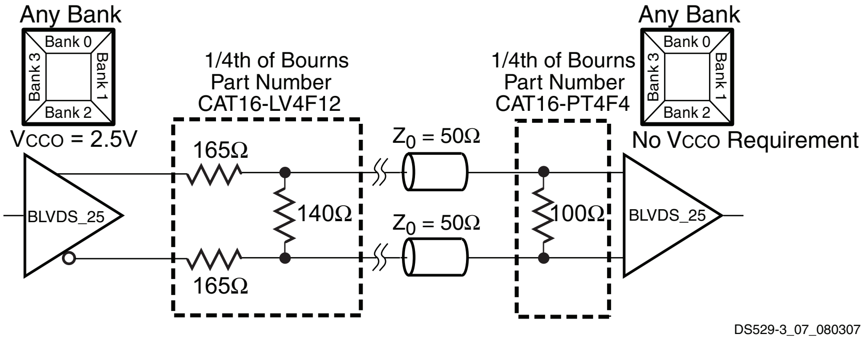


Figure 9: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

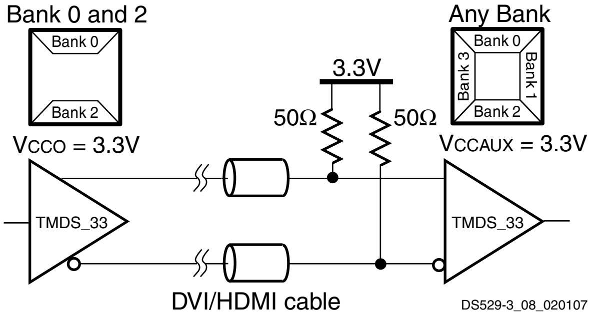


Figure 10: **External Input Resistors Required for TMDS_33 I/O Standard**

I/O Timing

Pin-to-Pin Clock-to-Output Times

Table 21: **Pin-to-Pin Clock-to-Output Times for the IOB Output Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Clock-to-Output Times						
$T_{ICKOFDCM}$	When reading from the Output Flip-Flop (OFF), the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, with DCM(3)	XC3S50AN	3.18	3.42	ns
			XC3S200AN	3.21	3.27	ns
			XC3S400AN	2.97	3.33	ns
			XC3S700AN	3.39	3.50	ns
			XC3S1400AN	3.51	3.99	ns
T_{ICKOF}	When reading from OFF, the time from the active transition on the Global Clock pin to data appearing at the Output pin. The DCM is not in use.	LVCMOS25(2), 12 mA output drive, Fast slew rate, without DCM	XC3S50AN	4.59	5.02	ns
			XC3S200AN	4.88	5.24	ns
			XC3S400AN	4.68	5.12	ns
			XC3S700AN	4.97	5.34	ns
			XC3S1400AN	5.06	5.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This clock-to-output time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or a standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. If the former is true, *add* the appropriate Input adjustment from Table 26. If the latter is true, *add* the appropriate Output adjustment from Table 29.
3. DCM output jitter is included in all measurements.

Three-State Output Propagation Times

Table 28: **Timing for the IOB Three-State Path**

Symbol	Description	Conditions	Device	Speed Grade -5 Max	Speed Grade -4 Max	Units
Synchronous Output Enable/Disable Times						
T_{IOCKHZ}	Time from the active transition at the OTCLK input of the Three-state Flip-Flop (TFF) to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	0.63	0.76	ns
T_{IOCKON}(2)	Time from the active transition at TFF's OTCLK input to when the Output pin drives valid data		All	2.80	3.06	ns
Asynchronous Output Enable/Disable Times						
T_{GTS}	Time from asserting the Global Three State (GTS) input on the STARTUP_SPARTAN3A primitive to when the Output pin enters the high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	9.47	10.36	ns
Set/Reset Times						
T_{IOSRHZ}	Time from asserting TFF's SR input to when the Output pin enters a high-impedance state	LVCMOS25, 12 mA output drive, Fast slew rate	All	1.61	1.86	ns
T_{IOSRON}(2)	Time from asserting TFF's SR input at TFF to when the Output pin drives valid data		All	3.57	3.82	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This time requires adjustment whenever a signal standard other than LVCMOS25 with 12 mA drive and Fast slew rate is assigned to the data Output. When this is true, *add* the appropriate Output adjustment from Table 29.

Table 29: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26(3)	2.26(3)	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns

Table 29: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns

Suspend Mode Timing

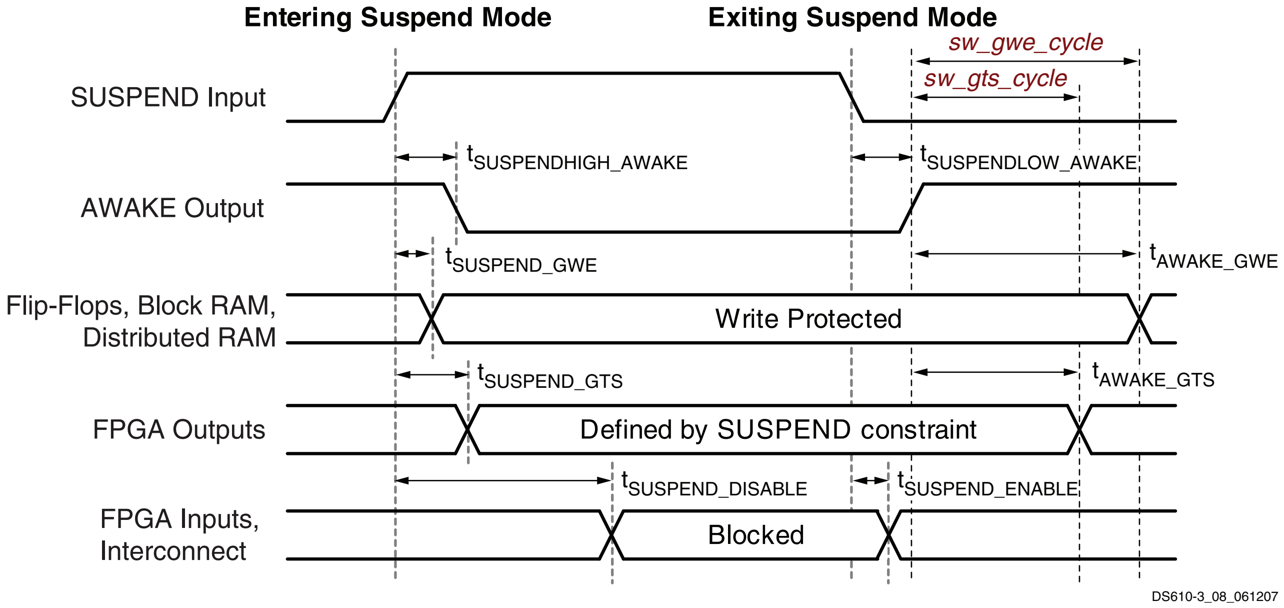


Figure 12: **Suspend Mode Timing**

Table 49: **Suspend Mode Timing Parameters**

Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***)	–	7	–	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***)	+160	+300	+600	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	< 5	–	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–	ns
Exiting Suspend Mode					
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin Does not include DCM lock time	–	4 to 108	–	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1***	–	67	–	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512***	–	14	–	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1***	–	57	–	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512***	–	14	–	µs

Notes:

1. These parameters based on characterization.
2. For information on using the Spartan-3AN Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

Configuration Clock (CCLK) Characteristics

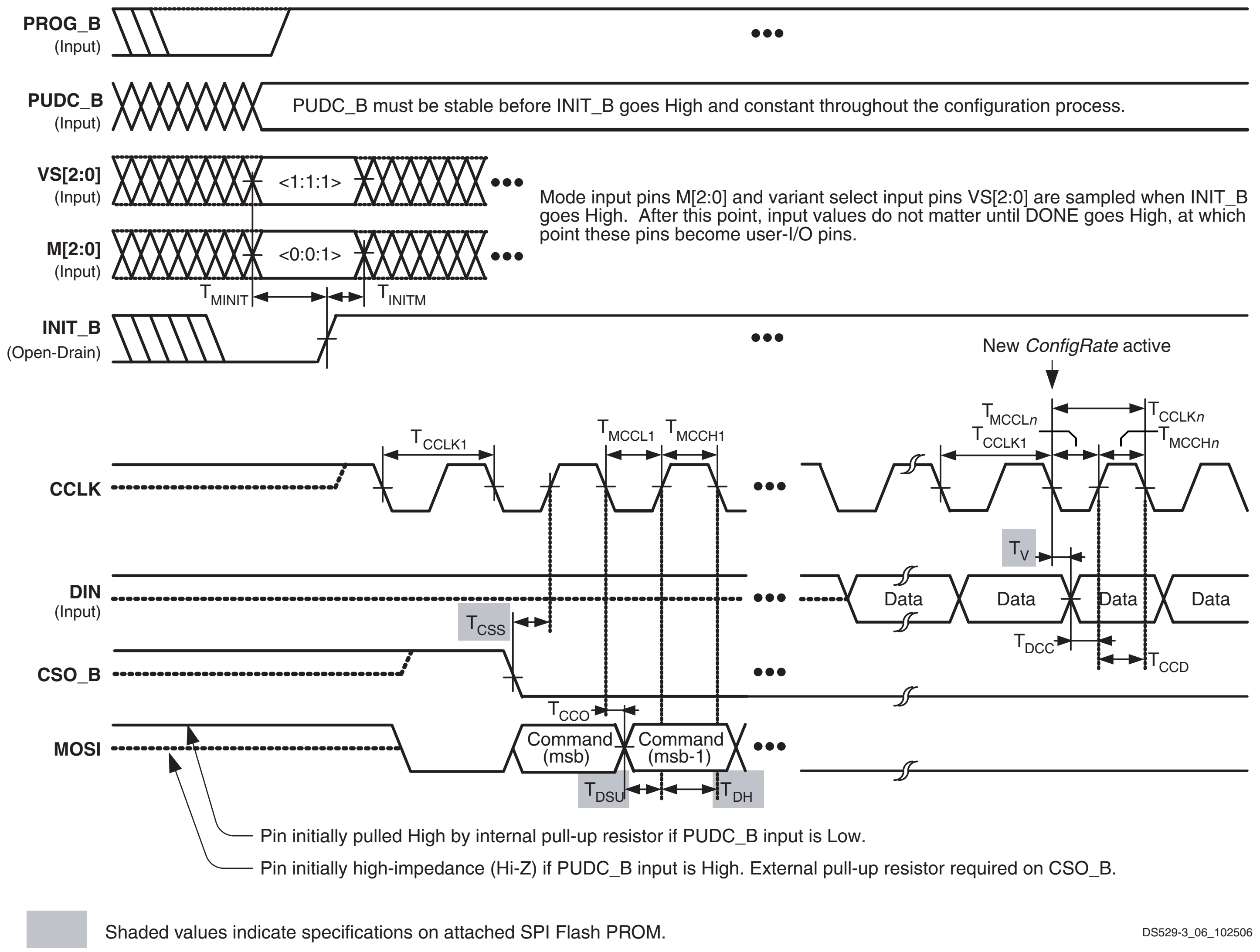
Table 51: **Master Mode CCLK Output Period by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting(1)	Temperature Range	Minimum	Maximum	Units
T_{CCLK1}	CCLK clock period by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	1,254	2,500	ns
			Industrial	1,180		ns
T_{CCLK3}		3	Commercial	413	833	ns
			Industrial	390		ns
T_{CCLK6}		6 (*default*)	Commercial	207	417	ns
			Industrial	195		ns
T_{CCLK7}		7	Commercial	178	357	ns
			Industrial	168		ns
T_{CCLK8}		8	Commercial	156	313	ns
			Industrial	147		ns
T_{CCLK10}		10	Commercial	123	250	ns
			Industrial	116		ns
T_{CCLK12}		12	Commercial	103	208	ns
			Industrial	97		ns
T_{CCLK13}		13	Commercial	93	192	ns
			Industrial	88		ns
T_{CCLK17}		17	Commercial	72	147	ns
			Industrial	68		ns
T_{CCLK22}		22	Commercial	54	114	ns
			Industrial	51		ns
T_{CCLK25}		25	Commercial	47	100	ns
			Industrial	45		ns
T_{CCLK27}		27	Commercial	44	93	ns
			Industrial	42		ns
T_{CCLK33}		33	Commercial	36	76	ns
			Industrial	34		ns
T_{CCLK44}		44	Commercial	26	57	ns
			Industrial	25		ns
T_{CCLK50}		50	Commercial	22	50	ns
			Industrial	21		ns
$T_{CCLK100}$		100	Commercial	11.2	25	ns
			Industrial	10.6		ns

Notes:

1. Set the ***ConfigRate*** option value when generating a configuration bitstream.

External Serial Peripheral Interface (SPI) Configuration Timing



PUDC_B must be stable before INIT_B goes High and constant throughout the configuration process.

Mode input pins M[2:0] and variant select input pins VS[2:0] are sampled when INIT_B goes High. After this point, input values do not matter until DONE goes High, at which point these pins become user-I/O pins.

Pin initially pulled High by internal pull-up resistor if PUDC_B input is Low.

Pin initially high-impedance (Hi-Z) if PUDC_B input is High. External pull-up resistor required on CSO_B.

▨ Shaded values indicate specifications on attached SPI Flash PROM.

Figure 16: **Waveforms for External Serial Peripheral Interface (SPI) Configuration**

Table 57: **Timing for External Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 51		
T_{CCLKn}	CCLK clock period after FPGA loads ***ConfigRate*** bitstream option setting	See Table 51		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling clock edge	See Table 55		
T_{DCC}	Setup time on the DIN data input before CCLK rising clock edge	See Table 55		
T_{CCD}	Hold time on the DIN data input after CCLK rising clock edge	See Table 55		

Table 58: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \le T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \le T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \le T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \le T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \ge \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

Byte Peripheral Interface (BPI) Configuration Timing

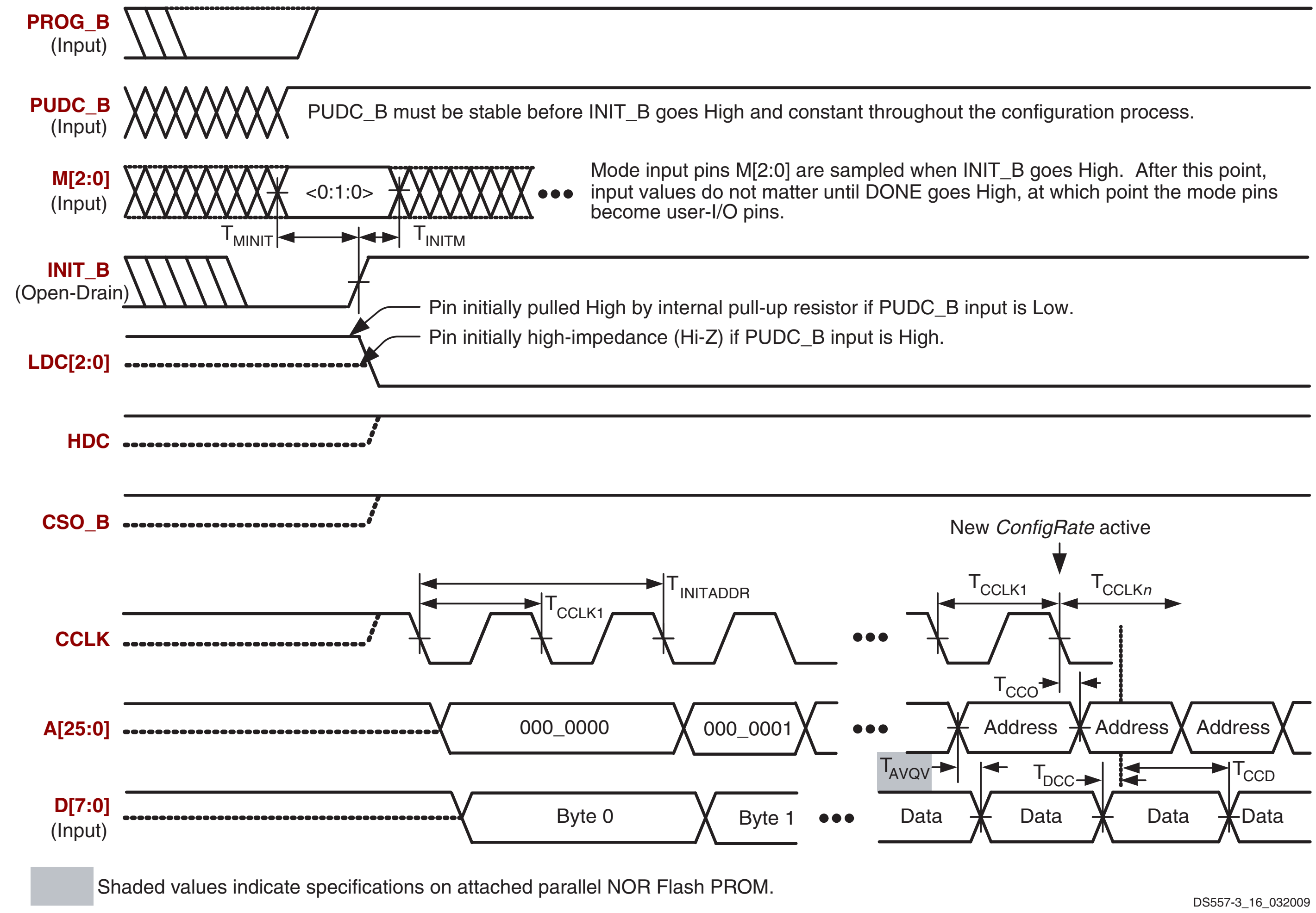


Figure 17: **Waveforms for Byte-wide Peripheral Interface (BPI) Configuration**

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device (XC3S200AN). Timing specifications updated for v1.38 speed files. DC specifications updated with production values. Other changes throughout.
08/31/07	2.0.1	Updated for Production release of XC3S1400AN. Improved t_{PEP} for XC3S700AN in Table 48.
09/12/07	2.0.2	Updated for Production release of XC3S700AN.
09/24/07	2.1	Updated for Production release of XC3S400AN. Updated Software Version Requirements to note that Production speed files are available as of Service Pack 3. Removed PCIX IOSTANDARD due to limited PCIX interface support. Added note that SPI_ACCESS (In-System Flash) is not currently supported in simulation.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that SPI_ACCESS simulation is supported in ISE 10.1 software. Removed DNA_RETENTION limit of 10 years in Table 17 since number of Read cycles is the only unique limit. Updated Setup, Hold, and Propagation Times for the IOB Input Path to show values by device in Table 23 and Table 25. Increased SSO recommendation for SSTL18_II in Table 32. Updated Figure 17 and Table 59 to show BPI data synchronous to CCLK rising edge. Updated links.
06/02/08	3.1	Improved V_{CCAUXT} and V_{CCO2T} POR minimum in Table 7 and updated V_{CCO} POR levels in Figure 13. Clarified power sequencing in Note 1 of Table 7, Table 8, and Figure 13. Added V_{IN} to Recommended Operating Conditions in Table 10 and added reference to XAPP459, "Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins." Reduced typical I_{CCINTQ} and I_{CCAUXQ} quiescent current values by 12%-58% in Table 12. Noted latest speed file v1.39 in ISE 10.1 software in Table 19. Added reference to Sample Window in Table 24. Changed Internal SPI interface max frequency to 50 MHz and updated other Internal SPI timing parameters to match names and values from speed file in Table 47. Restored Units column to Table 49. Updated CCLK output maximum period in Table 51 to match minimum frequency in Table 52. Added references to User Guides.
11/19/09	3.2	Updated selected I/O standard DC characteristics. Changed typical quiescent current temperature from ambient to junction. Removed references to older software versions. Updated column 3 header of Table 17 and Table 18. Added table note to Table 18. Added T_{IOPI} and T_{IOPID} propagation times in Table 25. Updated T_{IOCKHZ} and T_{IOCKON} synchronous output enable/disable times in Table 28. Removed V_{REF} requirements for differential HSTL and differential SSTL in Table 30. Improved DIFF_SSTL18_II SSO limits in Table 32. Updated table note 3 in Table 39. Removed references to old software versions from Table 47 and Table 48. Added description of spread spectrum in Spread Spectrum section. Updated BPI configuration waveforms in Figure 17. Updated T_{ACC} equation in Table 60.
12/02/10	4.0	Added I_{IK} to Table 6. Updated V_{IN} in Table 10 and added a footnote to I_L in Table 11 to note potential leakage between pins of a differential pair. Added note 6 to Table 13. Corrected CLK High and Low Time symbol in Table 46. Corrected symbols for $T_{SUSPEND\_GTS}$ and $T_{SUSPEND\_GWE}$ in Table 49. Updated link to sign up for Alerts and updated Notice of Disclaimer.
04/01/11	4.1	In Table 31, added the equivalent pairs per bank for the XC3S50AN and XC3S400AN in the FT(G)256 package and the XC3S1400AN in the FG(G)484 package.

FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FTG256, supports the XC3S50AN, XC3S200AN, and XC3S400AN devices. Table 70 lists all the package pins for these devices. They are sorted by bank number and then by the pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The differential I/O pairs that have different assignments between the XC3S50AN and the XC3S200AN or XC3S400AN are highlighted in light blue in Table 70. See Footprint Migration Differences, page 87 for additional information. The table also shows the pin number for each pin and the pin type (as defined in Table 62).

The footprints for the XC3S200AN and XC3S400AN in the FTG256 are identical. Figure 21 shows the common footprint for the XC3S200AN and XC3S400AN. The XC3S50AN footprint is compatible with the XC3S200AN and XC3S400AN, however, there are 51 unconnected balls (indicated as N.C. in Table 70).

Table 73 summarizes the XC3S50AN FPGA footprint migration differences for the FTG256 package.

The XC3S50AN does not support the address output pins for the byte-wide peripheral interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 70: **Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN)**

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
0	IO_L01N_0	IO_L01N_0	C13	I/O
0	IO_L01P_0	IO_L01P_0	D13	I/O
0	IO_L02N_0	IO_L02N_0	B14	I/O
0	IO_L02P_0/VREF_0	IO_L02P_0/VREF_0	B15	VREF
0	IO_L03N_0	IO_L03N_0	D11	I/O
0	IO_L03P_0	IO_L03P_0	C12	I/O
0	IO_L04N_0	IO_L04N_0	A13	I/O
0	IO_L04P_0	IO_L04P_0	A14	I/O
0	N.C.	IO_L05N_0	A12	I/O
0	IP_0	IO_L05P_0	B12	I/O
0	N.C.	IO_L06N_0/VREF_0	E10	VREF
0	N.C.	IO_L06P_0	D10	I/O
0	IO_L07N_0	IO_L07N_0	A11	I/O
0	IO_L07P_0	IO_L07P_0	C11	I/O
0	IO_L08N_0	IO_L08N_0	A10	I/O
0	IO_L08P_0	IO_L08P_0	B10	I/O
0	IO_L09N_0/GCLK5	IO_L09N_0/GCLK5	D9	GCLK
0	IO_L09P_0/GCLK4	IO_L09P_0/GCLK4	C10	GCLK
0	IO_L10N_0/GCLK7	IO_L10N_0/GCLK7	A9	GCLK
0	IO_L10P_0/GCLK6	IO_L10P_0/GCLK6	C9	GCLK
0	IO_L11N_0/GCLK9	IO_L11N_0/GCLK9	D8	GCLK
0	IO_L11P_0/GCLK8	IO_L11P_0/GCLK8	C8	GCLK
0	IO_L12N_0/GCLK11	IO_L12N_0/GCLK11	B8	GCLK
0	IO_L12P_0/GCLK10	IO_L12P_0/GCLK10	A8	GCLK
0	N.C.	IO_L13N_0	C7	I/O
0	N.C.	IO_L13P_0	A7	I/O

Table 76: **Spartan-3AN FGG400 Pinout *(Cont'd)***

Bank	Pin Name	FGG400 Ball	Type
1	IO_L38P_1/A24	B20	DUAL
1	IP_1/VREF_1	N14	VREF
1	IP_L04N_1/VREF_1	P15	VREF
1	IP_L04P_1	P14	INPUT
1	IP_L11N_1/VREF_1	M15	VREF
1	IP_L11P_1	M16	INPUT
1	IP_L15N_1	M13	INPUT
1	IP_L15P_1/VREF_1	M14	VREF
1	IP_L19N_1	L13	INPUT
1	IP_L19P_1	L14	INPUT
1	IP_L23N_1	K14	INPUT
1	IP_L23P_1/VREF_1	K15	VREF
1	IP_L27N_1	J15	INPUT
1	IP_L27P_1	J16	INPUT
1	IP_L31N_1	J13	INPUT
1	IP_L31P_1/VREF_1	J14	VREF
1	IP_L35N_1	H14	INPUT
1	IP_L35P_1	H15	INPUT
1	IP_L39N_1	G14	INPUT
1	IP_L39P_1/VREF_1	G15	VREF
1	VCCO_1	D19	VCCO
1	VCCO_1	H16	VCCO
1	VCCO_1	K19	VCCO
1	VCCO_1	N16	VCCO
1	VCCO_1	T19	VCCO
2	IO_L01N_2/M0	V4	DUAL
2	IO_L01P_2/M1	U4	DUAL
2	IO_L02N_2/CSO_B	Y2	DUAL
2	IO_L02P_2/M2	W3	DUAL
2	IO_L03N_2	W4	I/O
2	IO_L03P_2	Y3	I/O
2	IO_L04N_2	R7	I/O
2	IO_L04P_2	T6	I/O
2	IO_L05N_2	U5	I/O
2	IO_L05P_2	V5	I/O
2	IO_L06N_2	U6	I/O
2	IO_L06P_2	T7	I/O
2	IO_L07N_2/VS2	U7	DUAL
2	IO_L07P_2/RDWR_B	T8	DUAL
2	IO_L08N_2	Y5	I/O

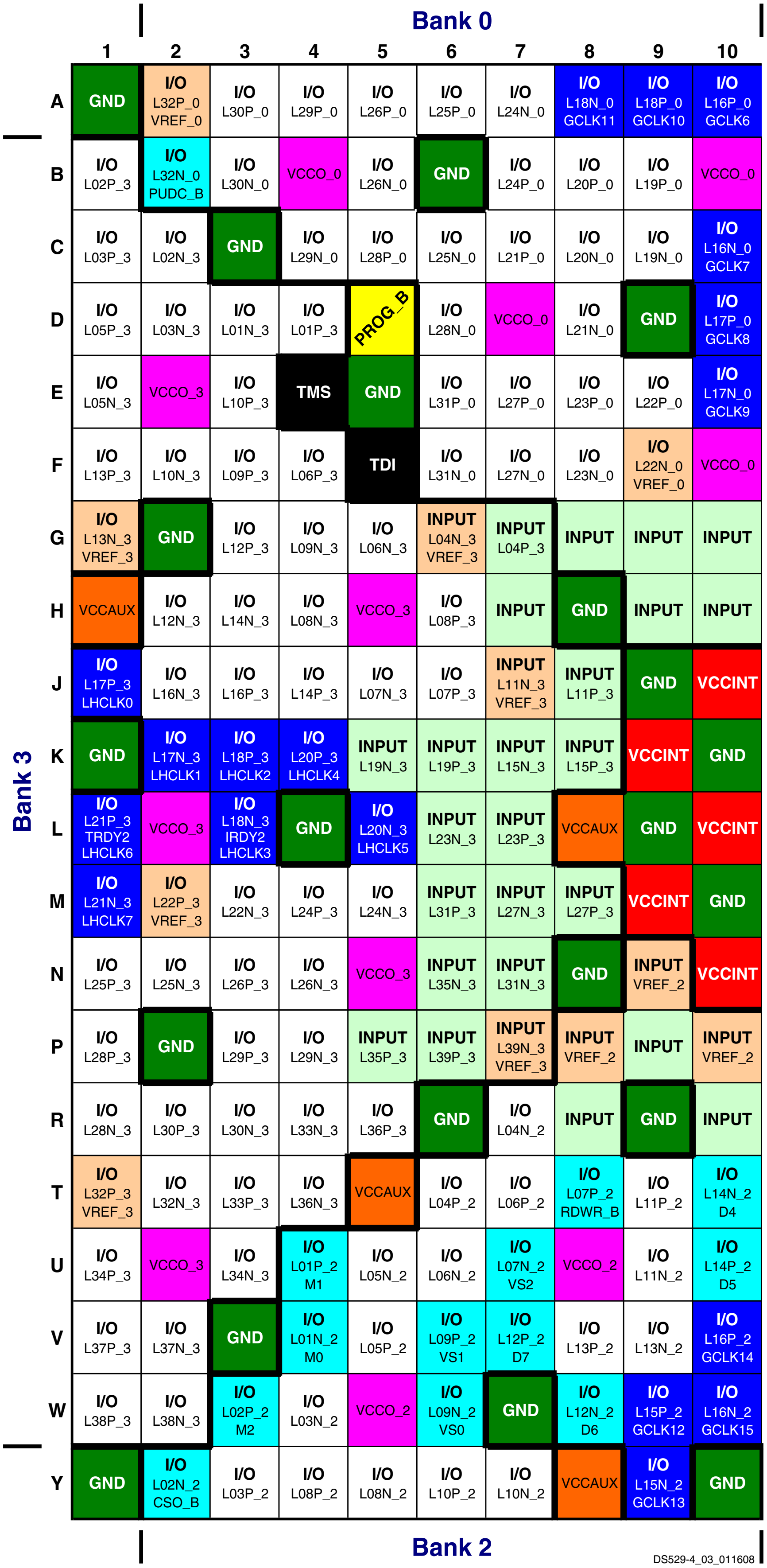
Table 76: **Spartan-3AN FGG400 Pinout *(Cont'd)***

Bank	Pin Name	FGG400 Ball	Type
2	IO_L08P_2	Y4	I/O
2	IO_L09N_2/VS0	W6	DUAL
2	IO_L09P_2/VS1	V6	DUAL
2	IO_L10N_2	Y7	I/O
2	IO_L10P_2	Y6	I/O
2	IO_L11N_2	U9	I/O
2	IO_L11P_2	T9	I/O
2	IO_L12N_2/D6	W8	DUAL
2	IO_L12P_2/D7	V7	DUAL
2	IO_L13N_2	V9	I/O
2	IO_L13P_2	V8	I/O
2	IO_L14N_2/D4	T10	DUAL
2	IO_L14P_2/D5	U10	DUAL
2	IO_L15N_2/GCLK13	Y9	GCLK
2	IO_L15P_2/GCLK12	W9	GCLK
2	IO_L16N_2/GCLK15	W10	GCLK
2	IO_L16P_2/GCLK14	V10	GCLK
2	IO_L17N_2/GCLK1	V11	GCLK
2	IO_L17P_2/GCLK0	Y11	GCLK
2	IO_L18N_2/GCLK3	V12	GCLK
2	IO_L18P_2/GCLK2	U11	GCLK
2	IO_L19N_2	R12	I/O
2	IO_L19P_2	T12	I/O
2	IO_L20N_2/MOSI/CSI_B	W12	DUAL
2	IO_L20P_2	Y12	I/O
2	IO_L21N_2	W13	I/O
2	IO_L21P_2	Y13	I/O
2	IO_L22N_2/DOUT	V13	DUAL
2	IO_L22P_2/AWAKE	U13	PWR MGMT
2	IO_L23N_2	R13	I/O
2	IO_L23P_2	T13	I/O
2	IO_L24N_2/D3	W14	DUAL
2	IO_L24P_2/INIT_B	Y14	DUAL
2	IO_L25N_2	T14	I/O
2	IO_L25P_2	V14	I/O
2	IO_L26N_2/D1	V15	DUAL
2	IO_L26P_2/D2	Y15	DUAL
2	IO_L27N_2	T15	I/O
2	IO_L27P_2	U15	I/O
2	IO_L28N_2	W16	I/O

FGG400 Footprint

Left Half of FGG400 Package (Top View)

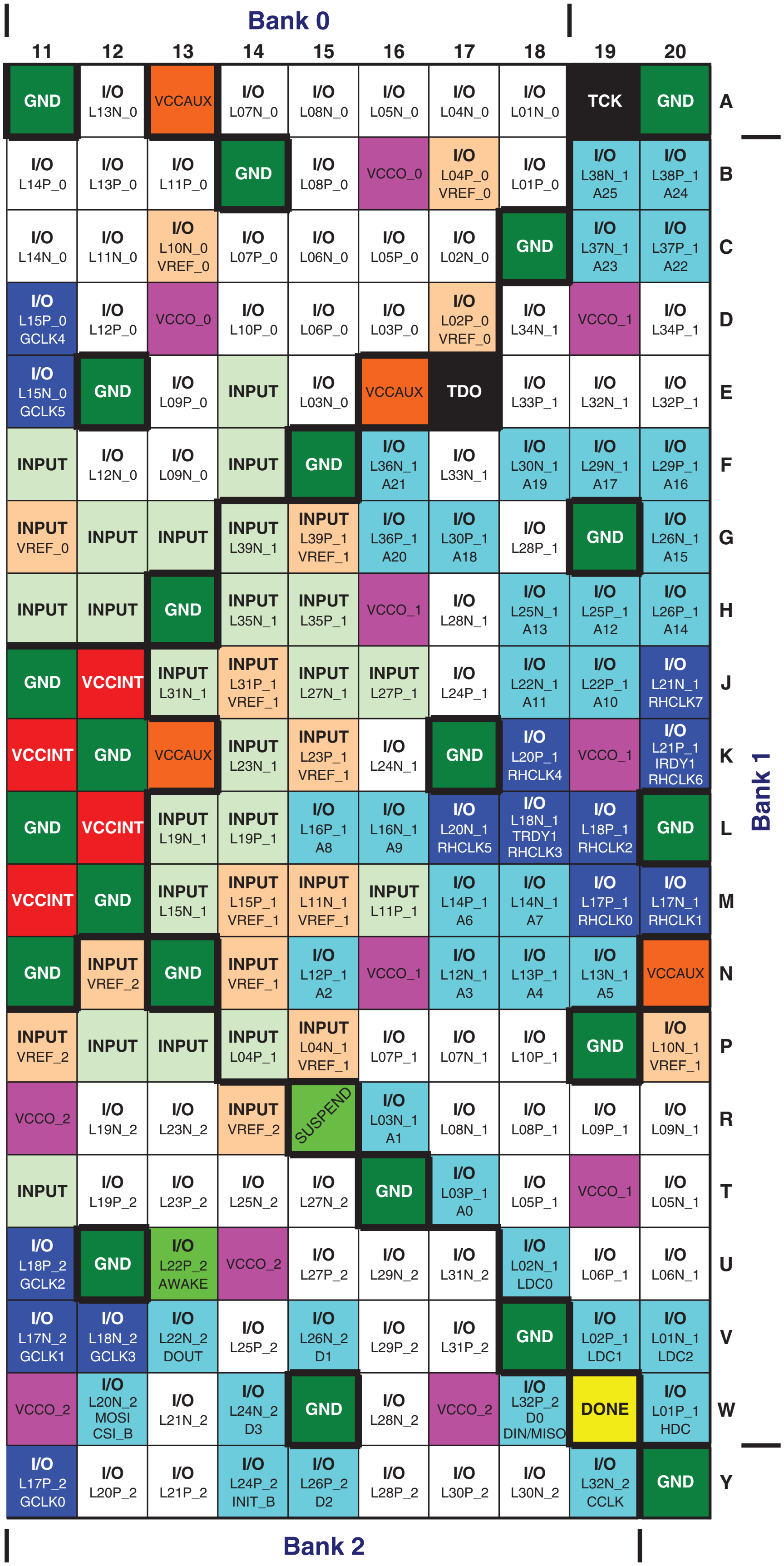
155	**I/O:** Unrestricted, general-purpose user I/O
46	**INPUT:** Unrestricted, general-purpose input pin
51	**DUAL:** Configuration pins, then possible user I/O
26	**VREF:** User I/O or input voltage reference for bank
32	**CLK:** User I/O, input, or clock buffer input
2	**CONFIG:** Dedicated configuration pins
4	**JTAG:** Dedicated JTAG port pins
2	**SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
43	**GND:** Ground
22	**VCCO:** Output voltage supply for bank
9	**VCCINT:** Internal core supply voltage (+1.2V)
8	**VCCAUX:** Auxiliary supply voltage



	1	2	3	4	5	6	7	8	9	10
A	GND	I/O L32P_0 VREF_0	I/O L30P_0	I/O L29P_0	I/O L26P_0	I/O L25P_0	I/O L24N_0	I/O L18N_0 GCLK11	I/O L18P_0 GCLK10	I/O L16P_0 GCLK6
B	I/O L02P_3	I/O L32N_0 PUDC_B	I/O L30N_0	VCCO_0	I/O L26N_0	GND	I/O L24P_0	I/O L20P_0	I/O L19P_0	VCCO_0
C	I/O L03P_3	I/O L02N_3	GND	I/O L29N_0	I/O L28P_0	I/O L25N_0	I/O L21P_0	I/O L20N_0	I/O L19N_0	I/O L16N_0 GCLK7
D	I/O L05P_3	I/O L03N_3	I/O L01N_3	I/O L01P_3	PROG_B	I/O L28N_0	VCCO_0	I/O L21N_0	GND	I/O L17P_0 GCLK8
E	I/O L05N_3	VCCO_3	I/O L10P_3	TMS	GND	I/O L31P_0	I/O L27P_0	I/O L23P_0	I/O L22P_0	I/O L17N_0 GCLK9
F	I/O L13P_3	I/O L10N_3	I/O L09P_3	I/O L06P_3	TDI	I/O L31N_0	I/O L27N_0	I/O L23N_0	I/O L22N_0 VREF_0	VCCO_0
G	I/O L13N_3 VREF_3	GND	I/O L12P_3	I/O L09N_3	I/O L06N_3	INPUT L04N_3 VREF_3	INPUT L04P_3	INPUT	INPUT	INPUT
H	VCCAUX	I/O L12N_3	I/O L14N_3	I/O L08N_3	VCCO_3	I/O L08P_3	INPUT	GND	INPUT	INPUT
J	I/O L17P_3 LHCLK0	I/O L16N_3	I/O L16P_3	I/O L14P_3	I/O L07N_3	I/O L07P_3	INPUT L11N_3 VREF_3	INPUT L11P_3	GND	VCCINT
K	GND	I/O L17N_3 LHCLK1	I/O L18P_3 LHCLK2	I/O L20P_3 LHCLK4	INPUT L19N_3	INPUT L19P_3	INPUT L15N_3	INPUT L15P_3	VCCINT	GND
L	I/O L21P_3 TRDY2 LHCLK6	VCCO_3	I/O L18N_3 IRDY2 LHCLK3	GND	I/O L20N_3 LHCLK5	INPUT L23N_3	INPUT L23P_3	VCCAUX	GND	VCCINT
M	I/O L21N_3 LHCLK7	I/O L22P_3 VREF_3	I/O L22N_3	I/O L24P_3	I/O L24N_3	INPUT L31P_3	INPUT L27N_3	INPUT L27P_3	VCCINT	GND
N	I/O L25P_3	I/O L25N_3	I/O L26P_3	I/O L26N_3	VCCO_3	INPUT L35N_3	INPUT L31N_3	GND	INPUT VREF_2	VCCINT
P	I/O L28P_3	GND	I/O L29P_3	I/O L29N_3	INPUT L35P_3	INPUT L39P_3	INPUT L39N_3 VREF_3	INPUT VREF_2	INPUT	INPUT VREF_2
R	I/O L28N_3	I/O L30P_3	I/O L30N_3	I/O L33N_3	I/O L36P_3	GND	I/O L04N_2	INPUT	GND	INPUT
T	I/O L32P_3 VREF_3	I/O L32N_3	I/O L33P_3	I/O L36N_3	VCCAUX	I/O L04P_2	I/O L06P_2	I/O L07P_2 RDWR_B	I/O L11P_2	I/O L14N_2 D4
U	I/O L34P_3	VCCO_3	I/O L34N_3	I/O L01P_2 M1	I/O L05N_2	I/O L06N_2	I/O L07N_2 VS2	VCCO_2	I/O L11N_2	I/O L14P_2 D5
V	I/O L37P_3	I/O L37N_3	GND	I/O L01N_2 M0	I/O L05P_2	I/O L09P_2 VS1	I/O L12P_2 D7	I/O L13P_2	I/O L13N_2	I/O L16P_2 GCLK14
W	I/O L38P_3	I/O L38N_3	I/O L02P_2 M2	I/O L03N_2	VCCO_2	I/O L09N_2 VS0	GND	I/O L12N_2 D6	I/O L15P_2 GCLK12	I/O L16N_2 GCLK15
Y	GND	I/O L02N_2 CSO_B	I/O L03P_2	I/O L08P_2	I/O L08N_2	I/O L10P_2	I/O L10N_2	VCCAUX	I/O L15N_2 GCLK13	GND

Figure 22: **FGG400 Package Footprint (Top View)**

Right Half of FGG400 Package (Top View)



	11	12	13	14	15	16	17	18	19	20
A	GND	I/O L13N_0	VCCAUX	I/O L07N_0	I/O L08N_0	I/O L05N_0	I/O L04N_0	I/O L01N_0	TCK	GND
B	I/O L14P_0	I/O L13P_0	I/O L11P_0	GND	I/O L08P_0	VCCO_0	I/O L04P_0 VREF_0	I/O L01P_0	I/O L38N_1 A25	I/O L38P_1 A24
C	I/O L14N_0	I/O L11N_0	I/O L10N_0 VREF_0	I/O L07P_0	I/O L06N_0	I/O L05P_0	I/O L02N_0	GND	I/O L37N_1 A23	I/O L37P_1 A22
D	I/O L15P_0 GCLK4	I/O L12P_0	VCCO_0	I/O L10P_0	I/O L06P_0	I/O L03P_0	I/O L02P_0 VREF_0	I/O L34N_1	VCCO_1	I/O L34P_1
E	I/O L15N_0 GCLK5	GND	I/O L09P_0	INPUT	I/O L03N_0	VCCAUX	TDO	I/O L33P_1	I/O L32N_1	I/O L32P_1
F	INPUT	I/O L12N_0	I/O L09N_0	INPUT	GND	I/O L36N_1 A21	I/O L33N_1	I/O L30N_1 A19	I/O L29N_1 A17	I/O L29P_1 A16
G	INPUT VREF_0	INPUT	INPUT	INPUT L39N_1	INPUT L39P_1 VREF_1	I/O L36P_1 A20	I/O L30P_1 A18	I/O L28P_1	GND	I/O L26N_1 A15
H	INPUT	INPUT	GND	INPUT L35N_1	INPUT L35P_1	VCCO_1	I/O L28N_1	I/O L25N_1 A13	I/O L25P_1 A12	I/O L26P_1 A14
J	GND	VCCINT	INPUT L31N_1	INPUT L31P_1 VREF_1	INPUT L27N_1	INPUT L27P_1	I/O L24P_1	I/O L22N_1 A11	I/O L22P_1 A10	I/O L21N_1 RHCLK7
K	VCCINT	GND	VCCAUX	INPUT L23N_1	INPUT L23P_1 VREF_1	I/O L24N_1	GND	I/O L20P_1 RHCLK4	VCCO_1	I/O L21P_1 IRDY1 RHCLK6
L	GND	VCCINT	INPUT L19N_1	INPUT L19P_1	I/O L16P_1 A8	I/O L16N_1 A9	I/O L20N_1 RHCLK5	I/O L18N_1 TRDY1 RHCLK3	I/O L18P_1 RHCLK2	GND
M	VCCINT	GND	INPUT L15N_1	INPUT L15P_1 VREF_1	INPUT L11N_1 VREF_1	INPUT L11P_1	I/O L14P_1 A6	I/O L14N_1 A7	I/O L17P_1 RHCLK0	I/O L17N_1 RHCLK1
N	GND	INPUT VREF_2	GND	INPUT VREF_1	I/O L12P_1 A2	VCCO_1	I/O L12N_1 A3	I/O L13P_1 A4	I/O L13N_1 A5	VCCAUX
P	INPUT VREF_2	INPUT	INPUT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L07P_1	I/O L07N_1	I/O L10P_1	GND	I/O L10N_1 VREF_1
R	VCCO_2	I/O L19N_2	I/O L23N_2	INPUT VREF_2	SUSPEND	I/O L03N_1 A1	I/O L08N_1	I/O L08P_1	I/O L09P_1	I/O L09N_1
T	INPUT	I/O L19P_2	I/O L23P_2	I/O L25N_2	I/O L27N_2	GND	I/O L03P_1 A0	I/O L05P_1	VCCO_1	I/O L05N_1
U	I/O L18P_2 GCLK2	GND	I/O L22P_2 AWAKE	VCCO_2	I/O L27P_2	I/O L29N_2	I/O L31N_2	I/O L02N_1 LDC0	I/O L06P_1	I/O L06N_1
V	I/O L17N_2 GCLK1	I/O L18N_2 GCLK3	I/O L22N_2 DOUT	I/O L25P_2	I/O L26N_2 D1	I/O L29P_2	I/O L31P_2	GND	I/O L02P_1 LDC1	I/O L01N_1 LDC2
W	VCCO_2	I/O L20N_2 MOSI CSI_B	I/O L21N_2	I/O L24N_2 D3	GND	I/O L28N_2	VCCO_2	I/O L32P_2 D0 DIN/MISO	DONE	I/O L01P_1 HDC
Y	I/O L17P_2 GCLK0	I/O L20P_2	I/O L21P_2	I/O L24P_2 INIT_B	I/O L26P_2 D2	I/O L28P_2	I/O L30P_2	I/O L30N_2	I/O L32N_2 CCLK	GND

DS557_4_22_030911

Figure 22: **FGG400 Package Footprint (Top View)**

FGG484: 484-Ball Fine-Pitch Ball Grid Array

The 484-ball fine-pitch ball grid array, FGG484, supports both the XC3S700AN and the XC3S1400AN FPGAs. There are three pinout differences, as described in Table 81.

Table 78 lists all the FGG484 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type (as defined in Table 62).

The shaded rows indicate pinout differences between the XC3S700AN and the XC3S1400AN FPGAs. The XC3S700AN has three unconnected balls, indicated as N.C. and with a black diamond (◆) in Table 78 and Figure 23.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 78: **Spartan-3AN FGG484 Pinout**

Bank	Pin Name	FGG484 Ball	Type
0	IO_L01N_0	D18	I/O
0	IO_L01P_0	E17	I/O
0	IO_L02N_0	C19	I/O
0	IO_L02P_0/VREF_0	D19	VREF
0	IO_L03N_0	A20	I/O
0	IO_L03P_0	B20	I/O
0	IO_L04N_0	F15	I/O
0	IO_L04P_0	E15	I/O
0	IO_L05N_0	A18	I/O
0	IO_L05P_0	C18	I/O
0	IO_L06N_0	A19	I/O
0	IO_L06P_0/VREF_0	B19	VREF
0	IO_L07N_0	C17	I/O
0	IO_L07P_0	D17	I/O
0	IO_L08N_0	C16	I/O
0	IO_L08P_0	D16	I/O
0	IO_L09N_0	E14	I/O
0	IO_L09P_0	C14	I/O
0	IO_L10N_0	A17	I/O
0	IO_L10P_0	B17	I/O
0	IO_L11N_0	C15	I/O
0	IO_L11P_0	D15	I/O
0	IO_L12N_0/VREF_0	A15	VREF
0	IO_L12P_0	A16	I/O
0	IO_L13N_0	A14	I/O
0	IO_L13P_0	B15	I/O
0	IO_L14N_0	E13	I/O
0	IO_L14P_0	F13	I/O
0	IO_L15N_0	C13	I/O
0	IO_L15P_0	D13	I/O
0	IO_L16N_0	A13	I/O
0	IO_L16P_0	B13	I/O
0	IO_L17N_0/GCLK5	E12	GCLK
0	IO_L17P_0/GCLK4	C12	GCLK
0	IO_L18N_0/GCLK7	A11	GCLK
0	IO_L18P_0/GCLK6	A12	GCLK
0	IO_L19N_0/GCLK9	C11	GCLK
0	IO_L19P_0/GCLK8	B11	GCLK
0	IO_L20N_0/GCLK11	E11	GCLK
0	IO_L20P_0/GCLK10	D11	GCLK
0	IO_L21N_0	C10	I/O
0	IO_L21P_0	A10	I/O
0	IO_L22N_0	A8	I/O
0	IO_L22P_0	A9	I/O
0	IO_L23N_0	E10	I/O
0	IO_L23P_0	D10	I/O
0	IO_L24N_0/VREF_0	C9	VREF
0	IO_L24P_0	B9	I/O
0	IO_L25N_0	C8	I/O
0	IO_L25P_0	B8	I/O
0	IO_L26N_0	A6	I/O
0	IO_L26P_0	A7	I/O
0	IO_L27N_0	C7	I/O
0	IO_L27P_0	D7	I/O
0	IO_L28N_0	A5	I/O
0	IO_L28P_0	B6	I/O

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
2	IO_L10N_2	AB7	I/O
2	IO_L10P_2	Y7	I/O
2	IO_L11N_2/VS0	Y8	DUAL
2	IO_L11P_2/VS1	W8	DUAL
2	IO_L12N_2	AB8	I/O
2	IO_L12P_2	AA8	I/O
2	IO_L13N_2	Y10	I/O
2	IO_L13P_2	V10	I/O
2	IO_L14N_2/D6	AB9	DUAL
2	IO_L14P_2/D7	Y9	DUAL
2	IO_L15N_2	AB10	I/O
2	IO_L15P_2	AA10	I/O
2	IO_L16N_2/D4	AB11	DUAL
2	IO_L16P_2/D5	Y11	DUAL
2	IO_L17N_2/GCLK13	V11	GCLK
2	IO_L17P_2/GCLK12	U11	GCLK
2	IO_L18N_2/GCLK15	Y12	GCLK
2	IO_L18P_2/GCLK14	W12	GCLK
2	IO_L19N_2/GCLK1	AB12	GCLK
2	IO_L19P_2/GCLK0	AA12	GCLK
2	IO_L20N_2/GCLK3	U12	GCLK
2	IO_L20P_2/GCLK2	V12	GCLK
2	IO_L21N_2	Y13	I/O
2	IO_L21P_2	AB13	I/O
2	IO_L22N_2/MOSI/CSI_B	AB14	DUAL
2	IO_L22P_2	AA14	I/O
2	IO_L23N_2	Y14	I/O
2	IO_L23P_2	W13	I/O
2	IO_L24N_2/DOUT	AA15	DUAL
2	IO_L24P_2/AWAKE	AB15	PWR MGMT
2	IO_L25N_2	Y15	I/O
2	IO_L25P_2	W15	I/O
2	IO_L26N_2/D3	U13	DUAL
2	IO_L26P_2/INIT_B	V13	DUAL
2	IO_L27N_2	Y16	I/O
2	IO_L27P_2	AB16	I/O
2	IO_L28N_2/D1	Y17	DUAL
2	IO_L28P_2/D2	AA17	DUAL
2	IO_L29N_2	AB18	I/O
2	IO_L29P_2	AB17	I/O

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
2	IO_L30N_2	V15	I/O
2	IO_L30P_2	V14	I/O
2	IO_L31N_2	V16	I/O
2	IO_L31P_2	W16	I/O
2	IO_L32N_2	AA19	I/O
2	IO_L32P_2	AB19	I/O
2	IO_L33N_2	V17	I/O
2	IO_L33P_2	W18	I/O
2	IO_L34N_2	W17	I/O
2	IO_L34P_2	Y18	I/O
2	IO_L35N_2	AA21	I/O
2	IO_L35P_2	AB21	I/O
2	IO_L36N_2/CCLK	AA20	DUAL
2	IO_L36P_2/D0/DIN/MISO	AB20	DUAL
2	IP_2	P12	INPUT
2	IP_2	R10	INPUT
2	IP_2	R11	INPUT
2	IP_2	R9	INPUT
2	IP_2	T13	INPUT
2	IP_2	T14	INPUT
2	IP_2	T9	INPUT
2	IP_2	U10	INPUT
2	IP_2	U15	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ◆	U16	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ◆	U7	INPUT
2	IP_2	U8	INPUT
2	IP_2	V7	INPUT
2	IP_2/VREF_2	R12	VREF
2	IP_2/VREF_2	R13	VREF
2	IP_2/VREF_2	R14	VREF
2	IP_2/VREF_2	T10	VREF
2	IP_2/VREF_2	T11	VREF
2	IP_2/VREF_2	T15	VREF
2	IP_2/VREF_2	T16	VREF
2	IP_2/VREF_2	T7	VREF
2	XC3S1400AN: IP_2/VREF_2 XC3S700AN: N.C. ◆	T8	VREF
2	IP_2/VREF_2	V8	VREF

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
VCCAUX	DONE	Y19	CONFIG
VCCAUX	PROG_B	C4	CONFIG
VCCAUX	TCK	A21	JTAG
VCCAUX	TDI	F5	JTAG
VCCAUX	TDO	E19	JTAG
VCCAUX	TMS	D4	JTAG
VCCAUX	VCCAUX	D12	VCCAUX
VCCAUX	VCCAUX	E18	VCCAUX
VCCAUX	VCCAUX	E5	VCCAUX
VCCAUX	VCCAUX	H11	VCCAUX
VCCAUX	VCCAUX	L4	VCCAUX
VCCAUX	VCCAUX	M19	VCCAUX
VCCAUX	VCCAUX	P11	VCCAUX
VCCAUX	VCCAUX	V18	VCCAUX
VCCAUX	VCCAUX	V5	VCCAUX
VCCAUX	VCCAUX	W11	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	K13	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	L14	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	M13	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	N10	VCCINT
VCCINT	VCCINT	N12	VCCINT
VCCINT	VCCINT	N14	VCCINT
VCCINT	VCCINT	P13	VCCINT

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L04N_1	W21	I/O
1	IO_L04P_1	W20	I/O
1	IO_L05N_1	AC25	I/O
1	IO_L05P_1	AD26	I/O
1	IO_L06N_1	AB26	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L07P_1	AB23	I/O
1	IO_L08N_1	V19	I/O
1	IO_L08P_1	V18	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L10N_1	U20	I/O
1	IO_L10P_1	V21	I/O
1	IO_L11N_1	AA25	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L13P_1	Y22	I/O
1	IO_L14N_1	T20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L15N_1	Y25	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L18N_1	V22	I/O
1	IO_L18P_1	W23	I/O
1	IO_L19N_1	V25	I/O
1	IO_L19P_1	V24	I/O
1	IO_L21N_1	U22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L22N_1	R20	I/O
1	IO_L22P_1	R19	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IO_L23P_1	U23	I/O
1	IO_L25N_1/A3	R22	DUAL
1	IO_L25P_1/A2	R21	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L26P_1/A4	T23	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L29P_1/A8	R25	DUAL
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L37N_1	N21	I/O
1	IO_L37P_1	P22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IO_L38P_1/A12	L24	DUAL
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L41N_1	K26	I/O
1	IO_L41P_1	K25	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L42P_1/A16	N20	DUAL
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L45N_1	M22	I/O
1	IO_L45P_1	M21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L50N_1	K21	I/O
1	IO_L50P_1	L22	I/O
1	IO_L51N_1	G24	I/O