AMD Xilinx - XC3S50AN-4FTG256I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	176
Number of Logic Elements/Cells	1584
Total RAM Bits	55296
Number of I/O	195
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50an-4ftg256i

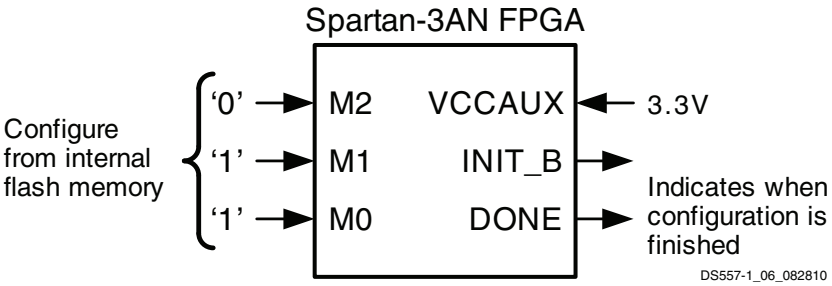


Figure 2: **Spartan-3AN FPGA Configuration Interface from Internal SPI Flash Memory**

Configuration

Spartan-3AN FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored on-chip in nonvolatile Flash memory, or externally in a PROM or some other nonvolatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Configure from internal SPI Flash memory (Figure 2)
  - Completely self-contained
  - Reduced board space
  - Easy-to-use configuration interface
- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an external industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary-Scan (JTAG), typically downloaded from a processor or system tester

The MultiBoot feature stores multiple configuration files in the on-chip Flash, providing extended life with field upgrades. MultiBoot also supports multiple system solutions with a single board to minimize inventory and simplify the addition of new features, even in the field. Flexibility is maintained to do additional MultiBoot configurations via the external configuration method.

The Spartan-3AN device authentication protocol prevents cloning. Design cloning, unauthorized overbuilding, and complete reverse engineering have driven device security requirements to higher and higher levels. Authentication moves the security from bitstream protection to the next generation of design-level security protecting both the design and embedded microcode. The authentication algorithm is entirely user defined, implemented using FPGA logic. Every product, generation, or design can have a different algorithm and functionality to enhance security.

In-System Flash Memory

Each Spartan-3AN FPGA contains abundant integrated SPI serial Flash memory, shown in Table 3, used primarily to store the FPGA's configuration bitstream. However, the Flash memory array is large enough to store at least two MultiBoot FPGA configuration bitstreams or nonvolatile data required by the FPGA application, such as code-shadowed MicroBlaze processor applications.

Table 3: **Spartan-3AN Device In-System Flash Memory**

Part Number	Total Flash Memory (Bits)	FPGA Bitstream (Bits)	Additional Flash Memory (Bits)(1)
XC3S50AN	1,081,344	437,312	642,048
XC3S200AN	4,325,376	1,196,128	3,127,872
XC3S400AN	4,325,376	1,886,560	2,437,248
XC3S700AN	8,650,752	2,732,640	5,917,824
XC3S1400AN	17,301,504	4,755,296	12,545,280

Notes:

1. Aligned to next available page location.

After configuration, the FPGA design has full access to the in-system Flash memory via an internal SPI interface; the control logic is implemented with FPGA logic. Additionally, the FPGA application itself can store nonvolatile data or provide live, in-system Flash updates.

The Spartan-3AN device in-system Flash memory supports leading-edge serial Flash features.

- Small page size (264 or 528 bytes) simplifies nonvolatile data storage
- Randomly accessible, byte addressable
- Up to 66 MHz serial data transfers
- SRAM page buffers
  - Read Flash data while programming another Flash page
  - EEPROM-like byte write functionality
  - Two buffers in most devices, one in XC3S50AN
- Page, Block, and Sector Erase

Notice of Disclaimer

DC Electrical Characteristics

In this section, specifications can be designated as Advance, Preliminary, or Production. These terms are defined as follows:

Advance: Initial estimates are based on simulation, early characterization, and/or extrapolation from the characteristics of other families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Production: These specifications are approved once the silicon has been characterized over numerous production lots. Parameter values are considered stable with no future changes expected.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. **Unless otherwise noted, the published parameter values apply to all Spartan®-3AN devices. AC and DC characteristics are specified using the same numbers for both commercial and industrial grades.**

Absolute Maximum Ratings

Stresses beyond those listed under Table 6: Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 6: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$(1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
1. For soldering guidelines, see UG112: Device Package User Guide and XAPP427: Implementation and Solder Reflow Guidelines for Pb-Free Packages.

Quiescent Current Requirements

Table 12: **Spartan-3AN FPGA Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical(2)	Commercial Maximum(2)	Industrial Maximum(2)	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XC3S50AN	2	20	30	mA
		XC3S200AN	7	50	70	mA
		XC3S400AN	10	85	125	mA
		XC3S700AN	13	120	185	mA
		XC3S1400AN	24	220	310	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XC3S50AN	0.2	2	3	mA
		XC3S200AN	0.2	2	3	mA
		XC3S400AN	0.3	3	4	mA
		XC3S700AN	0.3	3	4	mA
		XC3S1400AN	0.3	3	4	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XC3S50AN	3.1	8.1	10.1	mA
		XC3S200AN	5.1	12.1	15.1	mA
		XC3S400AN	5.1	18.1	24.1	mA
		XC3S700AN	6.1	28.1	34.1	mA
		XC3S1400AN	10.1	50.1	58.1	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 10.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. The internal SPI Flash is deselected (CSB = High); the internal SPI Flash current is consumed on the V_{CCAUX} supply rail. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 3.3V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a “blank” configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3AN FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design, and b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates. For more information on power for the In-System Flash memory, see the Power Management chapter of UG333.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Table 14: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL(3)	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24	–24		
LVCMOS33(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24(5)	24	–24		
LVCMOS25(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16(5)	16	–16		
	24(5)	24	–24		
LVCMOS18(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12(5)	12	–12		
	16(5)	16	–16		
LVCMOS15(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8(5)	8	–8		
	12(5)	12	–12		
LVCMOS12(3)	2	2	–2	0.4	V_{CCO} – 0.4
	4(5)	4	–4		
	6(5)	6	–6		
PCI33_3(4)		1.5	–0.5	10% V_{CCO}	90% V_{CCO}
PCI66_3(4)		1.5	–0.5	10% V_{CCO}	90% V_{CCO}

Table 14: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
HSTL_I(5)	8	–8	0.4	V_{CCO} - 0.4
HSTL_III(5)	24	–8	0.4	V_{CCO} - 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} - 0.4
HSTL_II_18(5)	16	–16	0.4	V_{CCO} - 0.4
HSTL_III_18	24	–8	0.4	V_{CCO} - 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II(5)	13.4	–13.4	V_{TT} – 0.603	V_{TT} + 0.603
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II(5)	16.2	–16.2	V_{TT} – 0.81	V_{TT} + 0.81
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 10 and Table 13.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} — the output current condition under which V_{OL} is tested
   I_{OH} — the output current condition under which V_{OH} is tested
   V_{OL} — the output voltage that indicates a Low logic level
   V_{OH} — the output voltage that indicates a High logic level
   V_{CCO} — the supply voltage for output drivers
   V_{TT} — the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for the Fast, Slow and QUIETIO slew attributes.
4. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCIX IOSTANDARD is available and has equivalent characteristics but no PCI-X IP is supported.
5. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.

Device DNA Read Endurance

Table 17: **Device DNA Identifier Memory Characteristics**

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations	30,000,000	Read cycles

In-System Flash Memory Data Retention, Program/Write Endurance

Table 18: **In-System Flash (ISF) Memory Characteristics**

Symbol	Description	Minimum[(1)]	Units
ISF_RETENTION	Data retention	20	Years
ISF_ACTIVE	Time that the ISF memory is selected and active. SPI_ACCESS design primitive pins CSB = Low, CLK toggling	2	Years
ISF_PAGE_CYCLES	Number of program/erase cycles, per ISF memory page	100,000	Cycles
ISF_PAGE_REWRITE	Number of cumulative random (non-sequential) page erase/program operations within a sector before pages must be rewritten	10,000	Cycles
ISF_SPR_CYCLES	Number of program/erase cycles for Sector Protection Register	10,000	Cycles
ISF_SEC_CYCLES	Number of program cycles for Sector Lockdown Register per sector, user-programmable field in Security Register, and Power-of-2 Page Size	1	Cycle

Notes:

1. Minimum value at which functionality is still guaranteed. Do not exceed these values.

Table 29: **Output Timing Adjustments for IOB *(Cont'd)***

Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26(3)	2.26(3)	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns

Table 29: **Output Timing Adjustments for IOB *(Cont'd)***

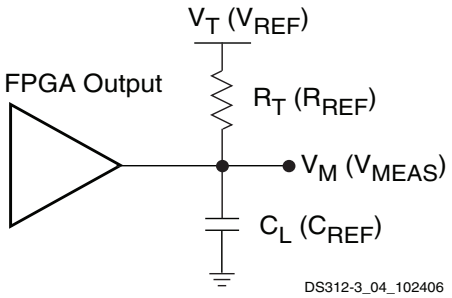
Convert Output Time from LVCMOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVCMOS18	Slow	2 mA	4.48	4.48	ns
		4 mA	3.69	3.69	ns
		6 mA	2.91	2.91	ns
		8 mA	1.99	1.99	ns
		12 mA	1.57	1.57	ns
		16 mA	1.19	1.19	ns
	Fast	2 mA	3.96	3.96	ns
		4 mA	2.57	2.57	ns
		6 mA	1.90	1.90	ns
		8 mA	1.06	1.06	ns
		12 mA	0.83	0.83	ns
		16 mA	0.63	0.63	ns
	QuietIO	2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns
		6 mA	24.08	24.08	ns
		8 mA	16.43	16.43	ns
		12 mA	14.52	14.52	ns
		16 mA	13.41	13.41	ns
LVCMOS15	Slow	2 mA	5.82	5.82	ns
		4 mA	3.97	3.97	ns
		6 mA	3.21	3.21	ns
		8 mA	2.53	2.53	ns
		12 mA	2.06	2.06	ns
	Fast	2 mA	5.23	5.23	ns
		4 mA	3.05	3.05	ns
		6 mA	1.95	1.95	ns
		8 mA	1.60	1.60	ns
		12 mA	1.30	1.30	ns
	QuietIO	2 mA	34.11	34.11	ns
		4 mA	25.66	25.66	ns
		6 mA	24.64	24.64	ns
		8 mA	22.06	22.06	ns
		12 mA	20.64	20.64	ns

Timing Measurement Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 30 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 11. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1MΩ to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 11: **Output Test Setup**

Table 30: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs[2]		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		–	0	3.3	1M	0	1.4
LVCMOS33		–	0	3.3	1M	0	1.65
LVCMOS25		–	0	2.5	1M	0	1.25
LVCMOS18		–	0	1.8	1M	0	0.9
LVCMOS15		–	0	1.5	1M	0	0.75
LVCMOS12		–	0	1.2	1M	0	0.6
PCI33_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
PCI66_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}

Configurable Logic Block (CLB) Timing

Table 33: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.60	–	0.68	ns
Setup Times						
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.18	–	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.58	–	1.88	–	ns
Hold Times						
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	0	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	–	0	–	ns
Clock Timing						
T_{CH}	The High pulse width of the CLB's CLK signal	0.63	–	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.63	–	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	770	0	667	MHz
Propagation Times						
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.62	–	0.71	ns
Set/Reset Pulse Width						
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.33	–	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 39 and Table 40) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 41 through Table 44) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 39 and Table 40.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469: *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop (DLL)

Table 39: **Recommended Operating Conditions for the DLL**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input		5(2)	280(3)	5(2)	250(3)	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \le 150$ MHz	40%	60%	40%	60%	%
			$F_{CLKIN} > 150$ MHz	45%	55%	45%	55%	%
Input Clock Jitter Tolerance and Delay Path Variation(4)								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \le 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF			$F_{CLKIN} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		–	±1	–	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 41.
3. The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to F_{BUFG}. When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.
5. The DCM specifications are guaranteed when both adjacent DCMs are locked.

DNA Port Timing

Table 46: **DNA_PORT Interface Timing**

Symbol	Description	Min	Max	Units
T_{DNASSU}	Setup time on SHIFT before the rising edge of CLK	1.0	–	ns
T_{DNASH}	Hold time on SHIFT after the rising edge of CLK	0.5	–	ns
T_{DNADSU}	Setup time on DIN before the rising edge of CLK	1.0	–	ns
T_{DNADH}	Hold time on DIN after the rising edge of CLK	0.5	–	ns
T_{DNARSU}	Setup time on READ before the rising edge of CLK	5.0	10,000	ns
T_{DNARH}	Hold time on READ after the rising edge of CLK	0	–	ns
$T_{DNADCKO}$	Clock-to-output delay on DOUT after rising edge of CLK	0.5	1.5	ns
$T_{DNACLKF}$	CLK frequency	0	100	MHz
$T_{DNACLKH}$	CLK High time	1.0	∞	ns
$T_{DNACLKL}$	CLK Low time	1.0	∞	ns

Notes:

1. The minimum READ pulse width is 5 ns, the maximum READ pulse width is 10 µs.

Internal SPI Access Port Timing

Table 47: **SPI_ACCESS Interface Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
T_{SPICCK_MOSI}	Setup time on MOSI before the active edge of CLK	4.47	–	5.0	–	ns
T_{SPICKC_MOSI}	Hold time on MOSI after the active edge of CLK	4.03	–	4.5	–	ns
T_{CSB}	CSB High time	50	–	50	–	ns
T_{SPICCK_CSB}	Setup time on CSB before the active edge of CLK	7.15	–	8.0	–	ns
T_{SPICCK_CSB}	Hold time on CSB after the active edge of CLK	7.15	–	8.0	–	ns
T_{SPICKO_MISO}	Clock-to-output delay on MISO after active edge of CLK	–	14.3	–	16.0	ns
F_{SPICLK}	CLK frequency	–	50	–	50	MHz
$F_{SPICAR1}$	CLK frequency for Continuous Array Read command	–	50	–	50	MHz
$F_{SPICAR1}$	CLK frequency for Continuous Array Read command, reduced initial latency	–	33	–	33	MHz
$T_{SPICLKL}$	CLK High time	–	∞	–	∞	ns
$T_{SPICLKH}$	CLK Low time	6.8	∞	6.8	∞	ns

Notes:

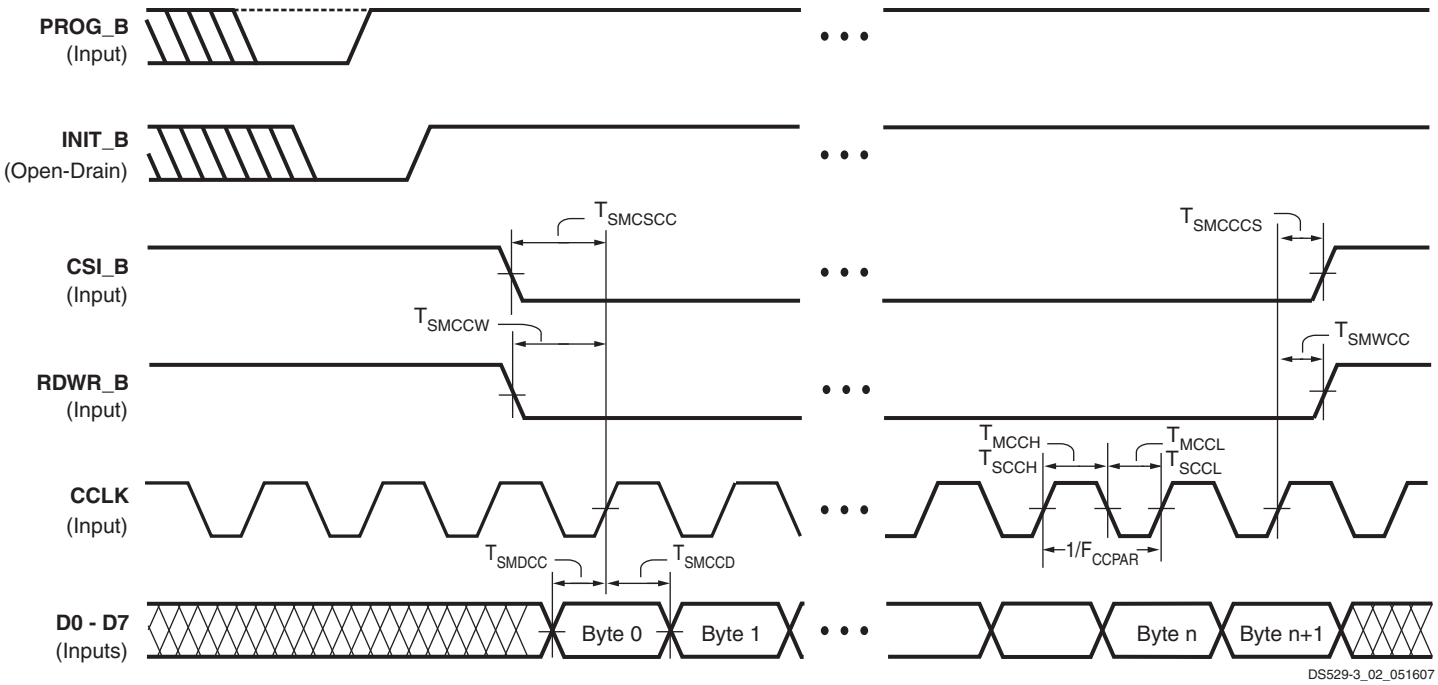
1. For details on using SPI_ACCESS and the In-System Flash memory, see UG333 *Spartan-3AN FPGA In-System Flash User Guide*.

In-System Flash (ISF) Memory Timing

Table 48: **In-System Flash (ISF) Memory Operations**

Symbol	Description	Device	Typical	Max	Units
T_{XFER}	Page to Buffer transfer time	All	–	400	µs
T_{COMP}	Page to Buffer compare time	All	–	400	µs
T_{PP}	Page Programming time	XC3S50AN XC3S200AN XC3S400AN	2	4	ms
		XC3S700AN XC3S1400AN	3	6	ms
T_{PE}	Page Erase time	XC3S50AN XC3S200AN XC3S400AN	13	32	ms
		XC3S700AN XC3S1400AN	15	35	ms
T_{PEP}	Page Erase and Programming time	XC3S50AN XC3S200AN XC3S400AN XC3S700AN	14	35	ms
		XC3S1400AN	17	40	ms
T_{BE}	Block Erase time	XC3S50AN	15	35	ms
		XC3S200AN XC3S400AN	30	75	ms
		XC3S700AN XC3S1400AN	45	100	ms
T_{SE}	Sector Erase time	XC3S50AN	0.8	2.5	s
		XC3S200AN XC3S400AN XC3S700AN XC3S1400AN	1.6	5	s

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0–D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0–D7 bus.
2. To pause configuration, pause CCLK instead of de-asserting CSI_B. See UG332, Chapter 7, section “Non-Continuous SelectMAP Data Loading” for more details.

Figure 15: **Waveforms for Slave Parallel Configuration**

Table 56: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		All Speed Grades		Units
			Min	Max	
Setup Times					
T_{SMDCC}	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}(2)	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		15	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1.0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10.
2. Some Xilinx documents refer to Parallel modes as SelectMAP modes.

Table 59: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 51		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 51		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 55		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 56		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	–	ns

Table 60: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 0.5\,T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

IEEE 1149.1/1532 JTAG Test Access Port Timing

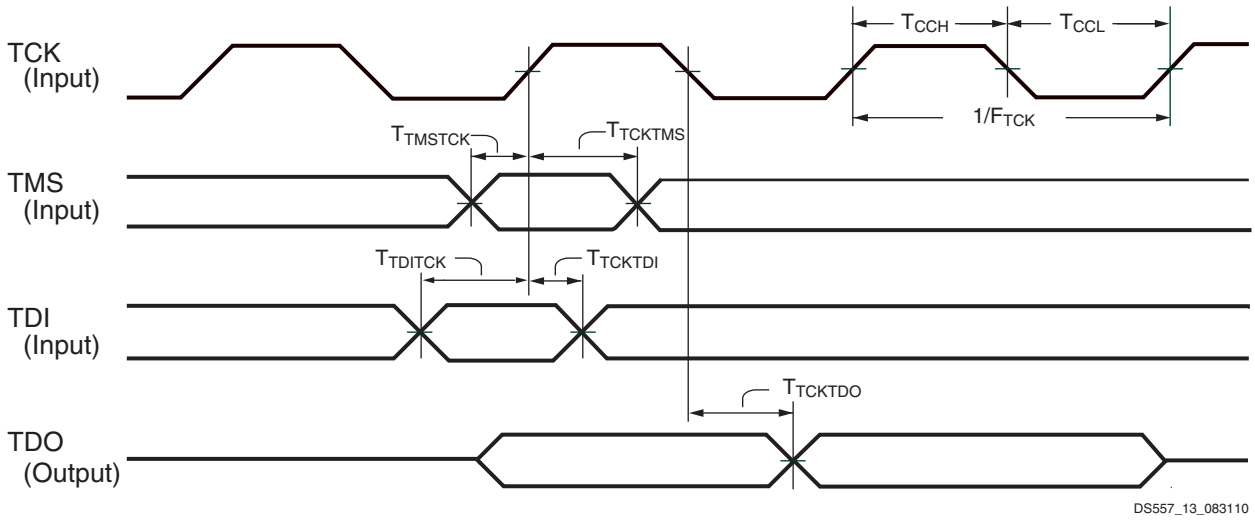


Figure 18: **JTAG Waveforms**

Table 62: **Types of Pins on Spartan-3AN FPGAs *(Cont'd)***

Type with Color Code	Description	Pin Name(s) in Type(1)
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on the DONE and PROG_B signals.	DONE, PROG_B
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a dual-purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. The In-System Flash memory is powered by VCCAUX. All must be connected to +3.3V.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination.	N.C.

Notes:

1. # = I/O bank number, an integer between 0 and 3.

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in Table 63.

Table 63: **Power and Ground Supply Pins by Package**

Package	VCCINT	VCCAUX	VCCO	GND
TQG144	4	4	8	13
FTG256	6	4	16	28
FGG400	9	8	22	43
FGG484	15	10	24	53
FGG676	23	14	36	77

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/Os depend on the device type and the package in which it is available, as shown in Table 64. The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. AWAKE is counted here as a dual-purpose I/O pin. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—N.C.—pins on the device.

Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in the top or bottom banks (I/O banks 0 and 2). Inputs are unrestricted. For more details, see the "Using I/O Resources" chapter in UG331.

Table 64: **Maximum User I/O by Package**

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF (1)	CLK	N.C.
XC3S50AN	TQG144	108	7	50	42	2	26	8	30	0
	FTG256	144	32	64	53	20	26	15	30	51
XC3S200AN	FTG256	195	35	90	69	21	52	21	32	0
XC3S400AN	FTG256	195	35	90	69	21	52	21	32	0
	FGG400	311	63	142	155	46	52	26	32	0
XC3S700AN	FGG484	372	84	165	194	61	52	33	32	3
XC3S1400AN	FGG484	375	87	165	195	62	52	34	32	0
	FGG676	502	94	227	313	67	52	38	32	17

Notes:

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and foot-prints are available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

Package Overview

Table 65 shows the five low-cost, space-saving production package styles for the Spartan-3AN family.

Table 65: **Spartan-3AN Family Package Options**

Package	Leads	Type	Maximum I/Os	Lead Pitch (mm)	Body Area (mm)	Height (mm)
TQ144/TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	20 x 20	1.60
FT256/FTG256	256	Fine-pitch Thin Ball Grid Array (FBGA)	195	1.0	17 x 17	1.55
FG400/FGG400	400	Fine-pitch Ball Grid Array (FBGA)	311	1.0	21 x 21	2.43
FG484/FGG484	484	Fine-pitch Ball Grid Array (FBGA)	375	1.0	23 x 23	2.60
FG676/FGG676	676	Fine-pitch Ball Grid Array (FBGA)	502	1.0	27 x 27	2.60

Notes:

1. For mass, refer to the MDDS files (see Table 66).

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra “G” in the package style name. For example, the standard “CS484” package becomes “CSG484” when ordered as the Pb-free option. Leaded (Pb) packages are available for selected devices, with the same pinout and without the “G” in the ordering code; See Table 5, page 7 for more information. The mechanical dimensions of the Pb and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 66.

For additional package information, see UG112: *Device Package User Guide*.

Table 70: **Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN) *(Cont'd)***

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
0	N.C.	IO_L14N_0/VREF_0	E7	VREF
0	N.C.	IO_L14P_0	F8	I/O
0	IO_L15N_0	IO_L15N_0	B6	I/O
0	IO_L15P_0	IO_L15P_0	A6	I/O
0	IO_L16N_0	IO_L16N_0	C6	I/O
0	IO_L16P_0	IO_L16P_0	D7	I/O
0	IO_L17N_0	IO_L17N_0	C5	I/O
0	IO_L17P_0	IO_L17P_0	A5	I/O
0	IO_L18N_0	IO_L18N_0	B4	I/O
0	IO_L18P_0	IO_L18P_0	A4	I/O
0	IO_L19N_0	IO_L19N_0	B3	I/O
0	IO_L19P_0	IO_L19P_0	A3	I/O
0	IO_L20N_0/PUDC_B	IO_L20N_0/PUDC_B	D5	DUAL
0	IO_L20P_0/VREF_0	IO_L20P_0/VREF_0	C4	VREF
0	IP_0	IP_0	D6	INPUT
0	IP_0	IP_0	D12	INPUT
0	IP_0	IP_0	E6	INPUT
0	IP_0	IP_0	F7	INPUT
0	IP_0	IP_0	F9	INPUT
0	IP_0	IP_0	F10	INPUT
0	IP_0/VREF_0	IP_0/VREF_0	E9	VREF
0	VCCO_0	VCCO_0	B5	VCCO
0	VCCO_0	VCCO_0	B9	VCCO
0	VCCO_0	VCCO_0	B13	VCCO
0	VCCO_0	VCCO_0	E8	VCCO
1	IO_L01N_1/LDC2	IO_L01N_1/LDC2	N14	DUAL
1	IO_L01P_1/HDC	IO_L01P_1/HDC	N13	DUAL
1	IO_L02N_1/LDC0	IO_L02N_1/LDC0	P15	DUAL
1	IO_L02P_1/LDC1	IO_L02P_1/LDC1	R15	DUAL
1	IO_L03N_1	IO_L03N_1/A1	N16	DUAL
1	IO_L03P_1	IO_L03P_1/A0	P16	DUAL
1	N.C.	IO_L05N_1/VREF_1	M14	VREF
1	N.C.	IO_L05P_1	M13	I/O
1	N.C.	IO_L06N_1/A3	K13	DUAL
1	N.C.	IO_L06P_1/A2	L13	DUAL
1	N.C.	IO_L07N_1/A5	M16	DUAL
1	N.C.	IO_L07P_1/A4	M15	DUAL
1	N.C.	IO_L08N_1/A7	L16	DUAL
1	N.C.	IO_L08P_1/A6	L14	DUAL
1	IO_L10N_1	IO_L10N_1/A9	J13	DUAL

Table 76: **Spartan-3AN FGG400 Pinout *(Cont'd)***

Bank	Pin Name	FGG400 Ball	Type
0	IO_L32N_0/PUDC_B	B2	DUAL
0	IO_L32P_0/VREF_0	A2	VREF
0	IP_0	E14	INPUT
0	IP_0	F11	INPUT
0	IP_0	F14	INPUT
0	IP_0	G8	INPUT
0	IP_0	G9	INPUT
0	IP_0	G10	INPUT
0	IP_0	G12	INPUT
0	IP_0	G13	INPUT
0	IP_0	H9	INPUT
0	IP_0	H10	INPUT
0	IP_0	H11	INPUT
0	IP_0	H12	INPUT
0	IP_0/VREF_0	G11	VREF
0	VCCO_0	B4	VCCO
0	VCCO_0	B10	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	D7	VCCO
0	VCCO_0	D13	VCCO
0	VCCO_0	F10	VCCO
1	IO_L01N_1/LDC2	V20	DUAL
1	IO_L01P_1/HDC	W20	DUAL
1	IO_L02N_1/LDC0	U18	DUAL
1	IO_L02P_1/LDC1	V19	DUAL
1	IO_L03N_1/A1	R16	DUAL
1	IO_L03P_1/A0	T17	DUAL
1	IO_L05N_1	T20	I/O
1	IO_L05P_1	T18	I/O
1	IO_L06N_1	U20	I/O
1	IO_L06P_1	U19	I/O
1	IO_L07N_1	P17	I/O
1	IO_L07P_1	P16	I/O
1	IO_L08N_1	R17	I/O
1	IO_L08P_1	R18	I/O
1	IO_L09N_1	R20	I/O
1	IO_L09P_1	R19	I/O
1	IO_L10N_1/VREF_1	P20	VREF
1	IO_L10P_1	P18	I/O
1	IO_L12N_1/A3	N17	DUAL

Table 76: **Spartan-3AN FGG400 Pinout *(Cont'd)***

Bank	Pin Name	FGG400 Ball	Type
1	IO_L12P_1/A2	N15	DUAL
1	IO_L13N_1/A5	N19	DUAL
1	IO_L13P_1/A4	N18	DUAL
1	IO_L14N_1/A7	M18	DUAL
1	IO_L14P_1/A6	M17	DUAL
1	IO_L16N_1/A9	L16	DUAL
1	IO_L16P_1/A8	L15	DUAL
1	IO_L17N_1/RHCLK1	M20	RHCLK
1	IO_L17P_1/RHCLK0	M19	RHCLK
1	IO_L18N_1/TRDY1/RHCLK3	L18	RHCLK
1	IO_L18P_1/RHCLK2	L19	RHCLK
1	IO_L20N_1/RHCLK5	L17	RHCLK
1	IO_L20P_1/RHCLK4	K18	RHCLK
1	IO_L21N_1/RHCLK7	J20	RHCLK
1	IO_L21P_1/IRDY1/RHCLK6	K20	RHCLK
1	IO_L22N_1/A11	J18	DUAL
1	IO_L22P_1/A10	J19	DUAL
1	IO_L24N_1	K16	I/O
1	IO_L24P_1	J17	I/O
1	IO_L25N_1/A13	H18	DUAL
1	IO_L25P_1/A12	H19	DUAL
1	IO_L26N_1/A15	G20	DUAL
1	IO_L26P_1/A14	H20	DUAL
1	IO_L28N_1	H17	I/O
1	IO_L28P_1	G18	I/O
1	IO_L29N_1/A17	F19	DUAL
1	IO_L29P_1/A16	F20	DUAL
1	IO_L30N_1/A19	F18	DUAL
1	IO_L30P_1/A18	G17	DUAL
1	IO_L32N_1	E19	I/O
1	IO_L32P_1	E20	I/O
1	IO_L33N_1	F17	I/O
1	IO_L33P_1	E18	I/O
1	IO_L34N_1	D18	I/O
1	IO_L34P_1	D20	I/O
1	IO_L36N_1/A21	F16	DUAL
1	IO_L36P_1/A20	G16	DUAL
1	IO_L37N_1/A23	C19	DUAL
1	IO_L37P_1/A22	C20	DUAL
1	IO_L38N_1/A25	B19	DUAL

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
3	IP_L04N_3/VREF_3	H7	VREF
3	IP_L04P_3	H8	INPUT
3	IP_L11N_3	K8	INPUT
3	IP_L11P_3	J7	INPUT
3	IP_L15N_3/VREF_3	L8	VREF
3	IP_L15P_3	K7	INPUT
3	IP_L19N_3	M8	INPUT
3	IP_L19P_3	L7	INPUT
3	IP_L23N_3	M6	INPUT
3	IP_L23P_3	M7	INPUT
3	IP_L27N_3	N9	INPUT
3	IP_L27P_3	N8	INPUT
3	IP_L31N_3	N5	INPUT
3	IP_L31P_3	N6	INPUT
3	IP_L35N_3	P8	INPUT
3	IP_L35P_3	N7	INPUT
3	IP_L39N_3	R8	INPUT
3	IP_L39P_3	P7	INPUT
3	IP_L46N_3/VREF_3	T6	VREF
3	IP_L46P_3	R7	INPUT
3	VCCO_3	E2	VCCO
3	VCCO_3	J2	VCCO
3	VCCO_3	J6	VCCO
3	VCCO_3	N2	VCCO
3	VCCO_3	P6	VCCO
3	VCCO_3	V2	VCCO
GND	GND	A1	GND
GND	GND	A22	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA7	GND
GND	GND	AB1	GND
GND	GND	AB22	GND
GND	GND	B12	GND
GND	GND	B16	GND
GND	GND	B7	GND
GND	GND	C20	GND
GND	GND	C3	GND
GND	GND	D14	GND
GND	GND	D9	GND

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
GND	GND	F11	GND
GND	GND	F17	GND
GND	GND	F6	GND
GND	GND	G2	GND
GND	GND	G21	GND
GND	GND	J11	GND
GND	GND	J13	GND
GND	GND	J14	GND
GND	GND	J19	GND
GND	GND	J4	GND
GND	GND	J9	GND
GND	GND	K10	GND
GND	GND	K12	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L17	GND
GND	GND	L2	GND
GND	GND	L6	GND
GND	GND	L9	GND
GND	GND	M10	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M21	GND
GND	GND	N11	GND
GND	GND	N13	GND
GND	GND	P10	GND
GND	GND	P14	GND
GND	GND	P19	GND
GND	GND	P4	GND
GND	GND	P9	GND
GND	GND	T12	GND
GND	GND	T2	GND
GND	GND	T21	GND
GND	GND	U17	GND
GND	GND	U6	GND
GND	GND	W10	GND
GND	GND	W14	GND
GND	GND	Y20	GND
GND	GND	Y3	GND
VCCAUX	SUSPEND	U18	PWR MGMT

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
1	IO_L02P_1/LDC1	AE26	DUAL
1	IO_L03N_1/A1	AC24	DUAL
1	IO_L03P_1/A0	AC23	DUAL
1	IO_L04N_1	W21	I/O
1	IO_L04P_1	W20	I/O
1	IO_L05N_1	AC25	I/O
1	IO_L05P_1	AD26	I/O
1	IO_L06N_1	AB26	I/O
1	IO_L06P_1	AC26	I/O
1	IO_L07N_1/VREF_1	AB24	VREF
1	IO_L07P_1	AB23	I/O
1	IO_L08N_1	V19	I/O
1	IO_L08P_1	V18	I/O
1	IO_L09N_1	AA23	I/O
1	IO_L09P_1	AA22	I/O
1	IO_L10N_1	U20	I/O
1	IO_L10P_1	V21	I/O
1	IO_L11N_1	AA25	I/O
1	IO_L11P_1	AA24	I/O
1	IO_L12N_1	U18	I/O
1	IO_L12P_1	U19	I/O
1	IO_L13N_1	Y23	I/O
1	IO_L13P_1	Y22	I/O
1	IO_L14N_1	T20	I/O
1	IO_L14P_1	U21	I/O
1	IO_L15N_1	Y25	I/O
1	IO_L15P_1	Y24	I/O
1	IO_L17N_1	T17	I/O
1	IO_L17P_1	T18	I/O
1	IO_L18N_1	V22	I/O
1	IO_L18P_1	W23	I/O
1	IO_L19N_1	V25	I/O
1	IO_L19P_1	V24	I/O
1	IO_L21N_1	U22	I/O
1	IO_L21P_1	V23	I/O
1	IO_L22N_1	R20	I/O
1	IO_L22P_1	R19	I/O
1	IO_L23N_1/VREF_1	U24	VREF
1	IO_L23P_1	U23	I/O
1	IO_L25N_1/A3	R22	DUAL

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
1	IO_L25P_1/A2	R21	DUAL
1	IO_L26N_1/A5	T24	DUAL
1	IO_L26P_1/A4	T23	DUAL
1	IO_L27N_1/A7	R17	DUAL
1	IO_L27P_1/A6	R18	DUAL
1	IO_L29N_1/A9	R26	DUAL
1	IO_L29P_1/A8	R25	DUAL
1	IO_L30N_1/RHCLK1	P20	RHCLK
1	IO_L30P_1/RHCLK0	P21	RHCLK
1	IO_L31N_1/TRDY1/RHCLK3	P25	RHCLK
1	IO_L31P_1/RHCLK2	P26	RHCLK
1	IO_L33N_1/RHCLK5	N24	RHCLK
1	IO_L33P_1/RHCLK4	P23	RHCLK
1	IO_L34N_1/RHCLK7	N19	RHCLK
1	IO_L34P_1/IRDY1/RHCLK6	P18	RHCLK
1	IO_L35N_1/A11	M25	DUAL
1	IO_L35P_1/A10	M26	DUAL
1	IO_L37N_1	N21	I/O
1	IO_L37P_1	P22	I/O
1	IO_L38N_1/A13	M23	DUAL
1	IO_L38P_1/A12	L24	DUAL
1	IO_L39N_1/A15	N17	DUAL
1	IO_L39P_1/A14	N18	DUAL
1	IO_L41N_1	K26	I/O
1	IO_L41P_1	K25	I/O
1	IO_L42N_1/A17	M20	DUAL
1	IO_L42P_1/A16	N20	DUAL
1	IO_L43N_1/A19	J25	DUAL
1	IO_L43P_1/A18	J26	DUAL
1	IO_L45N_1	M22	I/O
1	IO_L45P_1	M21	I/O
1	IO_L46N_1	K22	I/O
1	IO_L46P_1	K23	I/O
1	IO_L47N_1	M18	I/O
1	IO_L47P_1	M19	I/O
1	IO_L49N_1	J22	I/O
1	IO_L49P_1	J23	I/O
1	IO_L50N_1	K21	I/O
1	IO_L50P_1	L22	I/O
1	IO_L51N_1	G24	I/O