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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	176
Number of Logic Elements/Cells	1584
Total RAM Bits	55296
Number of I/O	108
Number of Gates	50000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s50an-4tqg144i

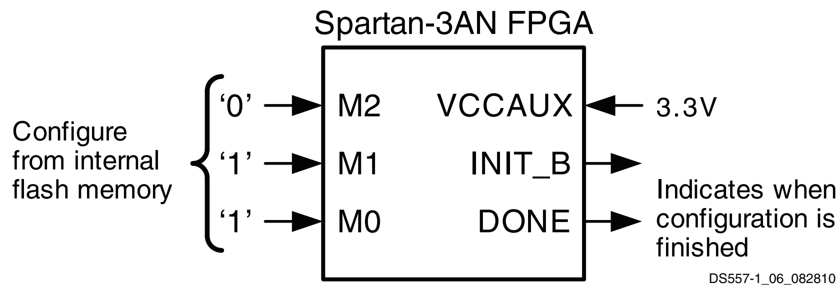

Figure 2: **Spartan-3AN FPGA Configuration Interface from Internal SPI Flash Memory**

Configuration

Spartan-3AN FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored on-chip in nonvolatile Flash memory, or externally in a PROM or some other nonvolatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Configure from internal SPI Flash memory (Figure 2)
    - Completely self-contained
    - Reduced board space
    - Easy-to-use configuration interface
- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an external industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary-Scan (JTAG), typically downloaded from a processor or system tester

The MultiBoot feature stores multiple configuration files in the on-chip Flash, providing extended life with field upgrades. MultiBoot also supports multiple system solutions with a single board to minimize inventory and simplify the addition of new features, even in the field. Flexibility is maintained to do additional MultiBoot configurations via the external configuration method.

The Spartan-3AN device authentication protocol prevents cloning. Design cloning, unauthorized overbuilding, and complete reverse engineering have driven device security requirements to higher and higher levels. Authentication moves the security from bitstream protection to the next generation of design-level security protecting both the design and embedded microcode. The authentication algorithm is entirely user defined, implemented using FPGA logic. Every product, generation, or design can have a different algorithm and functionality to enhance security.

In-System Flash Memory

Each Spartan-3AN FPGA contains abundant integrated SPI serial Flash memory, shown in Table 3, used primarily to store the FPGA's configuration bitstream. However, the Flash memory array is large enough to store at least two MultiBoot FPGA configuration bitstreams or nonvolatile data required by the FPGA application, such as code-shadowed MicroBlaze processor applications.

Table 3: **Spartan-3AN Device In-System Flash Memory**

Part Number	Total Flash Memory (Bits)	FPGA Bitstream (Bits)	Additional Flash Memory (Bits)[(1)]
XC3S50AN	1,081,344	437,312	642,048
XC3S200AN	4,325,376	1,196,128	3,127,872
XC3S400AN	4,325,376	1,886,560	2,437,248
XC3S700AN	8,650,752	2,732,640	5,917,824
XC3S1400AN	17,301,504	4,755,296	12,545,280

Notes:
1. Aligned to next available page location.

After configuration, the FPGA design has full access to the in-system Flash memory via an internal SPI interface; the control logic is implemented with FPGA logic. Additionally, the FPGA application itself can store nonvolatile data or provide live, in-system Flash updates.

The Spartan-3AN device in-system Flash memory supports leading-edge serial Flash features.

- Small page size (264 or 528 bytes) simplifies nonvolatile data storage
- Randomly accessible, byte addressable
- Up to 66 MHz serial data transfers
- SRAM page buffers
    - Read Flash data while programming another Flash page
    - EEPROM-like byte write functionality
    - Two buffers in most devices, one in XC3S50AN
- Page, Block, and Sector Erase

- Sector-based data protection and security features
  - Sector Protect: Write- and erase-protect a sector (changeable)
  - Sector Lockdown: Sector data is unchangeable (permanent)
- 128-byte Security Register
  - Separate from FPGA's unique Device DNA identifier
  - 64-byte factory-programmed identifier unique to the in-system Flash memory
  - 64-byte one-time programmable, user-programmable field
- 100,000 Program/Erase cycles
- 20-year data retention
- Comprehensive programming support
  - In-system prototype programming via JTAG using Xilinx Platform Cable USB and iMPACT software
  - Product programming support using BPM Microsystems programmers with appropriate programming adapter
  - Design examples demonstrating in-system programming from a Spartan-3AN FPGA application

I/O Capabilities

The Spartan-3AN FPGA SelectIO interface supports many popular single-ended and differential standards. Table 4 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional, input-only pins as indicated in Table 4.

Spartan-3AN FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3AN FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 4: **Available User I/Os and Differential (Diff) I/O Pairs**

Package [(1)]	**TQ144 TQG144**		**FT256 FTG256**		**FG400 FGG400**		**FG484 FGG484**		**FG676 FGG676**	
Body Size (mm)	**20 x 20** [(2)]		**17 x 17**		**21 x 21**		**23 x 23**		**27 x 27**	
Device [(3)]	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**
XC3S50AN	**108** [(4)] *(7)*	**50** *(24)*	**144** *(32)*	**64** *(32)*	–	–	–	–	–	–
XC3S200AN	–	–	**195** *(35)*	**90** *(50)*	–	–	–	–	–	–
XC3S400AN	–	–	**195** *(35)*	**90** *(50)*	**311** *(63)*	**142** *(78)*	–	–	–	–
XC3S700AN	–	–	–	–	–	–	**372** *(84)*	**165** *(93)*	–	–
XC3S1400AN	–	–	–	–	–	–	**375** *(87)*	**165** *(93)*	**502** *(94)*	**227** *(131)*

Notes:

1. See Pb and Pb-Free Packaging, page 7 for details on Pb and Pb-free packaging options.
2. The footprint for the TQ(G)144 (22 mm x 22 mm) package is larger than the package body.
3. Each Spartan-3AN FPGA has a pin-compatible Spartan-3A FPGA equivalent, although Spartan-3A FPGAs do not have internal SPI flash and offer more part/package combinations.
4. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

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General Recommended Operating Conditions

Table 10: **General Recommended Operating Conditions**

Symbol	Description			Min	Nominal	Max	Units
T_J	Junction temperature	Commercial		0	–	85	°C
		Industrial		–40	–	100	°C
V_{CCINT}	Internal supply voltage			1.14	1.20	1.26	V
V_{CCO} (1)	Output driver supply voltage			1.10	–	3.60	V
V_{CCAUX}	Auxiliary supply voltage	V_{CCAUX} = 3.3V		3.00	3.30	3.60	V
V_{IN} (2)	Input voltage	PCI IOSTANDARD		–0.5	–	V_{CCO} + 0.5	V
		All other IOSTANDARDs	IP or IO_#	–0.5	–	4.10	V
			IO_Lxxy_# (3)	–0.5	–	4.10	V
T_{IN}	Input signal transition time (4)			–	–	500	ns

Notes:

1. This V_{CCO} range spans the lowest and highest operating voltages for all supported I/O standards. Table 13 lists the recommended V_{CCO} range specific to each of the single-ended I/O standards, and Table 15 lists that specific to the differential standards.
2. See XAPP459, *Eliminating I/O Coupling Effects when Interfacing Large-Swing Single-Ended Signals to User I/O Pins on Spartan-3 Families*.
3. For single-ended signals that are placed on a differential-capable I/O, V_{IN} of –0.2V to –0.5V is supported but can cause increased leakage between the two pins. See *Parasitic Leakage* in UG331, *Spartan-3 Generation FPGA User Guide*.
4. Measured between 10% and 90% V_{CCO}. Follow Signal Integrity recommendations.

Input Setup and Hold Times

Table 23: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_ DELAY_ VALUE	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25[(2)]	0	XC3S50AN	1.56	1.58	ns
				XC3S200AN	1.71	1.81	ns
				XC3S400AN	1.30	1.51	ns
				XC3S700AN	1.34	1.51	ns
				XC3S1400AN	1.36	1.74	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25[(2)]	1	XC3S50AN	2.16	2.18	ns
			2		3.10	3.12	ns
			3		3.51	3.76	ns
			4		4.04	4.32	ns
			5		3.88	4.24	ns
			6		4.72	5.09	ns
			7		5.47	5.94	ns
			8		5.97	6.52	ns
			1	XC3S200AN	2.05	2.20	ns
			2		2.72	2.93	ns
			3		3.38	3.78	ns
			4		3.88	4.37	ns
			5		3.69	4.20	ns
			6		4.56	5.23	ns
			7		5.34	6.11	ns
			8		5.85	6.71	ns
			1	XC3S400AN	1.79	2.02	ns
			2		2.43	2.67	ns
			3		3.02	3.43	ns
			4		3.49	3.96	ns
			5		3.41	3.95	ns
			6		4.20	4.81	ns
			7		4.96	5.66	ns
			8		5.44	6.19	ns

Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type			
			TQG144		FTG256, FGG400, FGG484, FGG676	
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
LVCMOS25	Slow	2	16	16	76	76
		4	10	10	46	46
		6	8	8	33	33
		8	7	7	24	24
		12	6	6	18	18
		16	–	6	–	11
		24	–	5	–	7
	Fast	2	12	12	18	18
		4	10	10	14	14
		6	8	8	6	6
		8	6	6	6	6
		12	3	3	3	3
		16	–	3	–	3
		24	–	2	–	2
	QuietIO	2	36	36	76	76
		4	30	30	60	60
		6	24	24	48	48
		8	20	20	36	36
		12	12	12	36	36
		16	–	12	–	36
		24	–	8	–	8

Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type			
			TQG144		FTG256, FGG400, FGG484, FGG676	
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
LVCMOS18	Slow	2	13	13	64	64
		4	8	8	34	34
		6	8	8	22	22
		8	7	7	18	18
		12	–	5	–	13
		16	–	5	–	10
	Fast	2	13	13	18	18
		4	8	8	9	9
		6	7	7	7	7
		8	4	4	4	4
		12	–	4	–	4
		16	–	3	–	3
	QuietIO	2	30	30	64	64
		4	24	24	64	64
		6	20	20	48	48
		8	16	16	36	36
		12	–	12	–	36
		16	–	12	–	24
LVCMOS15	Slow	2	12	12	55	55
		4	7	7	31	31
		6	7	7	18	18
		8	–	6	–	15
		12	–	5	–	10
	Fast	2	10	10	25	25
		4	7	7	10	10
		6	6	6	6	6
		8	–	4	–	4
		12	–	3	–	3
	QuietIO	2	30	30	70	70
		4	21	21	40	40
		6	18	18	31	31
		8	–	12	–	31
		12	–	12	–	20

Block RAM Timing

Table 38: **Block RAM Timing**

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{RCKO}	When reading from block RAM, the delay from the active transition at the CLK input to data appearing at the DOUT output	–	2.06	–	2.49	ns
Setup Times						
T_{RCCK_ADDR}	Setup time for the ADDR inputs before the active transition at the CLK input of the block RAM	0.32	–	0.36	–	ns
T_{RDCK_DIB}	Setup time for data at the DIN inputs before the active transition at the CLK input of the block RAM	0.28	–	0.31	–	ns
T_{RCCK_ENB}	Setup time for the EN input before the active transition at the CLK input of the block RAM	0.69	–	0.77	–	ns
T_{RCCK_WEB}	Setup time for the WE input before the active transition at the CLK input of the block RAM	1.12	–	1.26	–	ns
Hold Times						
T_{RCKC_ADDR}	Hold time on the ADDR inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCKD_DIB}	Hold time on the DIN inputs after the active transition at the CLK input	0	–	0	–	ns
T_{RCKC_ENB}	Hold time on the EN input after the active transition at the CLK input	0	–	0	–	ns
T_{RCKC_WEB}	Hold time on the WE input after the active transition at the CLK input	0	–	0	–	ns
Clock Timing						
T_{BPWH}	High pulse width of the CLK signal	1.56	–	1.79	–	ns
T_{BPWL}	Low pulse width of the CLK signal	1.56	–	1.79	–	ns
Clock Frequency						
F_{BRAM}	Block RAM clock frequency	0	320	0	280	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 39 and Table 40) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 41 through Table 44) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 39 and Table 40.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469: *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop (DLL)

Table 39: **Recommended Operating Conditions for the DLL**

Symbol		Description		Speed Grade -5 Min	-5 Max	-4 Min	-4 Max	Units
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input		5[2]	280[3]	5[2]	250[3]	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \leq$ 150 MHz	40%	60%	40%	60%	%
			F_{CLKIN} > 150 MHz	45%	55%	45%	55%	%
Input Clock Jitter Tolerance and Delay Path Variation[4]								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \leq$ 150 MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF			F_{CLKIN} > 150 MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		–	±1	–	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 41.
3. The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to F_{BUFG}. When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.
5. The DCM specifications are guaranteed when both adjacent DCMs are locked.

Table 52: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by ***ConfigRate*** setting	1 *(power-on value)*	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F_{CCLK3}		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F_{CCLK6}		6 (*default*)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F_{CCLK7}		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F_{CCLK8}		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F_{CCLK10}		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F_{CCLK12}		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F_{CCLK13}		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F_{CCLK17}		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F_{CCLK22}		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F_{CCLK25}		25	Commercial	10.00	20.90	MHz
			Industrial		22.23	MHz
F_{CCLK27}		27	Commercial	10.80	22.39	MHz
			Industrial		23.81	MHz
F_{CCLK33}		33	Commercial	13.20	27.48	MHz
			Industrial		29.23	MHz
F_{CCLK44}		44	Commercial	17.60	37.60	MHz
			Industrial		40.00	MHz
F_{CCLK50}		50	Commercial	20.00	44.80	MHz
			Industrial		47.66	MHz
$F_{CCLK100}$		100	Commercial	40.00	88.68	MHz
			Industrial		94.34	MHz

Table 53: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting																Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T_{MCCL}, T_{MCCH}	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

External Serial Peripheral Interface (SPI) Configuration Timing

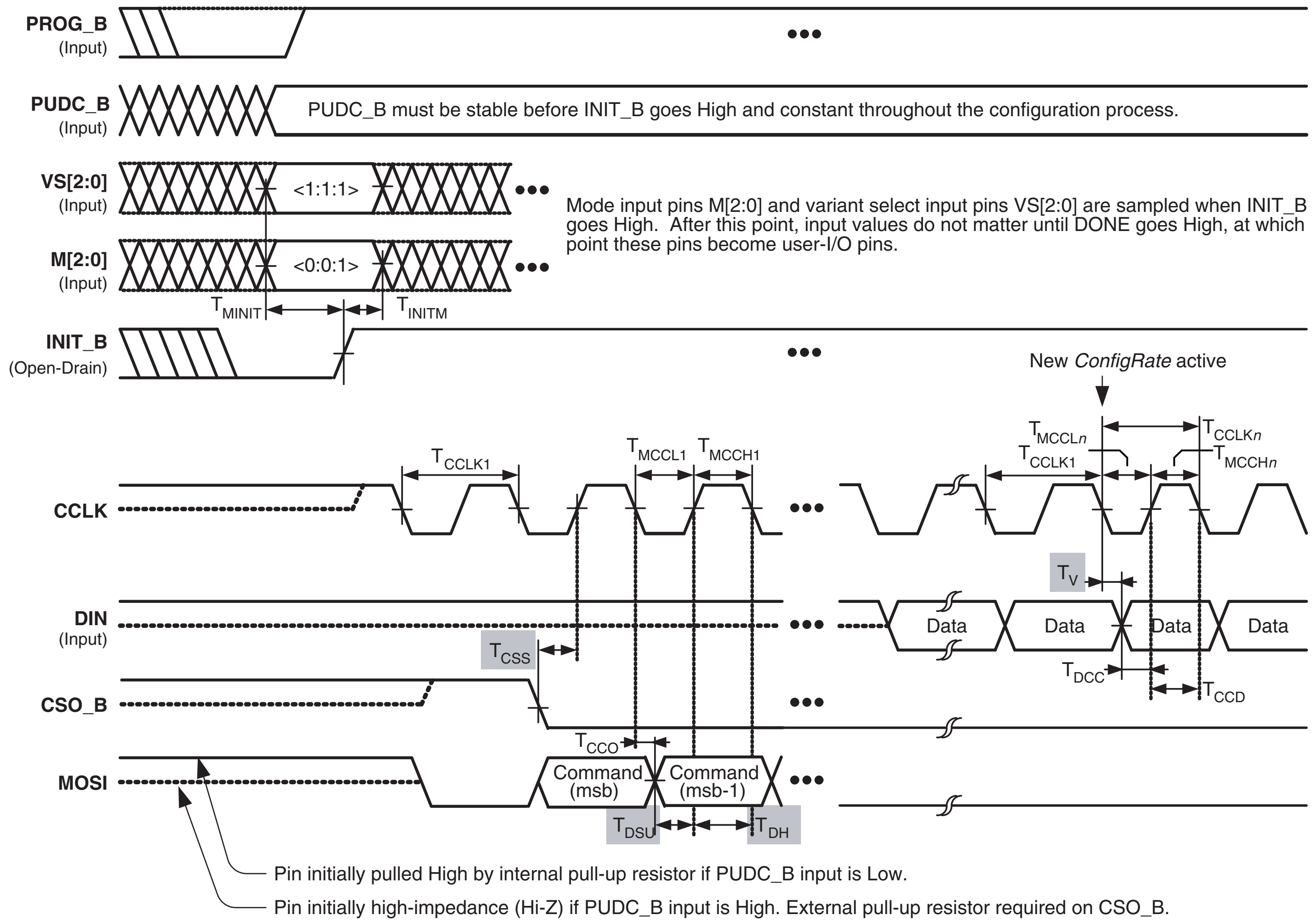

Figure 16: **Waveforms for External Serial Peripheral Interface (SPI) Configuration**

Table 57: **Timing for External Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 51		
T_{CCLKn}	CCLK clock period after FPGA loads ***ConfigRate*** bitstream option setting	See Table 51		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling clock edge	See Table 55		
T_{DCC}	Setup time on the DIN data input before CCLK rising clock edge	See Table 55		
T_{CCD}	Hold time on the DIN data input after CCLK rising clock edge	See Table 55		

Table 59: **Timing for Byte-wide Peripheral Interface (BPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 51		
T_{CCLKn}	CCLK clock period after FPGA loads ConfigRate setting	See Table 51		
T_{MINIT}	Setup time on M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
$T_{INITADDR}$	Minimum period of initial A[25:0] address cycle; LDC[2:0] and HDC are asserted and valid	5	5	T_{CCLK1} cycles
T_{CCO}	Address A[25:0] outputs valid after CCLK falling edge	See Table 55		
T_{DCC}	Setup time on D[7:0] data inputs before CCLK rising edge	See T_{SMDCC} in Table 56		
T_{CCD}	Hold time on D[7:0] data inputs after CCLK rising edge	0	–	ns

Table 60: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \le T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \le T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \le 0.5 T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time[3]	$T_{BYTE} \le T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

IEEE 1149.1/1532 JTAG Test Access Port Timing

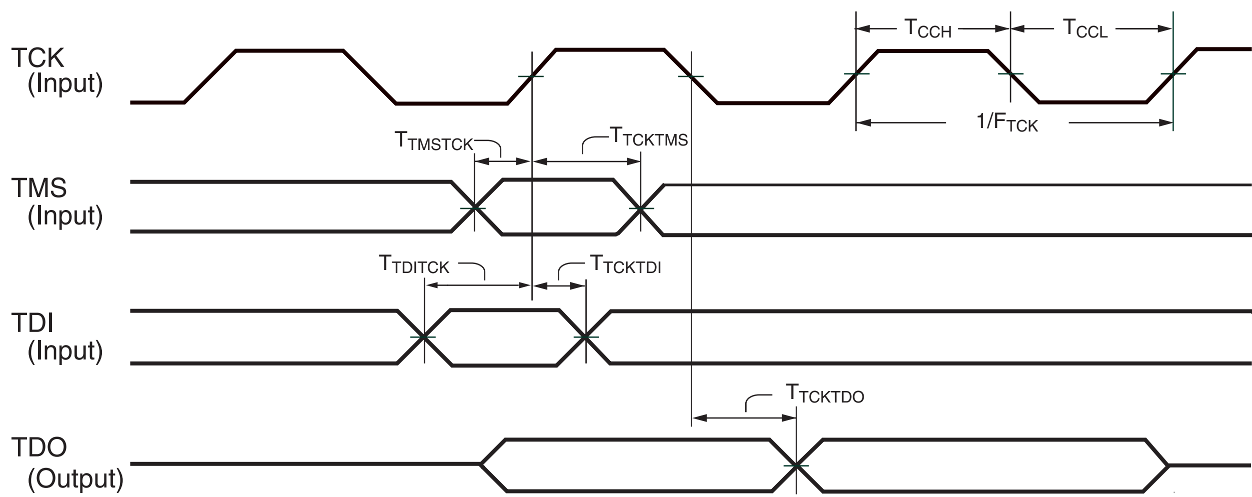

Figure 18: **JTAG Waveforms**

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Table 64: **Maximum User I/O by Package**

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF [1]	CLK	N.C.
XC3S50AN	TQG144	108	7	50	42	2	26	8	30	0
	FTG256	144	32	64	53	20	26	15	30	51
XC3S200AN	FTG256	195	35	90	69	21	52	21	32	0
XC3S400AN	FTG256	195	35	90	69	21	52	21	32	0
	FGG400	311	63	142	155	46	52	26	32	0
XC3S700AN	FGG484	372	84	165	194	61	52	33	32	3
XC3S1400AN	FGG484	375	87	165	195	62	52	34	32	0
	FGG676	502	94	227	313	67	52	38	32	17

Notes:
1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and foot-prints are available for download from the Xilinx website at:

http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip

Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

Package Overview

Table 65 shows the five low-cost, space-saving production package styles for the Spartan-3AN family.

Table 65: **Spartan-3AN Family Package Options**

Package	Leads	Type	Maximum I/Os	Lead Pitch (mm)	Body Area (mm)	Height (mm)
TQ144/TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	20 x 20	1.60
FT256/FTG256	256	Fine-pitch Thin Ball Grid Array (FBGA)	195	1.0	17 x 17	1.55
FG400/FGG400	400	Fine-pitch Ball Grid Array (FBGA)	311	1.0	21 x 21	2.43
FG484/FGG484	484	Fine-pitch Ball Grid Array (FBGA)	375	1.0	23 x 23	2.60
FG676/FGG676	676	Fine-pitch Ball Grid Array (FBGA)	502	1.0	27 x 27	2.60

Notes:
1. For mass, refer to the MDDS files (see Table 66).

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra “G” in the package style name. For example, the standard “CS484” package becomes “CSG484” when ordered as the Pb-free option. Leaded (Pb) packages are available for selected devices, with the same pinout and without the “G” in the ordering code; See Table 5, page 7 for more information. The mechanical dimensions of the Pb and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 66.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx website at the specified location in Table 66.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx website for each package.

Table 66: **Xilinx Package Documentation**

Package	Drawing	MDDS
TQ144	Package Drawing	PK169_TQ144
TQG144		PK461_TQG144
FT256	Package Drawing	PK158_FT256
FTG256		PK424_FTG256
FG400	Package Drawing	PK182_FG400
FGG400		PK108_FGG400
FG484	Package Drawing	PK183_FG484
FGG484		PK110_FGG484
FG676	Package Drawing	PK155_FG676
FGG676		PK394_FGG676

Package Thermal Characteristics

The power dissipated by an FPGA application has implications on package selection and system design. The power consumed by a Spartan-3AN FPGA is reported using either the XPower Power Estimator or the XPower Analyzer calculator integrated in the Xilinx® ISE® development software. Table 67 provides the thermal characteristics for the various Spartan-3AN FPGA packages. This information is also available using the Thermal Query tool at http://www.xilinx.com/cgi-bin/thermal/thermal.pl.

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the junction temperature per watt of power consumption. The junction-to-board (θ_{JB}) value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 67: **Spartan-3AN FPGA Package Thermal Characteristics**

Device	Package[1]	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
XC3S50AN	TQG144	13.4	32.8	38.9	32.8	32.5	31.7	°C/Watt
	FTG256							°C/Watt
XC3S200AN	FTG256	7.4	23.3	29.0	23.8	23.0	22.3	°C/Watt
XC3S400AN	FTG256							°C/Watt
	FGG400	6.2	12.9	22.5	16.7	15.6	15.0	°C/Watt
XC3S700AN	FGG484	5.3	11.5	19.4	15.0	13.9	13.4	°C/Watt
XC3S1400AN	FGG484							°C/Watt
	FGG676	4.3	10.9	17.7	13.7	12.6	12.1	°C/Watt

Notes:

1. Thermal characteristics are similar for leaded (non-Pb-free) packages.
2. Use the Thermal Query tool at http://www.xilinx.com/cgi-bin/thermal/thermal.pl for specific device information.

Table 70: **Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN)** ***(Cont'd)***

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
2	IP_2	IP_2	L7	INPUT
2	IP_2	IP_2	L8	INPUT
2	IP_2/VREF_2	IP_2/VREF_2	L9	VREF
2	IP_2/VREF_2	IP_2/VREF_2	L10	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M8	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	IP_2/VREF_2	N5	VREF
2	VCCO_2	VCCO_2	M9	VCCO
2	VCCO_2	VCCO_2	R4	VCCO
2	VCCO_2	VCCO_2	R8	VCCO
2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	C1	I/O
3	IO_L01P_3	IO_L01P_3	C2	I/O
3	IO_L02N_3	IO_L02N_3	D3	I/O
3	IO_L02P_3	IO_L02P_3	D4	I/O
3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	D1	I/O
3	N.C.	IO_L05N_3	E2	I/O
3	N.C.	IO_L05P_3	E3	I/O
3	N.C.	IO_L07N_3	G4	I/O
3	N.C.	IO_L07P_3	F3	I/O
3	IO_L08N_3/VREF_3	IO_L08N_3/VREF_3	G1	VREF
3	IO_L08P_3	IO_L08P_3	F1	I/O
3	N.C.	IO_L09N_3	H4	I/O
3	N.C.	IO_L09P_3	G3	I/O
3	N.C.	IO_L10N_3	H5	I/O
3	N.C.	IO_L10P_3	H6	I/O
3	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	H1	LHCLK
3	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	G2	LHCLK
3	IO_L12N_3/IRDY2/LHCLK3	IO_L12N_3/IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	H3	LHCLK
3	IO_L14N_3/LHCLK5	IO_L14N_3/LHCLK5	J1	LHCLK
3	IO_L14P_3/LHCLK4	IO_L14P_3/LHCLK4	J2	LHCLK
3	IO_L15N_3/LHCLK7	IO_L15N_3/LHCLK7	K1	LHCLK
3	IO_L15P_3/TRDY2/LHCLK6	IO_L15P_3/TRDY2/LHCLK6	K3	LHCLK
3	N.C.	IO_L16N_3	L2	I/O
3	N.C.	IO_L16P_3/VREF_3	L1	VREF
3	N.C.	IO_L17N_3	J6	I/O
3	N.C.	IO_L17P_3	J4	I/O

Table 73: **FTG256 XC3S50AN Footprint Migration/Differences *(Cont'd)***

FTG256 Ball	Bank	XC3S50AN	Migration	XC3S200AN or XC3S400AN
K13	1	N.C.	→	I/O
L1	3	N.C.	→	I/O/VREF
L2	3	N.C.	→	I/O
L3	3	N.C.	→	I/O
L4	3	N.C.	→	I/O
L13	1	N.C.	→	I/O
L14	1	N.C.	→	I/O
L16	1	N.C.	→	I/O
M3	3	N.C.	→	I/O
M10	2	N.C.	→	I/O
M13	1	N.C.	→	I/O
M14	1	N.C.	→	I/O/VREF
M15	1	N.C.	→	I/O
M16	1	N.C.	→	I/O
N7	2	N.C.	→	I/O
N10	2	N.C.	→	I/O
N12	2	N.C.	→	I/O
P6	2	N.C.	→	I/O
P13	2	N.C.	→	I/O
R7	2	N.C.	→	I/O
T7	2	N.C.	→	I/O
Number of Differences:			52	

FGG400 Footprint

Left Half of FGG400 Package (Top View)

Count	Type	Description
155	**I/O:**	Unrestricted, general-purpose user I/O
46	**INPUT:**	Unrestricted, general-purpose input pin
51	**DUAL:**	Configuration pins, then possible user I/O
26	**VREF:**	User I/O or input voltage reference for bank
32	**CLK:**	User I/O, input, or clock buffer input
2	**CONFIG:**	Dedicated configuration pins
4	**JTAG:**	Dedicated JTAG port pins
2	**SUSPEND:**	Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
43	**GND:**	Ground
22	**VCCO:**	Output voltage supply for bank
9	**VCCINT:**	Internal core supply voltage (+1.2V)
8	**VCCAUX:**	Auxiliary supply voltage

Bank 0 (top), Bank 3 (left), Bank 2 (bottom)

	1	2	3	4	5	6	7	8	9	10
A	GND	I/O L32P_0 VREF_0	I/O L30P_0	I/O L29P_0	I/O L26P_0	I/O L25P_0	I/O L24N_0	I/O L18N_0 GCLK11	I/O L18P_0 GCLK10	I/O L16P_0 GCLK6
B	I/O L02P_3	I/O L32N_0 PUDC_B	I/O L30N_0	VCCO_0	I/O L26N_0	GND	I/O L24P_0	I/O L20P_0	I/O L19P_0	VCCO_0
C	I/O L03P_3	I/O L02N_3	GND	I/O L29N_0	I/O L28P_0	I/O L25N_0	I/O L21P_0	I/O L20N_0	I/O L19N_0	I/O L16N_0 GCLK7
D	I/O L05P_3	I/O L03N_3	I/O L01N_3	I/O L01P_3	PROG_B	I/O L28N_0	VCCO_0	I/O L21N_0	GND	I/O L17P_0 GCLK8
E	I/O L05N_3	VCCO_3	I/O L10P_3	TMS	GND	I/O L31P_0	I/O L27P_0	I/O L23P_0	I/O L22P_0	I/O L17N_0 GCLK9
F	I/O L13P_3	I/O L10N_3	I/O L09P_3	I/O L06P_3	TDI	I/O L31N_0	I/O L27N_0	I/O L23N_0	I/O L22N_0 VREF_0	VCCO_0
G	I/O L13N_3 VREF_3	GND	I/O L12P_3	I/O L09N_3	I/O L06N_3	INPUT L04N_3 VREF_3	INPUT L04P_3	INPUT	INPUT	INPUT
H	VCCAUX	I/O L12N_3	I/O L14N_3	I/O L08N_3	VCCO_3	I/O L08P_3	INPUT	GND	INPUT	INPUT
J	I/O L17P_3 LHCLK0	I/O L16N_3	I/O L16P_3	I/O L14P_3	I/O L07N_3	I/O L07P_3	INPUT L11N_3 VREF_3	INPUT L11P_3	GND	VCCINT
K	GND	I/O L17N_3 LHCLK1	I/O L18P_3 LHCLK2	I/O L20P_3 LHCLK4	INPUT L19N_3	INPUT L19P_3	INPUT L15N_3	INPUT L15P_3	VCCINT	GND
L	I/O L21P_3 TRDY2 LHCLK6	VCCO_3	I/O L18N_3 IRDY2 LHCLK3	GND	I/O L20N_3 LHCLK5	INPUT L23N_3	INPUT L23P_3	VCCAUX	GND	VCCINT
M	I/O L21N_3 LHCLK7	I/O L22P_3 VREF_3	I/O L22N_3	I/O L24P_3	I/O L24N_3	INPUT L31P_3	INPUT L27N_3	INPUT L27P_3	VCCINT	GND
N	I/O L25P_3	I/O L25N_3	I/O L26P_3	I/O L26N_3	VCCO_3	INPUT L35N_3	INPUT L31N_3	GND	INPUT VREF_2	VCCINT
P	I/O L28P_3	GND	I/O L29P_3	I/O L29N_3	INPUT L35P_3	INPUT L39P_3	INPUT L39N_3 VREF_3	INPUT VREF_2	INPUT	INPUT VREF_2
R	I/O L28N_3	I/O L30P_3	I/O L30N_3	I/O L33N_3	I/O L36P_3	GND	I/O L04N_2	INPUT	GND	INPUT
T	I/O L32P_3 VREF_3	I/O L32N_3	I/O L33P_3	I/O L36N_3	VCCAUX	I/O L04P_2	I/O L06P_2	I/O L07P_2 RDWR_B	I/O L11P_2	I/O L14N_2 D4
U	I/O L34P_3	VCCO_3	I/O L34N_3	I/O L01P_2 M1	I/O L05N_2	I/O L06N_2	I/O L07N_2 VS2	VCCO_2	I/O L11N_2	I/O L14P_2 D5
V	I/O L37P_3	I/O L37N_3	GND	I/O L01N_2 M0	I/O L05P_2	I/O L09P_2 VS1	I/O L12P_2 D7	I/O L13P_2	I/O L13N_2	I/O L16P_2 GCLK14
W	I/O L38P_3	I/O L38N_3	I/O L02P_2 M2	I/O L03N_2	VCCO_2	I/O L09N_2 VS0	GND	I/O L12N_2 D6	I/O L15P_2 GCLK12	I/O L16N_2 GCLK15
Y	GND	I/O L02N_2 CSO_B	I/O L03P_2	I/O L08P_2	I/O L08N_2	I/O L10P_2	I/O L10N_2	VCCAUX	I/O L15N_2 GCLK13	GND

DS529-4_03_011608

Figure 22: **FGG400 Package Footprint (Top View)**

Right Half of FGG400 Package (Top View)

Bank 0 (top), Bank 1 (right), Bank 2 (bottom)

	11	12	13	14	15	16	17	18	19	20
A	GND	I/O L13N_0	VCCAUX	I/O L07N_0	I/O L08N_0	I/O L05N_0	I/O L04N_0	I/O L01N_0	TCK	GND
B	I/O L14P_0	I/O L13P_0	I/O L11P_0	GND	I/O L08P_0	VCCO_0	I/O L04P_0 VREF_0	I/O L01P_0	I/O L38N_1 A25	I/O L38P_1 A24
C	I/O L14N_0	I/O L11N_0	I/O L10N_0 VREF_0	I/O L07P_0	I/O L06N_0	I/O L05P_0	I/O L02N_0	GND	I/O L37N_1 A23	I/O L37P_1 A22
D	I/O L15P_0 GCLK4	I/O L12P_0	VCCO_0	I/O L10P_0	I/O L06P_0	I/O L03P_0	I/O L02P_0 VREF_0	I/O L34N_1	VCCO_1	I/O L34P_1
E	I/O L15N_0 GCLK5	GND	I/O L09P_0	INPUT	I/O L03N_0	VCCAUX	TDO	I/O L33P_1	I/O L32N_1	I/O L32P_1
F	INPUT	I/O L12N_0	I/O L09N_0	INPUT	GND	I/O L36N_1 A21	I/O L33N_1	I/O L30N_1 A19	I/O L29N_1 A17	I/O L29P_1 A16
G	INPUT VREF_0	INPUT	INPUT	INPUT L39N_1	INPUT L39P_1 VREF_1	I/O L36P_1 A20	I/O L30P_1 A18	I/O L28P_1	GND	I/O L26N_1 A15
H	INPUT	INPUT	GND	INPUT L35N_1	INPUT L35P_1	VCCO_1	I/O L28N_1	I/O L25N_1 A13	I/O L25P_1 A12	I/O L26P_1 A14
J	GND	VCCINT	INPUT L31N_1	INPUT L31P_1 VREF_1	INPUT L27N_1	INPUT L27P_1	I/O L24P_1	I/O L22N_1 A11	I/O L22P_1 A10	I/O L21N_1 RHCLK7
K	VCCINT	GND	VCCAUX	INPUT L23N_1	INPUT L23P_1 VREF_1	I/O L24N_1	GND	I/O L20P_1 RHCLK4	VCCO_1	I/O L21P_1 IRDY1 RHCLK6
L	GND	VCCINT	INPUT L19N_1	INPUT L19P_1	I/O L16P_1 A8	I/O L16N_1 A9	I/O L20N_1 RHCLK5	I/O L18N_1 TRDY1 RHCLK3	I/O L18P_1 RHCLK2	GND
M	VCCINT	GND	INPUT L15N_1	INPUT L15P_1 VREF_1	INPUT L11N_1 VREF_1	INPUT L11P_1	I/O L14P_1 A6	I/O L14N_1 A7	I/O L17P_1 RHCLK0	I/O L17N_1 RHCLK1
N	GND	INPUT VREF_2	GND	INPUT VREF_1	I/O L12P_1 A2	VCCO_1	I/O L12N_1 A3	I/O L13P_1 A4	I/O L13N_1 A5	VCCAUX
P	INPUT VREF_2	INPUT	INPUT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L07P_1	I/O L07N_1	I/O L10P_1	GND	I/O L10N_1 VREF_1
R	VCCO_2	I/O L19N_2	I/O L23N_2	INPUT VREF_2	SUSPEND	I/O L03N_1 A1	I/O L08N_1	I/O L08P_1	I/O L09P_1	I/O L09N_1
T	INPUT	I/O L19P_2	I/O L23P_2	I/O L25N_2	I/O L27N_2	GND	I/O L03P_1 A0	I/O L05P_1	VCCO_1	I/O L05N_1
U	I/O L18P_2 GCLK2	GND	I/O L22P_2 AWAKE	VCCO_2	I/O L27P_2	I/O L29N_2	I/O L31N_2	I/O L02N_1 LDC0	I/O L06P_1	I/O L06N_1
V	I/O L17N_2 GCLK1	I/O L18N_2 GCLK3	I/O L22N_2 DOUT	I/O L25P_2	I/O L26N_2 D1	I/O L29P_2	I/O L31P_2	GND	I/O L02P_1 LDC1	I/O L01N_1 LDC2
W	VCCO_2	I/O L20N_2 MOSI CSI_B	I/O L21N_2	I/O L24N_2 D3	GND	I/O L28N_2	VCCO_2	I/O L32P_2 D0 DIN/MISO	DONE	I/O L01P_1 HDC
Y	I/O L17P_2 GCLK0	I/O L20P_2	I/O L21P_2	I/O L24P_2 INIT_B	I/O L26P_2 D2	I/O L28P_2	I/O L30P_2	I/O L30N_2	I/O L32N_2 CCLK	GND

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Figure 22: **FGG400 Package Footprint (Top View)**

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
0	IO_L33N_0	B10	I/O
0	IO_L33P_0	A10	I/O
0	IO_L34N_0	D10	I/O
0	IO_L34P_0	C10	I/O
0	IO_L35N_0	H12	I/O
0	IO_L35P_0	G12	I/O
0	IO_L36N_0	B9	I/O
0	IO_L36P_0	A9	I/O
0	IO_L37N_0	D9	I/O
0	IO_L37P_0	E10	I/O
0	IO_L38N_0	B8	I/O
0	IO_L38P_0	A8	I/O
0	IO_L39N_0	K12	I/O
0	IO_L39P_0	J12	I/O
0	IO_L40N_0	D8	I/O
0	IO_L40P_0	C8	I/O
0	IO_L41N_0	C6	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L42P_0	B7	I/O
0	IO_L43N_0	K11	I/O
0	IO_L43P_0	J11	I/O
0	IO_L44N_0	D6	I/O
0	IO_L44P_0	C5	I/O
0	IO_L45N_0	B4	I/O
0	IO_L45P_0	A4	I/O
0	IO_L46N_0	H10	I/O
0	IO_L46P_0	G10	I/O
0	IO_L47N_0	H9	I/O
0	IO_L47P_0	G9	I/O
0	IO_L48N_0	E7	I/O
0	IO_L48P_0	F7	I/O
0	IO_L51N_0	B3	I/O
0	IO_L51P_0	A3	I/O
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L52P_0/VREF_0	F8	VREF
0	IP_0	A5	INPUT
0	IP_0	A7	INPUT
0	IP_0	A13	INPUT
0	IP_0	A17	INPUT

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
0	IP_0	A23	INPUT
0	IP_0	C4	INPUT
0	IP_0	D12	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	E11	INPUT
0	IP_0	E18	INPUT
0	IP_0	E20	INPUT
0	IP_0	F10	INPUT
0	IP_0	G14	INPUT
0	IP_0	G16	INPUT
0	IP_0	H13	INPUT
0	IP_0	H18	INPUT
0	IP_0	J10	INPUT
0	IP_0	J13	INPUT
0	IP_0	J15	INPUT
0	IP_0/VREF_0	D7	VREF
0	IP_0/VREF_0	D14	VREF
0	IP_0/VREF_0	G11	VREF
0	IP_0/VREF_0	J17	VREF
0	N.C.	A24	N.C.
0	N.C.	B24	N.C.
0	N.C.	D5	N.C.
0	N.C.	E9	N.C.
0	N.C.	F18	N.C.
0	N.C.	E6	N.C.
0	N.C.	F9	N.C.
0	N.C.	G18	N.C.
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device. Noted that family is available in Pb-free packages only.
09/12/07	2.0.1	Minor updates to text.
09/24/07	2.1	Update thermal characteristics in Table 67.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that non-Pb-free packages may be available for selected devices. Updated thermal characteristics in Table 67. Updated links.
06/02/08	3.1	Add Package Overview section. Removed VREF and INPUT designations and diamond symbols on unconnected N.C. pins for XC3S700AN FGG484 in Table 78 and Figure 22 and for XC3S1400AN FGG676 in Table 82 and Figure 23.
11/19/09	3.2	Renamed package ‘Footprint Area’ to ‘Body Area’ throughout document. Noted in Introduction that references to Pb-free package code also apply to the Pb package. Added Pb packages to Table 65 and Table 66. Changed Body Area of TQ144/TQG144 packages in Table 65. Corrected bank designation for SUSPEND to VCCAUX. Noted that non-Pb-free (Pb) packages are available for selected devices. Updated Table 79 and Figure 22 for I/O vs. Input pin counts.
12/02/10	4.0	Upgraded Notice of Disclaimer.
04/01/11	4.1	Updated the CLK description in Table 62. In Table 64, added device/package combinations for the XC3S50AN and XC3S400AN in the FT(G)256 package and the XC3S1400AN in the FG(G)484 package. In Table 65, updated the maximum I/Os for the FG484/FGG484 packages, removed the Mass column, and updated Note 1. In Table 65, changed the FTG256 link from PK115_FTG256, FGG676 link from PK111_FGG676, and the TQG144 link from PK126_TQG144. Completely replaced the section FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array with new information on the added device/package combinations and new figures and tables. Revised U16, U7, and T8 in Table 78. Added Table 80 and Table 81 and updated Figure 23.