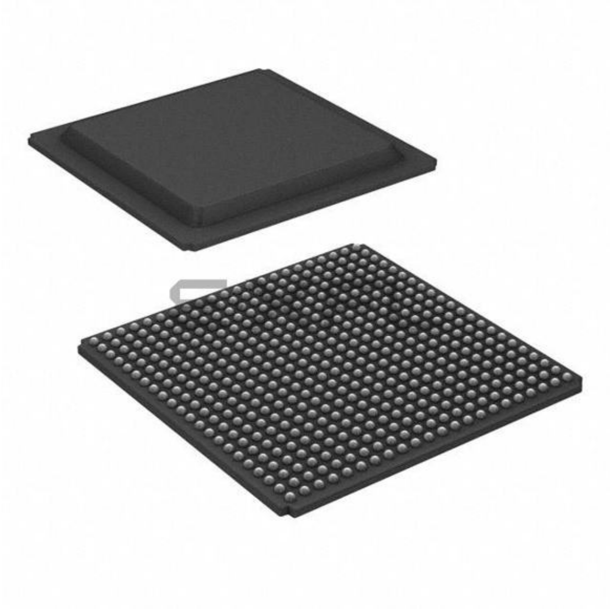
AMD Xilinx - XC3S700AN-4FGG484C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	1472
Number of Logic Elements/Cells	13248
Total RAM Bits	368640
Number of I/O	372
Number of Gates	700000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s700an-4fgg484c

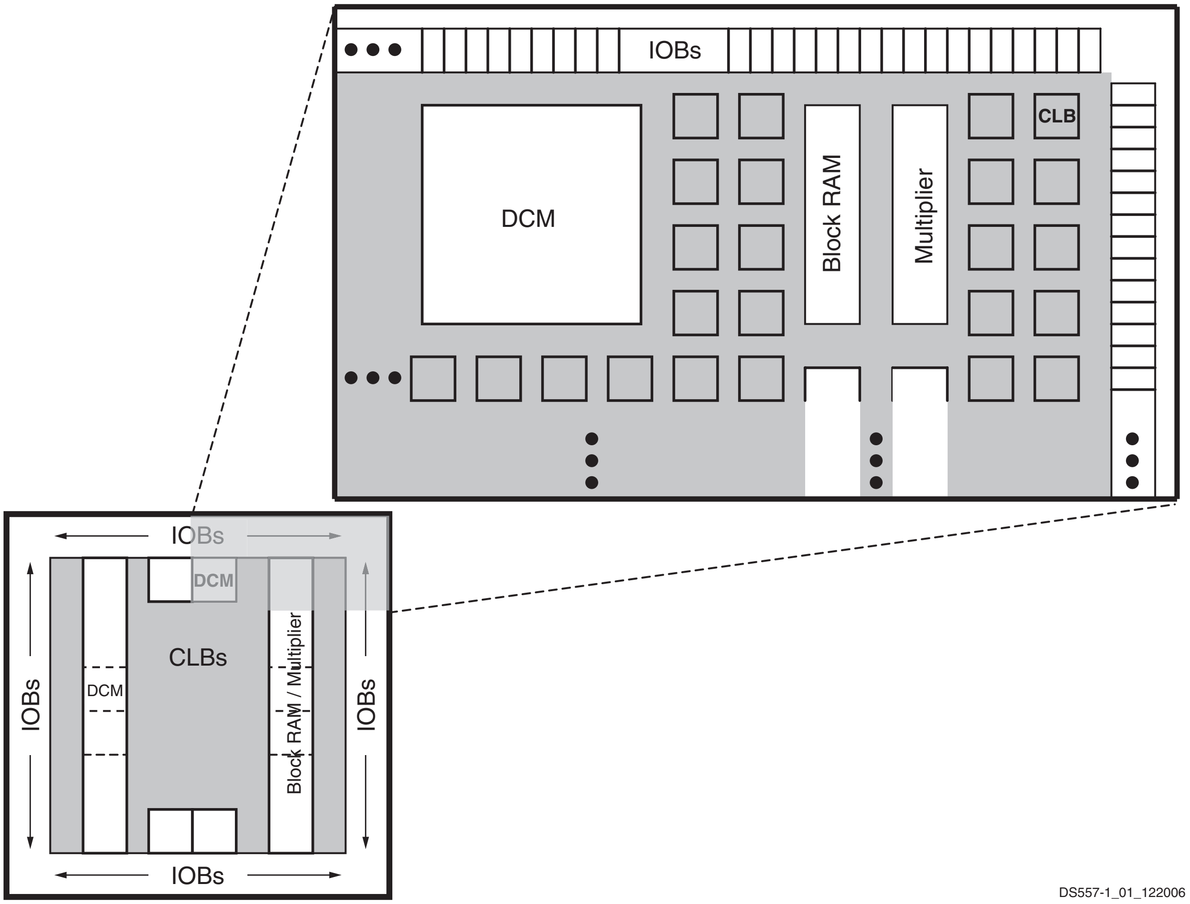
Architectural Overview

The Spartan-3AN FPGA architecture is compatible with that of the Spartan-3A FPGA. The architecture consists of five fundamental programmable functional elements:

- **Configurable Logic Blocks (CLBs)** contain flexible Look-Up Tables (LUTs) that implement logic plus storage elements used as flip-flops or latches.
- **Input/Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. IOBs support bidirectional data flow plus 3-state operation. They support a variety of signal standards, including several high-performance differential standards. Double Data-Rate (DDR) registers are included.
- **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
- **Multiplier Blocks** accept two 18-bit binary numbers as inputs and calculate the product.
- **Digital Clock Manager (DCM) Blocks** provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

These elements are organized as shown in Figure 1. A dual ring of staggered IOBs surrounds a regular array of CLBs. Each device has two columns of block RAM except for the XC3S50AN, which has one column. Each RAM column consists of several 18-Kbit RAM blocks. Each block RAM is associated with a dedicated multiplier. The DCMs are positioned in the center with two at the top and two at the bottom of the device. The XC3S50AN has DCMs only at the top, while the XC3S700AN and XC3S1400AN add two DCMs in the middle of the two columns of block RAM and multipliers.

The Spartan-3AN FPGA features a rich network of traces that interconnect all five functional elements, transmitting signals among them. Each functional element has an associated switch matrix that permits multiple connections to the routing.



Notes:

1. The XC3S700AN and XC3S1400AN have two additional DCMs on both the left and right sides as indicated by the dashed lines. The XC3S50AN has only two DCMs at the top and only one Block RAM/Multiplier column.

Figure 1: **Spartan-3AN Family Architecture**

- Sector-based data protection and security features
  - Sector Protect: Write- and erase-protect a sector (changeable)
  - Sector Lockdown: Sector data is unchangeable (permanent)
- 128-byte Security Register
  - Separate from FPGA's unique Device DNA identifier
  - 64-byte factory-programmed identifier unique to the in-system Flash memory
  - 64-byte one-time programmable, user-programmable field
- 100,000 Program/Erase cycles
- 20-year data retention
- Comprehensive programming support
  - In-system prototype programming via JTAG using Xilinx Platform Cable USB and iMPACT software
  - Product programming support using BPM Microsystems programmers with appropriate programming adapter
  - Design examples demonstrating in-system programming from a Spartan-3AN FPGA application

I/O Capabilities

The Spartan-3AN FPGA SelectIO interface supports many popular single-ended and differential standards. Table 4 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional, input-only pins as indicated in Table 4.

Spartan-3AN FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3AN FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 4: **Available User I/Os and Differential (Diff) I/O Pairs**

Package(1)	**TQ144 TQG144**		**FT256 FTG256**		**FG400 FGG400**		**FG484 FGG484**		**FG676 FGG676**	
Body Size (mm)	**20 x 20**(2)		**17 x 17**		**21 x 21**		**23 x 23**		**27 x 27**	
Device(3)	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**	**User**	**Diff**
XC3S50AN	**108**(4) *(7)*	**50** *(24)*	**144** *(32)*	**64** *(32)*	–	–	–	–	–	–
XC3S200AN	–	–	**195** *(35)*	**90** *(50)*	–	–	–	–	–	–
XC3S400AN	–	–	**195** *(35)*	**90** *(50)*	**311** *(63)*	**142** *(78)*	–	–	–	–
XC3S700AN	–	–	–	–	–	–	**372** *(84)*	**165** *(93)*	–	–
XC3S1400AN	–	–	–	–	–	–	**375** *(87)*	**165** *(93)*	**502** *(94)*	**227** *(131)*

Notes:

1. See Pb and Pb-Free Packaging, page 7 for details on Pb and Pb-free packaging options.
2. The footprint for the TQ(G)144 (22 mm x 22 mm) package is larger than the package body.
3. Each Spartan-3AN FPGA has a pin-compatible Spartan-3A FPGA equivalent, although Spartan-3A FPGAs do not have internal SPI flash and offer more part/package combinations.
4. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (*italics*) indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

Spartan-3AN FPGA Family: Functional Description

DS557 (v4.1) April 1, 2011

Product Specification

Spartan-3AN FPGA Design Documentation

The functionality of the Spartan®-3AN FPGA family is described in the following documents. The topics covered in each guide are listed below:

- **DS706: Extended Spartan-3A Family Overview**
- **UG331: Spartan-3 Generation FPGA User Guide**
  - Clocking Resources
  - Digital Clock Managers (DCMs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
    - Distributed RAM
    - SRL16 Shift Registers
    - Carry and Arithmetic Logic
  - I/O Resources
  - Embedded Multiplier Blocks
  - Programmable Interconnect
  - ISE® Design Tools
  - IP Cores
  - Embedded Processing and Control Solutions
  - Pin Types and Package Overview
  - Package Drawings
  - Powering FPGAs
  - Power Management
- **UG332: Spartan-3 Generation Configuration User Guide**
  - Configuration Overview
    - Configuration Pins and Behavior
    - Bitstream Sizes
  - Detailed Descriptions by Mode
    - Master Serial Mode using Xilinx® Platform Flash
    - Master SPI Mode using SPI Serial Flash PROM
    - Internal Master SPI Mode
    - Master BPI Mode using Parallel NOR Flash
    - Slave Parallel (SelectMAP) using a Processor
    - Slave Serial using a Processor
    - JTAG Mode
  - ISE iMPACT Programming Examples
  - MultiBoot Reconfiguration
  - Design Authentication using Device DNA
- **UG333: Spartan-3AN FPGA In-System Flash User Guide**
  - For FPGA applications that write to or read from the In-System Flash memory after configuration
  - SPI_ACCESS interface
  - In-System Flash memory architecture
  - Read, program, and erase commands
  - Status registers
  - Sector Protection and Sector Lockdown features
  - Security Register with Unique Identifier

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Spartan-3AN FPGA Starter Kit

For specific hardware examples, please see the Spartan-3AN FPGA Starter Kit board web page, which has links to various design examples and the user guide.

- **Spartan-3AN FPGA Starter Kit Board Page**
  http://www.xilinx.com/s3anstarter
- **UG334: Spartan-3AN FPGA Starter Kit User Guide**

Table 15: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards *(Cont'd)***

IOSTANDARD Attribute	V_{CCO} for Drivers(1)			V_{ID}			V_{ICM}(2)		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
DIFF_SSTL3_II(8)	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the “Using I/O Resources” chapter in UG331.
4. See External Termination Requirements for Differential I/O, page 22.
5. LVPECL is supported on inputs only, not outputs. Requires $V_{CCAUX} = 3.3V \pm 10\%$.
6. LVPECL_33 maximum $V_{ICM} = V_{CCAUX} - (V_{ID} / 2)$
7. Requires $V_{CCAUX} = 3.3V \pm 10\%$ for inputs. $(V_{CCAUX} - 300\text{ mV}) \leq V_{ICM} \leq (V_{CCAUX} - 37\text{ mV})$
8. V_{REF} inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The V_{REF} settings are the same as for the single-ended versions in Table 13. Other differential standards do not use V_{REF}.
9. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the “Using I/O Resources” chapter in UG331.

Differential Output Pairs

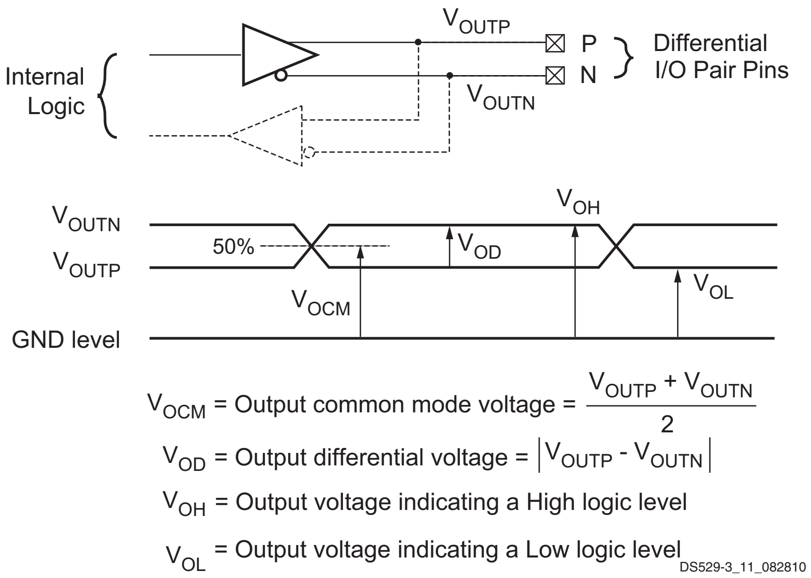


Figure 7: **Differential Output Voltages**

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

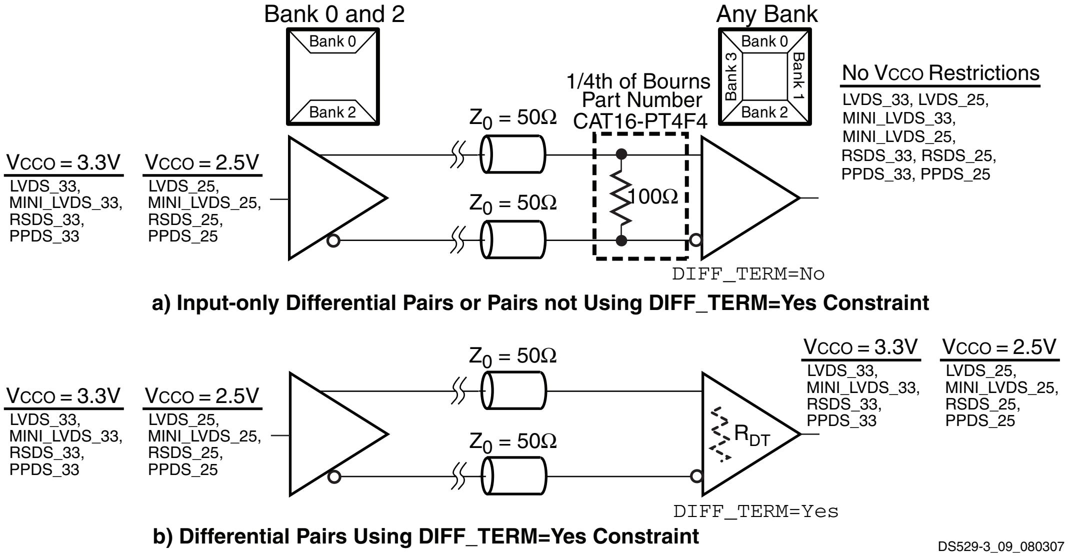


Figure 8: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

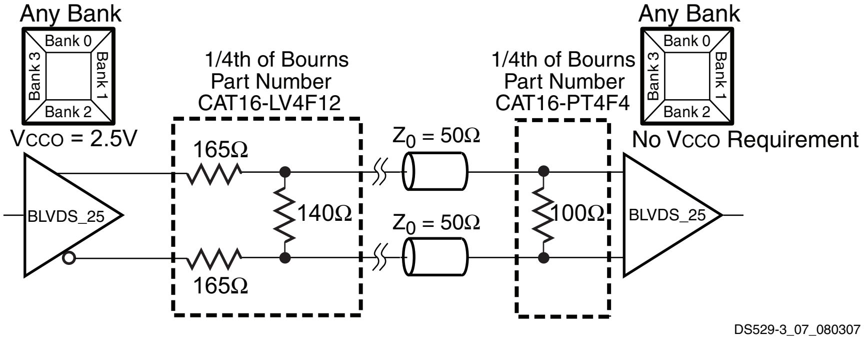


Figure 9: **External Output and Input Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

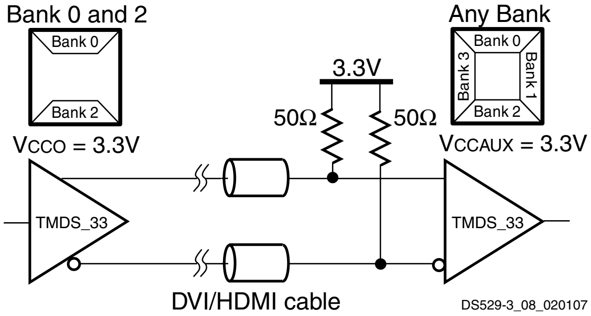


Figure 10: **External Input Resistors Required for TMDS_33 I/O Standard**

Pin-to-Pin Setup and Hold Times

Table 22: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade		Units
				-5	-4	
				Min	Min	
Setup Times						
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50AN	2.45	2.68	ns
			XC3S200AN	2.59	2.84	ns
			XC3S400AN	2.38	2.68	ns
			XC3S700AN	2.38	2.57	ns
			XC3S1400AN	1.91	2.17	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 5, without DCM	XC3S50AN	2.55	2.76	ns
			XC3S200AN	2.32	2.76	ns
			XC3S400AN	2.21	2.60	ns
			XC3S700AN	2.28	2.63	ns
			XC3S1400AN	2.33	2.41	ns
Hold Times						
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XC3S50AN	–0.36	–0.36	ns
			XC3S200AN	–0.52	–0.52	ns
			XC3S400AN	–0.33	–0.29	ns
			XC3S700AN	–0.17	–0.12	ns
			XC3S1400AN	–0.07	0.00	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 5, without DCM	XC3S50AN	–0.63	–0.58	ns
			XC3S200AN	–0.56	–0.56	ns
			XC3S400AN	–0.42	–0.42	ns
			XC3S700AN	–0.80	–0.75	ns
			XC3S1400AN	–0.69	–0.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 26. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 26. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Setup and Hold Times

Table 23: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
Setup Times							
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25[(2)]	0	XC3S50AN	1.56	1.58	ns
				XC3S200AN	1.71	1.81	ns
				XC3S400AN	1.30	1.51	ns
				XC3S700AN	1.34	1.51	ns
				XC3S1400AN	1.36	1.74	ns
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25[(2)]	1	XC3S50AN	2.16	2.18	ns
			2		3.10	3.12	ns
			3		3.51	3.76	ns
			4		4.04	4.32	ns
			5		3.88	4.24	ns
			6		4.72	5.09	ns
			7		5.47	5.94	ns
			8		5.97	6.52	ns
			1	XC3S200AN	2.05	2.20	ns
			2		2.72	2.93	ns
			3		3.38	3.78	ns
			4		3.88	4.37	ns
			5		3.69	4.20	ns
			6		4.56	5.23	ns
			7		5.34	6.11	ns
			8		5.85	6.71	ns
			1	XC3S400AN	1.79	2.02	ns
			2		2.43	2.67	ns
			3		3.02	3.43	ns
			4		3.49	3.96	ns
			5		3.41	3.95	ns
			6		4.20	4.81	ns
			7		4.96	5.66	ns
			8		5.44	6.19	ns

Table 23: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	IFD_ DELAY_ VALUE	Device	Speed Grade		Units
					-5	-4	
					Min	Min	
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25[(2)]	1	XC3S700AN	1.82	1.95	ns
			2		2.62	2.83	ns
			3		3.32	3.72	ns
			4		3.83	4.31	ns
			5		3.69	4.14	ns
			6		4.60	5.19	ns
			7		5.39	6.10	ns
			8		5.92	6.73	ns
			1	XC3S1400AN	1.79	2.17	ns
			2		2.55	2.92	ns
			3		3.38	3.76	ns
			4		3.75	4.32	ns
			5		3.81	4.19	ns
			6		4.39	5.09	ns
			7		5.16	5.98	ns
			8		5.69	6.57	ns
Hold Times							
T_{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25[(3)]	0	XC3S50AN	–0.66	–0.64	ns
				XC3S200AN	–0.85	–0.65	ns
				XC3S400AN	–0.42	–0.42	ns
				XC3S700AN	–0.81	–0.67	ns
				XC3S1400AN	–0.71	–0.71	ns
$T_{IOICKPD}$	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25[(3)]	1	XC3S50AN	–0.88	–0.88	ns
			2		–1.33	–1.33	ns
			3		–2.05	–2.05	ns
			4		–2.43	–2.43	ns
			5		–2.34	–2.34	ns
			6		–2.81	–2.81	ns
			7		–3.03	–3.03	ns
			8		–3.83	–3.57	ns
			1	XC3S200AN	–1.51	–1.51	ns
			2		–2.09	–2.09	ns
			3		–2.40	–2.40	ns
			4		–2.68	–2.68	ns
			5		–2.56	–2.56	ns
			6		–2.99	–2.99	ns
			7		–3.29	–3.29	ns
			8		–3.61	–3.61	ns

Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair** ***(Cont'd)***

Signal Standard (IOSTANDARD)			**Package Type**			
			TQG144		**FTG256, FGG400, FGG484, FGG676**	
			Top, Bottom Banks 0,2	**Left, Right Banks 1,3**	**Top, Bottom Banks 0,2**	**Left, Right Banks 1,3**
LVCMOS12	Slow	2	17	17	40	40
		4	–	13	–	25
		6	–	10	–	18
	Fast	2	12	9	31	31
		4	–	9	–	13
		6	–	9	–	9
	QuietIO	2	36	36	55	55
		4	–	33	–	36
		6	–	27	–	36
PCI33_3			9	9	16	16
PCI66_3			–	9	–	13
HSTL_I			–	11	–	20
HSTL_III			–	7	–	8
HSTL_I_18			13	13	17	17
HSTL_II_18			–	5	–	5
HSTL_III_18			8	8	10	8
SSTL18_I			7	13	7	15
SSTL18_II			–	9	–	9
SSTL2_I			10	10	18	18
SSTL2_II			–	6	–	9
SSTL3_I			7	8	8	10
SSTL3_II			5	6	6	7
Differential Standards (Number of I/O *Pairs* or Channels)						
LVDS_25			8	–	22	–
LVDS_33			8	–	27	–
BLVDS_25			1	1	4	4
MINI_LVDS_25			8	–	22	–
MINI_LVDS_33			8	–	27	–
LVPECL_25			Input Only			
LVPECL_33			Input Only			
RSDS_25			8	–	22	–
RSDS_33			8	–	27	–
TMDS_33			8	–	27	–
PPDS_25			8	–	22	–

Table 32: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}-GND Pair** ***(Cont'd)***

Signal Standard (IOSTANDARD)	**Package Type**			
	TQG144		**FTG256, FGG400, FGG484, FGG676**	
	Top, Bottom Banks 0,2	**Left, Right Banks 1,3**	**Top, Bottom Banks 0,2**	**Left, Right Banks 1,3**
PPDS_33	8	–	27	–
DIFF_HSTL_I	–	5	–	10
DIFF_HSTL_III	–	3	–	4
DIFF_HSTL_I_18	6	6	8	8
DIFF_HSTL_II_18	–	2	–	2
DIFF_HSTL_III_18	4	4	5	4
DIFF_SSTL18_I	3	6	3	7
DIFF_SSTL18_II	–	4	–	4
DIFF_SSTL2_I	5	5	9	9
DIFF_SSTL2_II	–	3	–	4
DIFF_SSTL3_I	3	4	4	5
DIFF_SSTL3_II	2	3	3	3

Notes:

1. Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMDS, are only supported in top or bottom banks (I/O banks 0 and 2). Refer to UG331: *Spartan-3 Generation FPGA User Guide* for additional information.
2. The numbers in this table are recommendations that assume sound board lay out practice. Test limits are the V_{IL}/V_{IH} voltage limits for the respective I/O standard.
3. If more than one signal standard is assigned to the I/Os of a given bank, refer to XAPP689: *Managing Ground Bounce in Large FPGAs* for information on how to perform weighted average SSO calculations.

Digital Clock Manager (DCM) Timing

For specification purposes, the DCM consists of three key components: the Delay-Locked Loop (DLL), the Digital Frequency Synthesizer (DFS), and the Phase Shifter (PS).

Aspects of DLL operation play a role in all DCM applications. All such applications inevitably use the CLKIN and the CLKFB inputs connected to either the CLK0 or the CLK2X feedback, respectively. Thus, specifications in the DLL tables (Table 39 and Table 40) apply to any application that only employs the DLL component. When the DFS and/or the PS components are used together with the DLL, then the specifications listed in the DFS and PS tables (Table 41 through Table 44) supersede any corresponding ones in the DLL tables. DLL specifications that do not change with the addition of DFS or PS functions are presented in Table 39 and Table 40.

Period jitter and cycle-cycle jitter are two of many different ways of specifying clock jitter. Both specifications describe statistical variation from a mean value.

Period jitter is the worst-case deviation from the ideal clock period over a collection of millions of samples. In a histogram of period jitter, the mean value is the clock period.

Cycle-cycle jitter is the worst-case difference in clock period between adjacent clock cycles in the collection of clock periods sampled. In a histogram of cycle-cycle jitter, the mean value is zero.

Spread Spectrum

DCMs accept typical spread spectrum clocks as long as they meet the input requirements. The DLL will track the frequency changes created by the spread spectrum clock to drive the global clocks to the FPGA logic. See XAPP469: *Spread-Spectrum Clocking Reception for Displays* for details.

Delay-Locked Loop (DLL)

Table 39: **Recommended Operating Conditions for the DLL**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges								
F_{CLKIN}	CLKIN_FREQ_DLL	Frequency of the CLKIN clock input		5[2]	280[3]	5[2]	250[3]	MHz
Input Pulse Requirements								
CLKIN_PULSE		CLKIN pulse width as a percentage of the CLKIN period	$F_{CLKIN} \leq 150$ MHz	40%	60%	40%	60%	%
			$F_{CLKIN} > 150$ MHz	45%	55%	45%	55%	%
Input Clock Jitter Tolerance and Delay Path Variation[4]								
CLKIN_CYC_JITT_DLL_LF		Cycle-to-cycle jitter at the CLKIN input	$F_{CLKIN} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_DLL_HF			$F_{CLKIN} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_DLL		Period jitter at the CLKIN input		–	±1	–	±1	ns
CLKFB_DELAY_VAR_EXT		Allowable variation of off-chip feedback delay from the DCM output to the CLKFB input		–	±1	–	±1	ns

Notes:

1. DLL specifications apply when any of the DLL outputs (CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, or CLKDV) are in use.
2. The DFS, when operating independently of the DLL, supports lower FCLKIN frequencies. See Table 41.
3. The CLKIN_DIVIDE_BY_2 attribute can be used to increase the effective input frequency range up to F_{BUFG}. When set to TRUE, CLKIN_DIVIDE_BY_2 divides the incoming clock frequency by two as it enters the DCM.
4. CLKIN input jitter beyond these limits might cause the DCM to lose lock.
5. The DCM specifications are guaranteed when both adjacent DCMs are locked.

Table 40: **Switching Characteristics for the DLL *(Cont'd)***

Symbol	Description	Device	Speed Grade				Units
			-5		-4		
			Min	Max	Min	Max	
Delay Lines							
DCM_DELAY_STEP(5)	Finest delay resolution, average over all taps	All	15	35	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 10 and Table 39.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250 ps.
5. The typical delay step size is 23 ps.

Digital Frequency Synthesizer (DFS)

Table 41: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade				Units
				-5		-4		
				Min	Max	Min	Max	
Input Frequency Ranges(2)								
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333(3)	0.200	333(3)	MHz
Input Clock Jitter Tolerance(4)								
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) are used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 39.
3. To support double the maximum effective FCLKIN limit, set the CLKIN_DIVIDE_BY_2 attribute to TRUE. This attribute divides the incoming clock frequency by two as it enters the DCM.
4. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Suspend Mode Timing

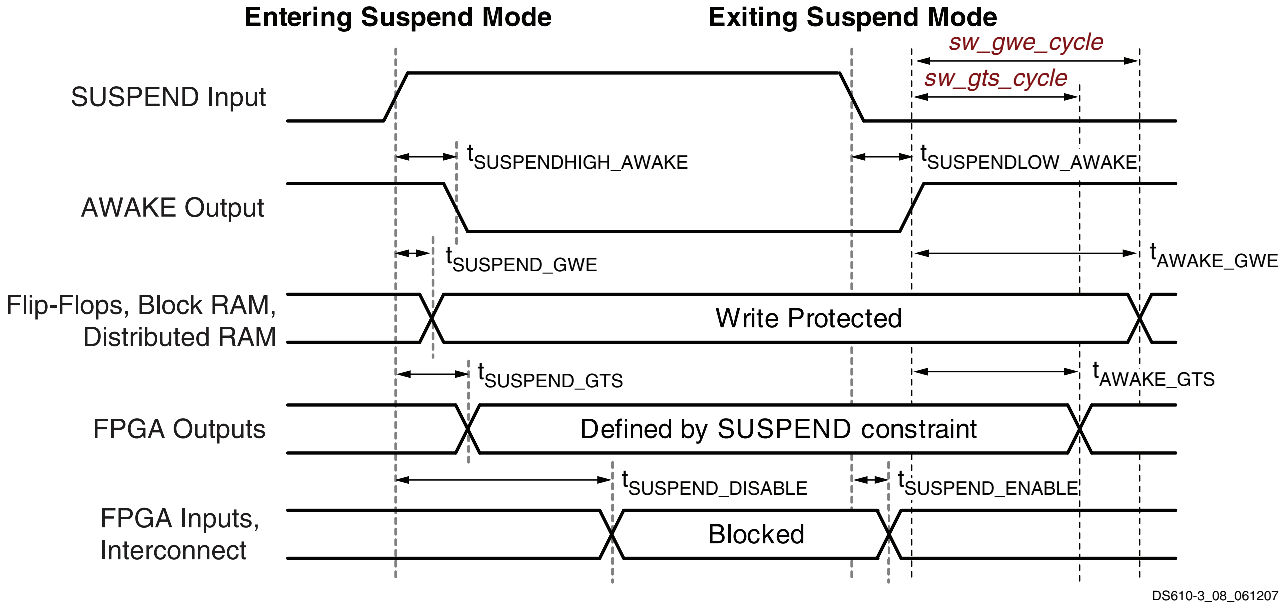


Figure 12: **Suspend Mode Timing**

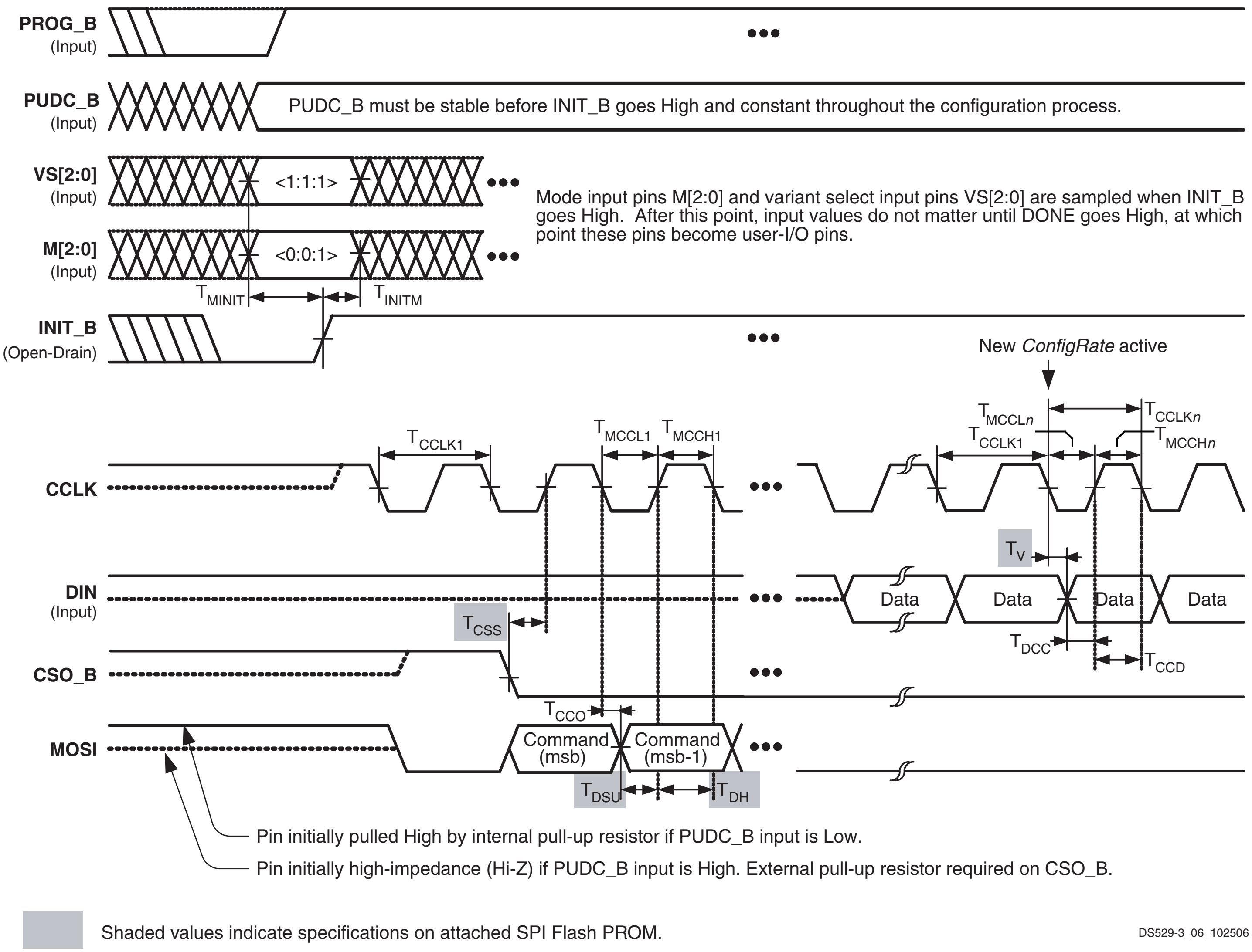
Table 49: **Suspend Mode Timing Parameters**

Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***)	–	7	–	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***)	+160	+300	+600	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	< 5	–	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–	ns
Exiting Suspend Mode					
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin Does not include DCM lock time	–	4 to 108	–	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1***	–	67	–	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512***	–	14	–	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1***	–	57	–	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512***	–	14	–	µs

Notes:

1. These parameters based on characterization.
2. For information on using the Spartan-3AN Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

External Serial Peripheral Interface (SPI) Configuration Timing



Pin initially pulled High by internal pull-up resistor if PUDC_B input is Low.

Pin initially high-impedance (Hi-Z) if PUDC_B input is High. External pull-up resistor required on CSO_B.

▨ Shaded values indicate specifications on attached SPI Flash PROM.

Figure 16: **Waveforms for External Serial Peripheral Interface (SPI) Configuration**

Table 57: **Timing for External Serial Peripheral Interface (SPI) Configuration Mode**

Symbol	Description	Minimum	Maximum	Units
T_{CCLK1}	Initial CCLK clock period	See Table 51		
$T_{CCLK\mathit{n}}$	CCLK clock period after FPGA loads ***ConfigRate*** bitstream option setting	See Table 51		
T_{MINIT}	Setup time on VS[2:0] variant-select pins and M[2:0] mode pins before the rising edge of INIT_B	50	–	ns
T_{INITM}	Hold time on VS[2:0] variant-select pins and M[2:0] mode pins after the rising edge of INIT_B	0	–	ns
T_{CCO}	MOSI output valid delay after CCLK falling clock edge	See Table 55		
T_{DCC}	Setup time on the DIN data input before CCLK rising clock edge	See Table 55		
T_{CCD}	Hold time on the DIN data input after CCLK rising clock edge	See Table 55		

Spartan-3AN FPGA Family: Pinout Descriptions

DS557 (v4.1) April 1, 2011 **Product Specification**

Introduction

This section describes how the various pins on a Spartan®-3AN FPGA connect within the supported component packages, and provides device-specific thermal characteristics. For general information on the pin functions and the package characteristics, see the Packaging section of UG331:

- **UG331: Spartan-3 Generation FPGA User Guide**
  http://www.xilinx.com/support/documentation/user_guides/ug331.pdf

Spartan-3AN FPGAs are available in Pb-free, RoHS packages, indicated by a "G" in the middle of the package code. Leaded (Pb) packages are available for selected devices, with the same pinout and without the "G" in the ordering code (see Table 5, page 7). The Pb-free package code can be selected in the software for the Pb packages since the pinouts are identical. References to the Pb-free package code in this document apply also to the Pb package.

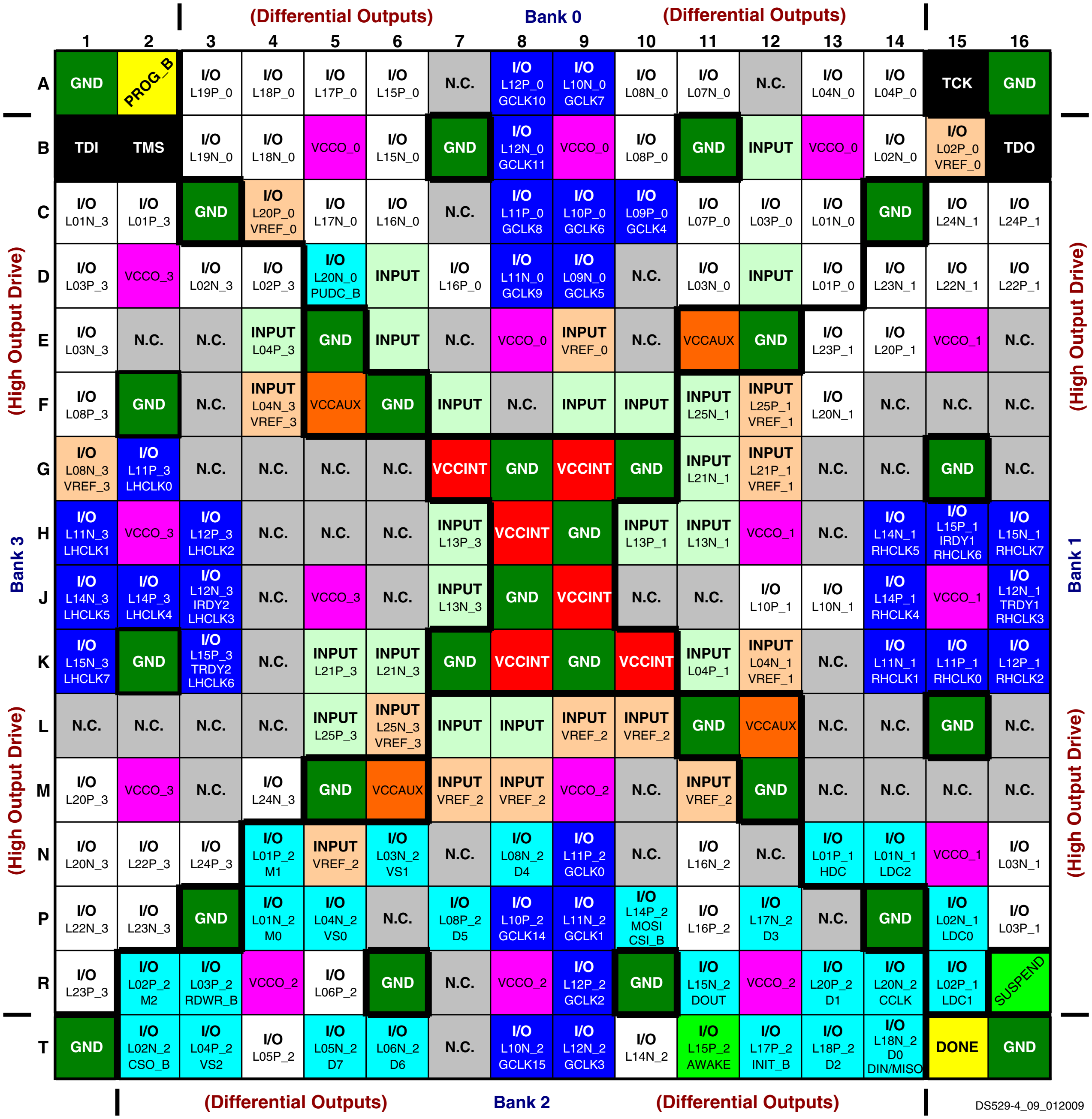
Pin Types

Most pins on a Spartan-3AN FPGA are general-purpose, user-defined I/O pins. There are, however, up to 12 different functional types of pins on Spartan-3AN FPGA packages, as outlined in Table 62. In the package footprint drawings that follow, the individual pins are color-coded according to pin type as in the table.

Table 62: **Types of Pins on Spartan-3AN FPGAs**

Type with Color Code	Description	Pin Name(s) in Type[(1)]
I/O	Unrestricted, general-purpose user-I/O pin. Most pins can be paired together to form differential I/Os.	IO_# IO_Lxxy_#
INPUT	Unrestricted, general-purpose input-only pin. This pin does not have an output structure, differential termination resistor, or PCI™ clamp diode.	IP_# IP_Lxxy_#
DUAL	Dual-purpose pin used in some configuration modes during the configuration process and then usually available as a user I/O after configuration. If the pin is not used during configuration, this pin behaves as an I/O-type pin. See UG332: *Spartan-3 Generation Configuration User Guide* for additional information on these signals.	M[2:0] PUDC_B CCLK MOSI/CSI_B D[7:1] D0/DIN DOUT CSO_B RDWR_B INIT_B A[25:0] VS[2:0] LDC[2:0] HDC
VREF	Dual-purpose pin that is either a user-I/O pin or Input-only pin, or, along with all other VREF pins in the same bank, provides a reference voltage input for certain I/O standards. If used for a reference voltage within a bank, all VREF pins within the bank must be connected.	IP/VREF_# IP_Lxx_#/VREF_# IO/VREF_# IO_Lxx_#/VREF_#
CLK	Either a user-I/O pin or an input to a specific clock buffer driver. Most packages have 16 global clock inputs that optionally clock the entire device. The exceptions are all devices in the TQG144 package and the XC3S50AN in the FTG256 package. The RHCLK inputs optionally clock the right half of the device. The LHCLK inputs optionally clock the left half of the device. See the Using Global Clock Resources chapter in UG331: *Spartan-3 Generation FPGA User Guide* for additional information on these signals.	IO_Lxx_#/GCLK[15:0], IO_Lxx_#/LHCLK[7:0], IO_Lxx_#/RHCLK[7:0]

FTG256 Footprint (XC3S50AN)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	N.C.	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	N.C.	I/O L04N_0	I/O L04P_0	TCK	GND
B	TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	INPUT	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO
C	I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	N.C.	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1	I/O L24P_1
D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	INPUT	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	N.C.	I/O L03N_0	INPUT	I/O L01P_0	I/O L23N_1	I/O L22N_1	I/O L22P_1
E	I/O L03N_3	N.C.	N.C.	INPUT L04P_3	GND	INPUT	N.C.	VCCO_0	INPUT VREF_0	N.C.	VCCAUX	GND	I/O L23P_1	I/O L20P_1	VCCO_1	N.C.
F	I/O L08P_3	GND	N.C.	INPUT L04N_3 VREF_3	VCCAUX	GND	INPUT	N.C.	INPUT	INPUT	INPUT L25N_1	INPUT L25P_1 VREF_1	I/O L20N_1	N.C.	N.C.	N.C.
G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	N.C.	N.C.	N.C.	N.C.	VCCINT	GND	VCCINT	GND	INPUT L21N_1	INPUT L21P_1 VREF_1	N.C.	N.C.	GND	N.C.
H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	N.C.	N.C.	N.C.	INPUT L13P_3	VCCINT	GND	INPUT L13P_1	INPUT L13N_1	VCCO_1	N.C.	I/O L14N_1 RHCLK5	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7
J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	N.C.	VCCO_3	N.C.	INPUT L13N_3	GND	VCCINT	N.C.	N.C.	I/O L10P_1	I/O L10N_1	I/O L14P_1 RHCLK4	VCCO_1	I/O L12N_1 TRDY1 RHCLK3
K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	N.C.	INPUT L21P_3	INPUT L21N_3	GND	VCCINT	GND	VCCINT	INPUT L04P_1	INPUT L04N_1 VREF_1	N.C.	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2
L	N.C.	N.C.	N.C.	N.C.	INPUT L25P_3	INPUT L25N_3 VREF_3	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	GND	VCCAUX	N.C.	N.C.	GND	N.C.
M	I/O L20P_3	VCCO_3	N.C.	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	INPUT VREF_2	VCCO_2	N.C.	INPUT VREF_2	GND	N.C.	N.C.	N.C.	N.C.
N	I/O L20N_3	I/O L22P_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L03N_2 VS1	N.C.	I/O L08N_2 D4	I/O L11P_2 GCLK0	N.C.	I/O L16N_2	N.C.	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1
P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	N.C.	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14P_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	N.C.	GND	I/O L02N_1 LDC0	I/O L03P_1
R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L06P_2	GND	N.C.	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L20P_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND
T	GND	I/O L02N_2 CSO_B	I/O L04P_2 VS2	I/O L05P_2	I/O L05N_2 D7	I/O L06N_2 D6	N.C.	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14N_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L18N_2 D0 DIN/MISO	DONE	GND

Figure 20: **XC3S50AN FTG256 Package Footprint (Top View)**

53 **I/O:** Unrestricted, general-purpose user I/O

20 **INPUT:** Unrestricted, general-purpose input pin

2 **CONFIG:** Dedicated configuration pins

51 **N.C.:** Not connected (XC3S50AN only)

25 **DUAL:** Configuration pins, then possible user I/O

30 **CLK:** User I/O, input, or global buffer input

4 **JTAG:** Dedicated JTAG port pins

28 **GND:** Ground

15 **VREF:** User I/O or input voltage reference for bank

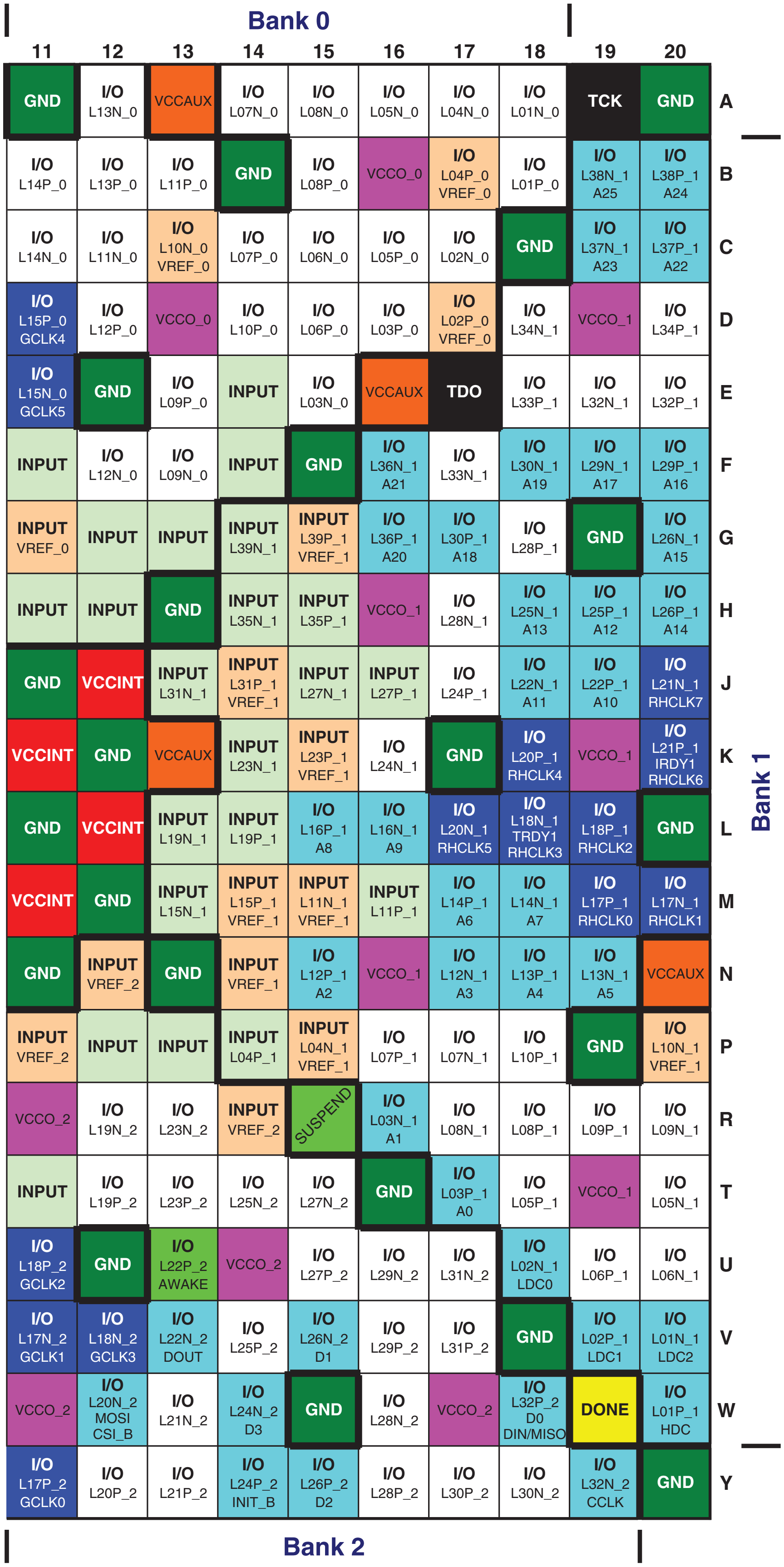
16 **VCCO:** Output voltage supply for bank

6 **VCCINT:** Internal core supply voltage (+1.2V)

4 **VCCAUX:** Auxiliary supply voltage

2 **SUSPEND:** Dedicated SUSPEND and dual-purpose AWAKE Power Management pins

Right Half of FGG400 Package (Top View)



11	12	13	14	15	16	17	18	19	20	
GND	I/O L13N_0	VCCAUX	I/O L07N_0	I/O L08N_0	I/O L05N_0	I/O L04N_0	I/O L01N_0	TCK	GND	A
I/O L14P_0	I/O L13P_0	I/O L11P_0	GND	I/O L08P_0	VCCO_0	I/O L04P_0 VREF_0	I/O L01P_0	I/O L38N_1 A25	I/O L38P_1 A24	B
I/O L14N_0	I/O L11N_0	I/O L10N_0 VREF_0	I/O L07P_0	I/O L06N_0	I/O L05P_0	I/O L02N_0	GND	I/O L37N_1 A23	I/O L37P_1 A22	C
I/O L15P_0 GCLK4	I/O L12P_0	VCCO_0	I/O L10P_0	I/O L06P_0	I/O L03P_0	I/O L02P_0 VREF_0	I/O L34N_1	VCCO_1	I/O L34P_1	D
I/O L15N_0 GCLK5	GND	I/O L09P_0	INPUT	I/O L03N_0	VCCAUX	TDO	I/O L33P_1	I/O L32N_1	I/O L32P_1	E
INPUT	I/O L12N_0	I/O L09N_0	INPUT	GND	I/O L36N_1 A21	I/O L33N_1	I/O L30N_1 A19	I/O L29N_1 A17	I/O L29P_1 A16	F
INPUT VREF_0	INPUT	INPUT	INPUT L39N_1	INPUT L39P_1 VREF_1	I/O L36P_1 A20	I/O L30P_1 A18	I/O L28P_1	GND	I/O L26N_1 A15	G
INPUT	INPUT	GND	INPUT L35N_1	INPUT L35P_1	VCCO_1	I/O L28N_1	I/O L25N_1 A13	I/O L25P_1 A12	I/O L26P_1 A14	H
GND	VCCINT	INPUT L31N_1	INPUT L31P_1 VREF_1	INPUT L27N_1	INPUT L27P_1	I/O L24P_1	I/O L22N_1 A11	I/O L22P_1 A10	I/O L21N_1 RHCLK7	J
VCCINT	GND	VCCAUX	INPUT L23N_1	INPUT L23P_1 VREF_1	I/O L24N_1	GND	I/O L20P_1 RHCLK4	VCCO_1	I/O L21P_1 IRDY1 RHCLK6	K
GND	VCCINT	INPUT L19N_1	INPUT L19P_1	I/O L16P_1 A8	I/O L16N_1 A9	I/O L20N_1 RHCLK5	I/O L18N_1 TRDY1 RHCLK3	I/O L18P_1 RHCLK2	GND	L
VCCINT	GND	INPUT L15N_1	INPUT L15P_1 VREF_1	INPUT L11N_1 VREF_1	INPUT L11P_1	I/O L14P_1 A6	I/O L14N_1 A7	I/O L17P_1 RHCLK0	I/O L17N_1 RHCLK1	M
GND	INPUT VREF_2	GND	INPUT VREF_1	I/O L12P_1 A2	VCCO_1	I/O L12N_1 A3	I/O L13P_1 A4	I/O L13N_1 A5	VCCAUX	N
INPUT VREF_2	INPUT	INPUT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L07P_1	I/O L07N_1	I/O L10P_1	GND	I/O L10N_1 VREF_1	P
VCCO_2	I/O L19N_2	I/O L23N_2	INPUT VREF_2	SUSPEND	I/O L03N_1 A1	I/O L08N_1	I/O L08P_1	I/O L09P_1	I/O L09N_1	R
INPUT	I/O L19P_2	I/O L23P_2	I/O L25N_2	I/O L27N_2	GND	I/O L03P_1 A0	I/O L05P_1	VCCO_1	I/O L05N_1	T
I/O L18P_2 GCLK2	GND	I/O L22P_2 AWAKE	VCCO_2	I/O L27P_2	I/O L29N_2	I/O L31N_2	I/O L02N_1 LDC0	I/O L06P_1	I/O L06N_1	U
I/O L17N_2 GCLK1	I/O L18N_2 GCLK3	I/O L22N_2 DOUT	I/O L25P_2	I/O L26N_2 D1	I/O L29P_2	I/O L31P_2	GND	I/O L02P_1 LDC1	I/O L01N_1 LDC2	V
VCCO_2	I/O L20N_2 MOSI CSI_B	I/O L21N_2	I/O L24N_2 D3	GND	I/O L28N_2	VCCO_2	I/O L32P_2 D0 DIN/MISO	DONE	I/O L01P_1 HDC	W
I/O L17P_2 GCLK0	I/O L20P_2	I/O L21P_2	I/O L24P_2 INIT_B	I/O L26P_2 D2	I/O L28P_2	I/O L30P_2	I/O L30N_2	I/O L32N_2 CCLK	GND	Y

Figure 22: **FGG400 Package Footprint (Top View)**

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
2	IO_L10N_2	AB7	I/O
2	IO_L10P_2	Y7	I/O
2	IO_L11N_2/VS0	Y8	DUAL
2	IO_L11P_2/VS1	W8	DUAL
2	IO_L12N_2	AB8	I/O
2	IO_L12P_2	AA8	I/O
2	IO_L13N_2	Y10	I/O
2	IO_L13P_2	V10	I/O
2	IO_L14N_2/D6	AB9	DUAL
2	IO_L14P_2/D7	Y9	DUAL
2	IO_L15N_2	AB10	I/O
2	IO_L15P_2	AA10	I/O
2	IO_L16N_2/D4	AB11	DUAL
2	IO_L16P_2/D5	Y11	DUAL
2	IO_L17N_2/GCLK13	V11	GCLK
2	IO_L17P_2/GCLK12	U11	GCLK
2	IO_L18N_2/GCLK15	Y12	GCLK
2	IO_L18P_2/GCLK14	W12	GCLK
2	IO_L19N_2/GCLK1	AB12	GCLK
2	IO_L19P_2/GCLK0	AA12	GCLK
2	IO_L20N_2/GCLK3	U12	GCLK
2	IO_L20P_2/GCLK2	V12	GCLK
2	IO_L21N_2	Y13	I/O
2	IO_L21P_2	AB13	I/O
2	IO_L22N_2/MOSI/CSI_B	AB14	DUAL
2	IO_L22P_2	AA14	I/O
2	IO_L23N_2	Y14	I/O
2	IO_L23P_2	W13	I/O
2	IO_L24N_2/DOUT	AA15	DUAL
2	IO_L24P_2/AWAKE	AB15	PWR MGMT
2	IO_L25N_2	Y15	I/O
2	IO_L25P_2	W15	I/O
2	IO_L26N_2/D3	U13	DUAL
2	IO_L26P_2/INIT_B	V13	DUAL
2	IO_L27N_2	Y16	I/O
2	IO_L27P_2	AB16	I/O
2	IO_L28N_2/D1	Y17	DUAL
2	IO_L28P_2/D2	AA17	DUAL
2	IO_L29N_2	AB18	I/O
2	IO_L29P_2	AB17	I/O

Table 78: **Spartan-3AN FGG484 Pinout *(Cont'd)***

Bank	Pin Name	FGG484 Ball	Type
2	IO_L30N_2	V15	I/O
2	IO_L30P_2	V14	I/O
2	IO_L31N_2	V16	I/O
2	IO_L31P_2	W16	I/O
2	IO_L32N_2	AA19	I/O
2	IO_L32P_2	AB19	I/O
2	IO_L33N_2	V17	I/O
2	IO_L33P_2	W18	I/O
2	IO_L34N_2	W17	I/O
2	IO_L34P_2	Y18	I/O
2	IO_L35N_2	AA21	I/O
2	IO_L35P_2	AB21	I/O
2	IO_L36N_2/CCLK	AA20	DUAL
2	IO_L36P_2/D0/DIN/MISO	AB20	DUAL
2	IP_2	P12	INPUT
2	IP_2	R10	INPUT
2	IP_2	R11	INPUT
2	IP_2	R9	INPUT
2	IP_2	T13	INPUT
2	IP_2	T14	INPUT
2	IP_2	T9	INPUT
2	IP_2	U10	INPUT
2	IP_2	U15	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ◆	U16	INPUT
2	XC3S1400AN: IP_2 XC3S700AN: N.C. ◆	U7	INPUT
2	IP_2	U8	INPUT
2	IP_2	V7	INPUT
2	IP_2/VREF_2	R12	VREF
2	IP_2/VREF_2	R13	VREF
2	IP_2/VREF_2	R14	VREF
2	IP_2/VREF_2	T10	VREF
2	IP_2/VREF_2	T11	VREF
2	IP_2/VREF_2	T15	VREF
2	IP_2/VREF_2	T16	VREF
2	IP_2/VREF_2	T7	VREF
2	XC3S1400AN: IP_2/VREF_2 XC3S700AN: N.C. ◆	T8	VREF
2	IP_2/VREF_2	V8	VREF

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
2	IP_2	AD9	INPUT
2	IP_2	AD10	INPUT
2	IP_2	AD16	INPUT
2	IP_2	AF2	INPUT
2	IP_2	AF7	INPUT
2	IP_2	Y11	INPUT
2	IP_2/VREF_2	AA9	VREF
2	IP_2/VREF_2	AA20	VREF
2	IP_2/VREF_2	AB6	VREF
2	IP_2/VREF_2	AB10	VREF
2	IP_2/VREF_2	AC10	VREF
2	IP_2/VREF_2	AD12	VREF
2	IP_2/VREF_2	AF15	VREF
2	IP_2/VREF_2	AF17	VREF
2	IP_2/VREF_2	AF22	VREF
2	IP_2/VREF_2	Y16	VREF
2	N.C.	AA8	N.C.
2	N.C.	AC5	N.C.
2	N.C.	AC22	N.C.
2	N.C.	AD5	N.C.
2	N.C.	Y18	N.C.
2	N.C.	Y19	N.C.
2	N.C.	AD23	N.C.
2	N.C.	W18	N.C.
2	N.C.	Y8	N.C.
2	VCCO_2	AB8	VCCO
2	VCCO_2	AB14	VCCO
2	VCCO_2	AB19	VCCO
2	VCCO_2	AE5	VCCO
2	VCCO_2	AE11	VCCO
2	VCCO_2	AE16	VCCO
2	VCCO_2	AE22	VCCO
2	VCCO_2	W11	VCCO
2	VCCO_2	W16	VCCO
3	IO_L01N_3	J9	I/O
3	IO_L01P_3	J8	I/O
3	IO_L02N_3	B1	I/O
3	IO_L02P_3	B2	I/O
3	IO_L03N_3	H7	I/O
3	IO_L03P_3	G6	I/O

Table 82: **Spartan-3AN FGG676 Pinout *(Cont'd)***

Bank	Pin Name	FGG676 Ball	Type
3	IO_L05N_3	K8	I/O
3	IO_L05P_3	K9	I/O
3	IO_L06N_3	E4	I/O
3	IO_L06P_3	D3	I/O
3	IO_L07N_3	F4	I/O
3	IO_L07P_3	E3	I/O
3	IO_L09N_3	G4	I/O
3	IO_L09P_3	F5	I/O
3	IO_L10N_3	H6	I/O
3	IO_L10P_3	J7	I/O
3	IO_L11N_3	F2	I/O
3	IO_L11P_3	E1	I/O
3	IO_L13N_3	J6	I/O
3	IO_L13P_3	K7	I/O
3	IO_L14N_3	F3	I/O
3	IO_L14P_3	G3	I/O
3	IO_L15N_3	L9	I/O
3	IO_L15P_3	L10	I/O
3	IO_L17N_3	H1	I/O
3	IO_L17P_3	H2	I/O
3	IO_L18N_3	L7	I/O
3	IO_L18P_3	K6	I/O
3	IO_L19N_3	J4	I/O
3	IO_L19P_3	J5	I/O
3	IO_L21N_3	M9	I/O
3	IO_L21P_3	M10	I/O
3	IO_L22N_3	K4	I/O
3	IO_L22P_3	K5	I/O
3	IO_L23N_3	K2	I/O
3	IO_L23P_3	K3	I/O
3	IO_L25N_3	L3	I/O
3	IO_L25P_3	L4	I/O
3	IO_L26N_3	M7	I/O
3	IO_L26P_3	M8	I/O
3	IO_L27N_3	M3	I/O
3	IO_L27P_3	M4	I/O
3	IO_L28N_3	M6	I/O
3	IO_L28P_3	M5	I/O
3	IO_L29N_3/VREF_3	M1	VREF
3	IO_L29P_3	M2	I/O

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device. Noted that family is available in Pb-free packages only.
09/12/07	2.0.1	Minor updates to text.
09/24/07	2.1	Update thermal characteristics in Table 67.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that non-Pb-free packages may be available for selected devices. Updated thermal characteristics in Table 67. Updated links.
06/02/08	3.1	Add Package Overview section. Removed VREF and INPUT designations and diamond symbols on unconnected N.C. pins for XC3S700AN FGG484 in Table 78 and Figure 22 and for XC3S1400AN FGG676 in Table 82 and Figure 23.
11/19/09	3.2	Renamed package 'Footprint Area' to 'Body Area' throughout document. Noted in Introduction that references to Pb-free package code also apply to the Pb package. Added Pb packages to Table 65 and Table 66. Changed Body Area of TQ144/TQG144 packages in Table 65. Corrected bank designation for SUSPEND to VCCAUX. Noted that non-Pb-free (Pb) packages are available for selected devices. Updated Table 79 and Figure 22 for I/O vs. Input pin counts.
12/02/10	4.0	Upgraded Notice of Disclaimer.
04/01/11	4.1	Updated the CLK description in Table 62. In Table 64, added device/package combinations for the XC3S50AN and XC3S400AN in the FT(G)256 package and the XC3S1400AN in the FG(G)484 package. In Table 65, updated the maximum I/Os for the FG484/FGG484 packages, removed the Mass column, and updated Note 1. In Table 65, changed the FTG256 link from PK115_FTG256, FGG676 link from PK111_FGG676, and the TQG144 link from PK126_TQG144. Completely replaced the section FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array with new information on the added device/package combinations and new figures and tables. Revised U16, U7, and T8 in Table 78. Added Table 80 and Table 81 and updated Figure 23.

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