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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1472
Number of Logic Elements/Cells	13248
Total RAM Bits	368640
Number of I/O	372
Number of Gates	700000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc3s700an-4fgg484i

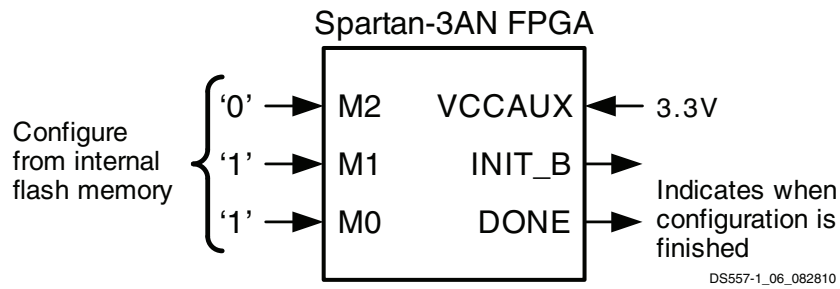


Figure 2: Spartan-3AN FPGA Configuration Interface from Internal SPI Flash Memory

Configuration

Spartan-3AN FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored on-chip in nonvolatile Flash memory, or externally in a PROM or some other nonvolatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of seven different modes:

- Configure from internal SPI Flash memory (Figure 2)
 - Completely self-contained
 - Reduced board space
 - Easy-to-use configuration interface
- Master Serial from a Xilinx Platform Flash PROM
- Serial Peripheral Interface (SPI) from an external industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary-Scan (JTAG), typically downloaded from a processor or system tester

The MultiBoot feature stores multiple configuration files in the on-chip Flash, providing extended life with field upgrades. MultiBoot also supports multiple system solutions with a single board to minimize inventory and simplify the addition of new features, even in the field. Flexibility is maintained to do additional MultiBoot configurations via the external configuration method.

The Spartan-3AN device authentication protocol prevents cloning. Design cloning, unauthorized overbuilding, and complete reverse engineering have driven device security requirements to higher and higher levels. Authentication moves the security from bitstream protection to the next generation of design-level security protecting both the design and embedded microcode. The authentication algorithm is entirely user defined, implemented using FPGA logic. Every product, generation, or design can have a different algorithm and functionality to enhance security.

In-System Flash Memory

Each Spartan-3AN FPGA contains abundant integrated SPI serial Flash memory, shown in Table 3, used primarily to store the FPGA's configuration bitstream. However, the Flash memory array is large enough to store at least two MultiBoot FPGA configuration bitstreams or nonvolatile data required by the FPGA application, such as code-shadowed MicroBlaze processor applications.

Table 3: Spartan-3AN Device In-System Flash Memory

Part Number	Total Flash Memory (Bits)	FPGA Bitstream (Bits)	Additional Flash Memory (Bits) ⁽¹⁾
XC3S50AN	1,081,344	437,312	642,048
XC3S200AN	4,325,376	1,196,128	3,127,872
XC3S400AN	4,325,376	1,886,560	2,437,248
XC3S700AN	8,650,752	2,732,640	5,917,824
XC3S1400AN	17,301,504	4,755,296	12,545,280

Notes:

1. Aligned to next available page location.

After configuration, the FPGA design has full access to the in-system Flash memory via an internal SPI interface; the control logic is implemented with FPGA logic. Additionally, the FPGA application itself can store nonvolatile data or provide live, in-system Flash updates.

The Spartan-3AN device in-system Flash memory supports leading-edge serial Flash features.

- Small page size (264 or 528 bytes) simplifies nonvolatile data storage
- Randomly accessible, byte addressable
- Up to 66 MHz serial data transfers
- SRAM page buffers
 - Read Flash data while programming another Flash page
 - EEPROM-like byte write functionality
 - Two buffers in most devices, one in XC3S50AN
- Page, Block, and Sector Erase

- Sector-based data protection and security features
 - Sector Protect: Write- and erase-protect a sector (changeable)
 - Sector Lockdown: Sector data is unchangeable (permanent)
- 128-byte Security Register
 - Separate from FPGA's unique Device DNA identifier
 - 64-byte factory-programmed identifier unique to the in-system Flash memory
 - 64-byte one-time programmable, user-programmable field
- 100,000 Program/Erase cycles
- 20-year data retention
- Comprehensive programming support
 - In-system prototype programming via JTAG using Xilinx [Platform Cable USB](#) and iMPACT software
 - Product programming support using BPM Microsystems programmers with appropriate programming adapter
 - Design examples demonstrating in-system programming from a Spartan-3AN FPGA application

I/O Capabilities

The Spartan-3AN FPGA SelectIO interface supports many popular single-ended and differential standards. [Table 4](#) shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional, input-only pins as indicated in [Table 4](#).

Spartan-3AN FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3AN FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 4: Available User I/Os and Differential (Diff) I/O Pairs

Package ⁽¹⁾	TQ144 TQG144		FT256 FTG256		FG400 FGG400		FG484 FGG484		FG676 FGG676	
	20 x 20 ⁽²⁾		17 x 17		21 x 21		23 x 23		27 x 27	
Device ⁽³⁾	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S50AN	108 ⁽⁴⁾ <i>(7)</i>	50 <i>(24)</i>	144 <i>(32)</i>	64 <i>(32)</i>	–	–	–	–	–	–
XC3S200AN	–	–	195 <i>(35)</i>	90 <i>(50)</i>	–	–	–	–	–	–
XC3S400AN	–	–	195 <i>(35)</i>	90 <i>(50)</i>	311 <i>(63)</i>	142 <i>(78)</i>	–	–	–	–
XC3S700AN	–	–	–	–	–	–	372 <i>(84)</i>	165 <i>(93)</i>	–	–
XC3S1400AN	–	–	–	–	–	–	375 <i>(87)</i>	165 <i>(93)</i>	502 <i>(94)</i>	227 <i>(131)</i>

Notes:

1. See [Pb and Pb-Free Packaging, page 7](#) for details on Pb and Pb-free packaging options.
2. The footprint for the TQ(G)144 (22 mm x 22 mm) package is larger than the package body.
3. Each Spartan-3AN FPGA has a pin-compatible Spartan-3A FPGA equivalent, although Spartan-3A FPGAs do not have internal SPI flash and offer more part/package combinations.
4. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in *italics* indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

Related Product Families

The Spartan-3AN FPGA family is generally compatible with the Spartan-3A FPGA family.

- [DS529: Spartan-3A FPGA Family Data Sheet](#)

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device.
09/12/07	2.0.1	Minor updates to text.
09/24/07	2.1	Added note that In-System Flash commands were not supported by simulation until ISE 10.1 software.
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that SPI_ACCESS simulation is supported in ISE 10.1 software. Updated links.
06/02/08	3.1	Minor updates.
11/19/09	3.2	In the Spartan-3AN FPGA Design Documentation section, added link to DS706 , <i>Extended Spartan-3A Family Overview</i> and removed references to older software versions.
12/02/10	4.0	Updated link to sign up for Alerts and updated Notice of Disclaimer .
04/01/11	4.1	Added the FT(G)256 package selection for the XC3S50AN and XC3S400AN devices and the FG(G)484 package selection for the XC3S1400AN device throughout this data sheet.

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Table 15: Recommended Operating Conditions for User I/Os Using Differential Signal Standards (Cont'd)

IOSTANDARD Attribute	V _{CCO} for Drivers ⁽¹⁾			V _{ID}			V _{ICM} ⁽²⁾		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
DIFF_SSTL3_II ⁽⁸⁾	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the “Using I/O Resources” chapter in [UG331](#).
4. See [External Termination Requirements for Differential I/O, page 22](#).
5. LVPECL is supported on inputs only, not outputs. Requires V_{CCAUX} = 3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = V_{CCAUX} - (V_{ID} / 2)
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. (V_{CCAUX} - 300 mV) ≤ V_{ICM} ≤ (V_{CCAUX} - 37 mV)
8. V_{REF} inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The V_{REF} settings are the same as for the single-ended versions in [Table 13](#). Other differential standards do not use V_{REF}.
9. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the “Using I/O Resources” chapter in [UG331](#).

Differential Output Pairs

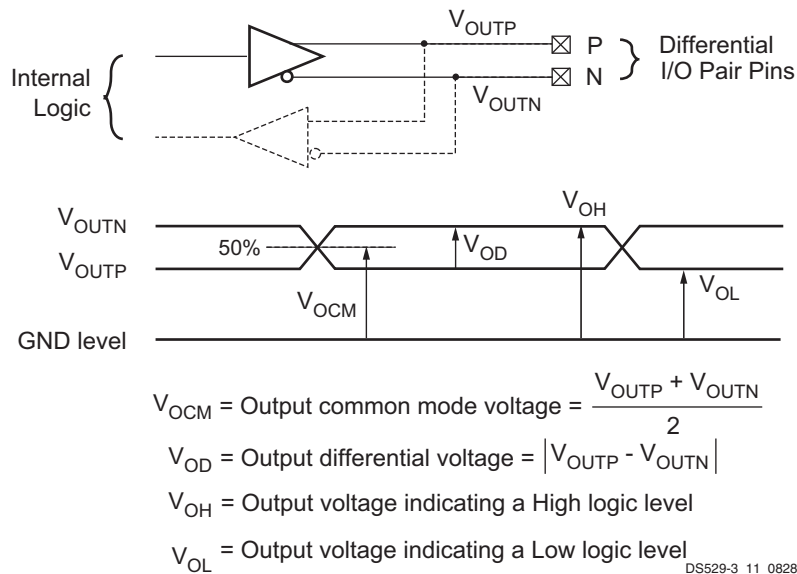


Figure 7: Differential Output Voltages

Table 23: Setup and Hold Times for the IOB Input Path (Cont'd)

Symbol	Description	Conditions	IFD_ DELAY_ VALUE	Device	Speed Grade		Units	
					-5	-4		
					Min	Min		
T _{IOICKPD}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. The Input Delay is programmed.	LVCMOS25 ⁽³⁾	1	XC3S400AN	-1.12	-1.12	ns	
					2	-1.70	-1.70	ns
					3	-2.08	-2.08	ns
					4	-2.38	-2.38	ns
					5	-2.23	-2.23	ns
					6	-2.69	-2.69	ns
					7	-3.08	-3.08	ns
					8	-3.35	-3.35	ns
			2	XC3S700AN	-1.67	-1.67	ns	
					2	-2.27	-2.27	ns
					3	-2.59	-2.59	ns
					4	-2.92	-2.92	ns
					5	-2.89	-2.89	ns
					6	-3.22	-3.22	ns
					7	-3.52	-3.52	ns
					8	-3.81	-3.81	ns
			3	XC3S1400AN	-1.60	-1.60	ns	
					2	-2.06	-2.06	ns
					3	-2.46	-2.46	ns
					4	-2.86	-2.86	ns
					5	-2.88	-2.88	ns
					6	-3.24	-3.24	ns
					7	-3.55	-3.55	ns
					8	-3.89	-3.89	ns
Set/Reset Pulse Width								
T _{RPW_IOB}	Minimum pulse width to SR control input on IOB	–	–	All	1.33	1.61	ns	

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10 and Table 13.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, add the appropriate Input adjustment from Table 26.
3. These hold times require adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. If this is true, subtract the appropriate Input adjustment from Table 26. When the hold time is negative, it is possible to change the data before the clock's active edge.

Table 24: Sample Window (Source Synchronous)

Symbol	Description	Maximum	Units
T _{SAMP}	Setup and hold capture window of an IOB flip-flop.	The input capture sample window value is highly specific to a particular application, device, package, I/O standard, I/O placement, DCM usage, and clock buffer. Please consult the appropriate Xilinx Answer Record for application-specific values. <ul style="list-style-type: none"> • Answer Record 30879 	ps

Table 25: Propagation Times for the IOB Input Path (Cont'd)

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T _{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	15	XC3S200AN	5.43	6.24	ns
			16		5.75	6.59	ns
			1	XC3S400AN	1.32	1.43	ns
			2		1.67	1.83	ns
			3		1.90	2.07	ns
			4		2.33	2.52	ns
			5		2.60	2.91	ns
			6		2.94	3.20	ns
			7		3.23	3.51	ns
			8		3.50	3.85	ns
			9		3.18	3.55	ns
			10		3.53	3.95	ns
			11		3.76	4.20	ns
			12		4.26	4.67	ns
			13		4.51	4.97	ns
			14		4.85	5.32	ns
			15		5.14	5.64	ns
			16		5.40	5.95	ns
			1	XC3S700AN	1.84	1.87	ns
			2		2.20	2.27	ns
			3		2.46	2.60	ns
			4		2.93	3.15	ns
			5		3.21	3.45	ns
			6		3.54	3.80	ns
			7		3.86	4.16	ns
			8		4.13	4.48	ns
			9		3.82	4.19	ns
			10		4.17	4.58	ns
			11		4.43	4.89	ns
			12		4.95	5.49	ns
			13		5.22	5.83	ns
			14		5.57	6.21	ns
			15		5.89	6.55	ns
			16		6.16	6.89	ns
			1	XC3S1400AN	1.95	2.18	ns
			2		2.29	2.59	ns
			3		2.54	2.84	ns
			4		2.96	3.30	ns

Table 25: Propagation Times for the IOB Input Path (Cont'd)

Symbol	Description	Conditions	DELAY_VALUE	Device	Speed Grade		Units
					-5	-4	
					Max	Max	
T _{IOPID}	The time it takes for data to travel from the Input pin to the I output with the input delay programmed	LVCMOS25 ⁽²⁾	5	XC3S1400AN	3.17	3.52	ns
			6		3.52	3.92	ns
			7		3.82	4.18	ns
			8		4.10	4.57	ns
			9		3.84	4.31	ns
			10		4.20	4.79	ns
			11		4.46	5.06	ns
			12		4.87	5.51	ns
			13		5.07	5.73	ns
			14		5.43	6.08	ns
			15		5.73	6.33	ns
16	6.01	6.77	ns				
T _{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25 ⁽²⁾	IFD_DELAY_VALUE=0	XC3S50AN	1.70	1.81	ns
				XC3S200AN	1.85	2.04	ns
				XC3S400AN	1.44	1.74	ns
				XC3S700AN	1.48	1.74	ns
				XC3S1400AN	1.50	1.97	ns

Table 29: Output Timing Adjustments for IOB (Cont'd)

Convert Output Time from LVC MOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units
			Speed Grade		
			-5	-4	
LVC MOS25	Slow	2 mA	5.33	5.33	ns
		4 mA	2.81	2.81	ns
		6 mA	2.82	2.82	ns
		8 mA	1.14	1.14	ns
		12 mA	1.10	1.10	ns
		16 mA	0.83	0.83	ns
		24 mA	2.26 ⁽³⁾	2.26 ⁽³⁾	ns
	Fast	2 mA	4.36	4.36	ns
		4 mA	1.76	1.76	ns
		6 mA	1.25	1.25	ns
		8 mA	0.38	0.38	ns
		12 mA	0	0	ns
		16 mA	0.01	0.01	ns
		24 mA	0.01	0.01	ns
	QuietIO	2 mA	25.92	25.92	ns
		4 mA	25.92	25.92	ns
		6 mA	25.92	25.92	ns
		8 mA	15.57	15.57	ns
		12 mA	15.59	15.59	ns
		16 mA	14.27	14.27	ns
		24 mA	11.37	11.37	ns

Table 29: Output Timing Adjustments for IOB (Cont'd)

Convert Output Time from LVC MOS25 with 12 mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below		Units	
			Speed Grade			
			-5	-4		
LVC MOS18	Slow	2 mA	4.48	4.48	ns	
		4 mA	3.69	3.69	ns	
		6 mA	2.91	2.91	ns	
		8 mA	1.99	1.99	ns	
		12 mA	1.57	1.57	ns	
		16 mA	1.19	1.19	ns	
		Fast	2 mA	3.96	3.96	ns
	4 mA		2.57	2.57	ns	
	6 mA		1.90	1.90	ns	
	8 mA		1.06	1.06	ns	
	12 mA		0.83	0.83	ns	
	16 mA		0.63	0.63	ns	
	QuietIO		2 mA	24.97	24.97	ns
		4 mA	24.97	24.97	ns	
		6 mA	24.08	24.08	ns	
		8 mA	16.43	16.43	ns	
		12 mA	14.52	14.52	ns	
		16 mA	13.41	13.41	ns	
		LVC MOS15	Slow	2 mA	5.82	5.82
	4 mA			3.97	3.97	ns
	6 mA			3.21	3.21	ns
8 mA	2.53			2.53	ns	
12 mA	2.06			2.06	ns	
Fast	2 mA		5.23	5.23	ns	
	4 mA		3.05	3.05	ns	
	6 mA		1.95	1.95	ns	
	8 mA		1.60	1.60	ns	
	12 mA		1.30	1.30	ns	
QuietIO	2 mA		34.11	34.11	ns	
	4 mA		25.66	25.66	ns	
	6 mA		24.64	24.64	ns	
	8 mA		22.06	22.06	ns	
		12 mA	20.64	20.64	ns	

Table 34: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.69	–	2.01	ns
Setup Times						
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.07	–	–0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
Hold Times						
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 10.

Table 35: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
Clock-to-Output Times						
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.11	–	4.82	ns
Setup Times						
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
Hold Times						
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
Clock Pulse Width						
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

Notes:

- The numbers in this table are based on the operating conditions set forth in Table 10.

In-System Flash (ISF) Memory Timing

Table 48: In-System Flash (ISF) Memory Operations

Symbol	Description	Device	Typical	Max	Units
T_{XFER}	Page to Buffer transfer time	All	–	400	μ s
T_{COMP}	Page to Buffer compare time	All	–	400	μ s
T_{PP}	Page Programming time	XC3S50AN XC3S200AN XC3S400AN	2	4	ms
		XC3S700AN XC3S1400AN	3	6	ms
T_{PE}	Page Erase time	XC3S50AN XC3S200AN XC3S400AN	13	32	ms
		XC3S700AN XC3S1400AN	15	35	ms
T_{PEP}	Page Erase and Programming time	XC3S50AN XC3S200AN XC3S400AN XC3S700AN	14	35	ms
		XC3S1400AN	17	40	ms
T_{BE}	Block Erase time	XC3S50AN	15	35	ms
		XC3S200AN XC3S400AN	30	75	ms
		XC3S700AN XC3S1400AN	45	100	ms
T_{SE}	Sector Erase time	XC3S50AN	0.8	2.5	s
		XC3S200AN XC3S400AN XC3S700AN XC3S1400AN	1.6	5	s

Table 62: Types of Pins on Spartan-3AN FPGAs (Cont'd)

Type with Color Code	Description	Pin Name(s) in Type ⁽¹⁾
CONFIG	Dedicated configuration pin, two per device. Not available as a user-I/O pin. Every package has two dedicated configuration pins. These pins are powered by VCCAUX. See UG332: Spartan-3 Generation Configuration User Guide for additional information on the DONE and PROG_B signals.	DONE, PROG_B
PWR MGMT	Control and status pins for the power-saving Suspend mode. SUSPEND is a dedicated pin and is powered by VCCAUX. AWAKE is a dual-purpose pin. Unless Suspend mode is enabled in the application, AWAKE is available as a user-I/O pin.	SUSPEND, AWAKE
JTAG	Dedicated JTAG pin - 4 per device. Not available as a user-I/O pin. Every package has four dedicated JTAG pins. These pins are powered by VCCAUX.	TDI, TMS, TCK, TDO
GND	Dedicated ground pin. The number of GND pins depends on the package used. All must be connected.	GND
VCCAUX	Dedicated auxiliary power supply pin. The number of VCCAUX pins depends on the package used. The In-System Flash memory is powered by VCCAUX. All must be connected to +3.3V.	VCCAUX
VCCINT	Dedicated internal core logic power supply pin. The number of VCCINT pins depends on the package used. All must be connected to +1.2V.	VCCINT
VCCO	Along with all the other VCCO pins in the same bank, this pin supplies power to the output buffers within the I/O bank and sets the input threshold voltage for some I/O standards. All must be connected.	VCCO_#
N.C.	This package pin is not connected in this specific device/package combination.	N.C.

Notes:

- # = I/O bank number, an integer between 0 and 3.

Package Pins by Type

Each package has three separate voltage supply inputs—VCCINT, VCCAUX, and VCCO—and a common ground return, GND. The numbers of pins dedicated to these functions vary by package, as shown in [Table 63](#).

Table 63: Power and Ground Supply Pins by Package

Package	VCCINT	VCCAUX	VCCO	GND
TQG144	4	4	8	13
FTG256	6	4	16	28
FGG400	9	8	22	43
FGG484	15	10	24	53
FGG676	23	14	36	77

A majority of package pins are user-defined I/O or input pins. However, the numbers and characteristics of these I/Os depend on the device type and the package in which it is available, as shown in [Table 64](#). The table shows the maximum number of single-ended I/O pins available, assuming that all I/O-, INPUT-, DUAL-, VREF-, and CLK-type pins are used as general-purpose I/O. AWAKE is counted here as a dual-purpose I/O pin. Likewise, the table shows the maximum number of differential pin-pairs available on the package. Finally, the table shows how the total maximum user-I/Os are distributed by pin type, including the number of unconnected—N.C.—pins on the device.

Not all I/O standards are supported on all I/O banks. The left and right banks (I/O banks 1 and 3) support higher output drive current than the top and bottom banks (I/O banks 0 and 2). Similarly, true differential output standards, such as LVDS, RSDS, PPDS, miniLVDS, and TMS, are only supported in the top or bottom banks (I/O banks 0 and 2). Inputs are unrestricted. For more details, see the “Using I/O Resources” chapter in [UG331](#).

TQG144: 144-lead Thin Quad Flat Package

The XC3S50AN is available in the 144-lead thin quad flat package, TQG144.

Table 68 lists all the package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type (as defined in Table 62). The XC3S50AN does not support the address output pins for the Byte-wide Peripheral Interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 68: Spartan-3AN TQG144 Pinout

Bank	Pin Name	Pin	Type
0	IO_0	P142	I/O
0	IO_L01N_0	P111	I/O
0	IO_L01P_0	P110	I/O
0	IO_L02N_0	P113	I/O
0	IO_L02P_0/VREF_0	P112	VREF
0	IO_L03N_0	P117	I/O
0	IO_L03P_0	P115	I/O
0	IO_L04N_0	P116	I/O
0	IO_L04P_0	P114	I/O
0	IO_L05N_0	P121	I/O
0	IO_L05P_0	P120	I/O
0	IO_L06N_0/GCLK5	P126	GCLK
0	IO_L06P_0/GCLK4	P124	GCLK
0	IO_L07N_0/GCLK7	P127	GCLK
0	IO_L07P_0/GCLK6	P125	GCLK
0	IO_L08N_0/GCLK9	P131	GCLK
0	IO_L08P_0/GCLK8	P129	GCLK
0	IO_L09N_0/GCLK11	P132	GCLK
0	IO_L09P_0/GCLK10	P130	GCLK
0	IO_L10N_0	P135	I/O
0	IO_L10P_0	P134	I/O
0	IO_L11N_0	P139	I/O
0	IO_L11P_0	P138	I/O
0	IO_L12N_0/PUDC_B	P143	DUAL
0	IO_L12P_0/VREF_0	P141	VREF
0	IP_0	P140	INPUT
0	IP_0/VREF_0	P123	VREF
0	VCCO_0	P119	VCCO
0	VCCO_0	P136	VCCO
1	IO_1	P79	I/O
1	IO_L01N_1/LDC2	P78	DUAL
1	IO_L01P_1/HDC	P76	DUAL
1	IO_L02N_1/LDC0	P77	DUAL

Table 68: Spartan-3AN TQG144 Pinout (Cont'd)

Bank	Pin Name	Pin	Type
1	IO_L02P_1/LDC1	P75	DUAL
1	IO_L03N_1	P84	I/O
1	IO_L03P_1	P82	I/O
1	IO_L04N_1/RHCLK1	P85	RHCLK
1	IO_L04P_1/RHCLK0	P83	RHCLK
1	IO_L05N_1/TRDY1/RHCLK3	P88	RHCLK
1	IO_L05P_1/RHCLK2	P87	RHCLK
1	IO_L06N_1/RHCLK5	P92	RHCLK
1	IO_L06P_1/RHCLK4	P90	RHCLK
1	IO_L07N_1/RHCLK7	P93	RHCLK
1	IO_L07P_1/IRDY1/RHCLK6	P91	RHCLK
1	IO_L08N_1	P98	I/O
1	IO_L08P_1	P96	I/O
1	IO_L09N_1	P101	I/O
1	IO_L09P_1	P99	I/O
1	IO_L10N_1	P104	I/O
1	IO_L10P_1	P102	I/O
1	IO_L11N_1	P105	I/O
1	IO_L11P_1	P103	I/O
1	IP_1/VREF_1	P80	VREF
1	IP_1/VREF_1	P97	VREF
1	VCCO_1	P86	VCCO
1	VCCO_1	P95	VCCO
2	IO_2/MOSI/CSI_B	P62	DUAL
2	IO_L01N_2/M0	P38	DUAL
2	IO_L01P_2/M1	P37	DUAL
2	IO_L02N_2/CSO_B	P41	DUAL
2	IO_L02P_2/M2	P39	DUAL
2	IO_L03N_2/VS1	P44	DUAL
2	IO_L03P_2/RDWR_B	P42	DUAL
2	IO_L04N_2/VS0	P45	DUAL
2	IO_L04P_2/VS2	P43	DUAL
2	IO_L05N_2/D7	P48	DUAL

FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array

The 256-ball fine-pitch, thin ball grid array package, FTG256, supports the XC3S50AN, XC3S200AN, and XC3S400AN devices. Table 70 lists all the package pins for these devices. They are sorted by bank number and then by the pin name of the largest device. Pins that form a differential I/O pair appear together in the table. The differential I/O pairs that have different assignments between the XC3S50AN and the XC3S200AN or XC3S400AN are highlighted in light blue in Table 70. See Footprint Migration Differences, page 87 for additional information. The table also shows the pin number for each pin and the pin type (as defined in Table 62).

The footprints for the XC3S200AN and XC3S400AN in the FTG256 are identical. Figure 21 shows the common footprint for the XC3S200AN and XC3S400AN. The XC3S50AN footprint is compatible with the XC3S200AN and XC3S400AN, however, there are 51 unconnected balls (indicated as N.C. in Table 70).

Table 73 summarizes the XC3S50AN FPGA footprint migration differences for the FTG256 package.

The XC3S50AN does not support the address output pins for the byte-wide peripheral interface (BPI) configuration mode.

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip.

Pinout Table

Table 70: Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN)

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
0	IO_L01N_0	IO_L01N_0	C13	I/O
0	IO_L01P_0	IO_L01P_0	D13	I/O
0	IO_L02N_0	IO_L02N_0	B14	I/O
0	IO_L02P_0/VREF_0	IO_L02P_0/VREF_0	B15	VREF
0	IO_L03N_0	IO_L03N_0	D11	I/O
0	IO_L03P_0	IO_L03P_0	C12	I/O
0	IO_L04N_0	IO_L04N_0	A13	I/O
0	IO_L04P_0	IO_L04P_0	A14	I/O
0	N.C.	IO_L05N_0	A12	I/O
0	IP_0	IO_L05P_0	B12	I/O
0	N.C.	IO_L06N_0/VREF_0	E10	VREF
0	N.C.	IO_L06P_0	D10	I/O
0	IO_L07N_0	IO_L07N_0	A11	I/O
0	IO_L07P_0	IO_L07P_0	C11	I/O
0	IO_L08N_0	IO_L08N_0	A10	I/O
0	IO_L08P_0	IO_L08P_0	B10	I/O
0	IO_L09N_0/GCLK5	IO_L09N_0/GCLK5	D9	GCLK
0	IO_L09P_0/GCLK4	IO_L09P_0/GCLK4	C10	GCLK
0	IO_L10N_0/GCLK7	IO_L10N_0/GCLK7	A9	GCLK
0	IO_L10P_0/GCLK6	IO_L10P_0/GCLK6	C9	GCLK
0	IO_L11N_0/GCLK9	IO_L11N_0/GCLK9	D8	GCLK
0	IO_L11P_0/GCLK8	IO_L11P_0/GCLK8	C8	GCLK
0	IO_L12N_0/GCLK11	IO_L12N_0/GCLK11	B8	GCLK
0	IO_L12P_0/GCLK10	IO_L12P_0/GCLK10	A8	GCLK
0	N.C.	IO_L13N_0	C7	I/O
0	N.C.	IO_L13P_0	A7	I/O

FTG256 Footprint (XC3S200AN, XC3S400AN)

		Bank 0															
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Bank 3	A	GND	PROG_B	I/O L19P_0	I/O L18P_0	I/O L17P_0	I/O L15P_0	I/O L13P_0	I/O L12P_0 GCLK10	I/O L10N_0 GCLK7	I/O L08N_0	I/O L07N_0	I/O L05N_0	I/O L04N_0	I/O L04P_0	TCK	GND
	B	TDI	TMS	I/O L19N_0	I/O L18N_0	VCCO_0	I/O L15N_0	GND	I/O L12N_0 GCLK11	VCCO_0	I/O L08P_0	GND	I/O L05P_0	VCCO_0	I/O L02N_0	I/O L02P_0 VREF_0	TDO
	C	I/O L01N_3	I/O L01P_3	GND	I/O L20P_0 VREF_0	I/O L17N_0	I/O L16N_0	I/O L13N_0	I/O L11P_0 GCLK8	I/O L10P_0 GCLK6	I/O L09P_0 GCLK4	I/O L07P_0	I/O L03P_0	I/O L01N_0	GND	I/O L24N_1 A25	I/O L24P_1 A24
	D	I/O L03P_3	VCCO_3	I/O L02N_3	I/O L02P_3	I/O L20N_0 PUDC_B	INPUT	I/O L16P_0	I/O L11N_0 GCLK9	I/O L09N_0 GCLK5	I/O L06P_0	I/O L03N_0	INPUT	I/O L01P_0	I/O L23N_1 A23	I/O L22N_1 A21	I/O L22P_1 A20
	E	I/O L03N_3	I/O L05N_3	I/O L05P_3	INPUT L04P_3	GND	INPUT	I/O L14N_0 VREF_0	VCCO_0	INPUT VREF_0	I/O L06N_0 VREF_0	VCCAUX	GND	I/O L23P_1 A22	I/O L20P_1 A18	VCCO_1	I/O L18P_1 A14
	F	I/O L08P_3	GND	I/O L07P_3	INPUT L04N_3 VREF_3	VCCAUX	GND	INPUT	I/O L14P_0	INPUT	INPUT	INPUT L25N_1	INPUT L25P_1 VREF_1	I/O L20N_1 A19	I/O L19N_1 A17	I/O L18N_1 A15	I/O L16N_1 A11
	G	I/O L08N_3 VREF_3	I/O L11P_3 LHCLK0	I/O L09P_3	I/O L07N_3	INPUT L06N_3 VREF_3	INPUT L06P_3	VCCINT	GND	VCCINT	GND	INPUT L21N_1	INPUT L21P_1 VREF_1	I/O L19P_1 A16	I/O L17N_1 A13	GND	I/O L16P_1 A10
	H	I/O L11N_3 LHCLK1	VCCO_3	I/O L12P_3 LHCLK2	I/O L09N_3	I/O L10N_3	I/O L10P_3	INPUT L13P_3	VCCINT	GND	INPUT L13P_1	INPUT L13N_1	VCCO_1	I/O L17P_1 A12	I/O L14N_1 RHCLK5	I/O L15P_1 IRDY1 RHCLK6	I/O L15N_1 RHCLK7
	J	I/O L14N_3 LHCLK5	I/O L14P_3 LHCLK4	I/O L12N_3 IRDY2 LHCLK3	I/O L17P_3	VCCO_3	I/O L17N_3	INPUT L13N_3	GND	VCCINT	INPUT L09P_1 VREF_1	INPUT L09N_1	I/O L10P_1 A8	I/O L10N_1 A9	I/O L14P_1 RHCLK4	VCCO_1	I/O L12N_1 TRDY1 RHCLK3
	K	I/O L15N_3 LHCLK7	GND	I/O L15P_3 TRDY2 LHCLK6	I/O L18P_3	INPUT L21P_3	INPUT L21N_3	GND	VCCINT	GND	VCCINT	INPUT L04P_1	INPUT L04N_1 VREF_1	I/O L06N_1 A3	I/O L11N_1 RHCLK1	I/O L11P_1 RHCLK0	I/O L12P_1 RHCLK2
	L	I/O L16P_3 VREF_3	I/O L16N_3	I/O L18N_3	I/O L19N_3	INPUT L25P_3	INPUT L25N_3 VREF_3	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	GND	VCCAUX	I/O L06P_1 A2	I/O L08P_1 A6	GND	I/O L08N_1 A7
	M	I/O L20P_3	VCCO_3	I/O L19P_3	I/O L24N_3	GND	VCCAUX	INPUT VREF_2	INPUT VREF_2	VCCO_2	I/O L13N_2	INPUT VREF_2	GND	I/O L05P_1	I/O L05N_1 VREF_1	I/O L07P_1 A4	I/O L07N_1 A5
	N	I/O L20N_3	I/O L22P_3	I/O L24P_3	I/O L01P_2 M1	INPUT VREF_2	I/O L04P_2 VS1	I/O L07P_2	I/O L08N_2 D4	I/O L11P_2 GCLK0	I/O L13P_2	I/O L16N_2	I/O L19P_2	I/O L01P_1 HDC	I/O L01N_1 LDC2	VCCO_1	I/O L03N_1 A1
	P	I/O L22N_3	I/O L23N_3	GND	I/O L01N_2 M0	I/O L04N_2 VS0	I/O L07N_2	I/O L08P_2 D5	I/O L10P_2 GCLK14	I/O L11N_2 GCLK1	I/O L14N_2 MOSI CSI_B	I/O L16P_2	I/O L17N_2 D3	I/O L19N_2	GND	I/O L02N_1 LDC0	I/O L03P_1 A0
	R	I/O L23P_3	I/O L02P_2 M2	I/O L03P_2 RDWR_B	VCCO_2	I/O L05N_2	GND	I/O L09P_2 GCLK12	VCCO_2	I/O L12P_2 GCLK2	GND	I/O L15N_2 DOUT	VCCO_2	I/O L18N_2 D1	I/O L20N_2 CCLK	I/O L02P_1 LDC1	SUSPEND
	T	GND	I/O L02N_2 CSO_B	I/O L03N_2 VS2	I/O L05P_2	I/O L06P_2 D7	I/O L06N_2 D6	I/O L09N_2 GCLK13	I/O L10N_2 GCLK15	I/O L12N_2 GCLK3	I/O L14P_2	I/O L15P_2 AWAKE	I/O L17P_2 INIT_B	I/O L18P_2 D2	I/O L20P_2 D0 DIN/MISO	DONE	GND
		Bank 2															

Figure 21: XC3S200AN and XC3S400AN FPGA in FTG256 Package Footprint (Top View)

69	I/O: Unrestricted, general-purpose user I/O	51	DUAL: Configuration pins, then possible user I/O	21	VREF: User I/O or input voltage reference for bank	2	SUSPEND: Dedicated SUSPEND and dual-purpose AWAKE Power Management pins
21	INPUT: Unrestricted, general-purpose input pin	32	CLK: User I/O, input, or global buffer input	16	VCCO: Output voltage supply for bank		
2	CONFIG: Dedicated configuration pins	4	JTAG: Dedicated JTAG port pins	6	VCCINT: Internal core supply voltage (+1.2V)		
0	N.C.: Not connected	28	GND: Ground	4	VCCAUX: Auxiliary supply voltage		

Table 76: Spartan-3AN FGG400 Pinout (Cont'd)

Bank	Pin Name	FGG400 Ball	Type
VCCAUX	TMS	E4	JTAG
VCCAUX	VCCAUX	A13	VCCAUX
VCCAUX	VCCAUX	E16	VCCAUX
VCCAUX	VCCAUX	H1	VCCAUX
VCCAUX	VCCAUX	K13	VCCAUX
VCCAUX	VCCAUX	L8	VCCAUX
VCCAUX	VCCAUX	N20	VCCAUX
VCCAUX	VCCAUX	T5	VCCAUX
VCCAUX	VCCAUX	Y8	VCCAUX
VCCINT	VCCINT	J10	VCCINT
VCCINT	VCCINT	J12	VCCINT
VCCINT	VCCINT	K9	VCCINT
VCCINT	VCCINT	K11	VCCINT
VCCINT	VCCINT	L10	VCCINT
VCCINT	VCCINT	L12	VCCINT
VCCINT	VCCINT	M9	VCCINT
VCCINT	VCCINT	M11	VCCINT
VCCINT	VCCINT	N10	VCCINT

User I/Os by Bank

Table 77 indicates how the 311 available user-I/O pins are distributed between the four I/O banks on the FGG400 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 77: User I/Os Per Bank for the XC3S400AN in the FGG400 Package

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	77	50	12	1	6	8
Right	1	79	21	12	30	8	8
Bottom	2	76	35	6	21	6	8
Left	3	79	49	16	0	6	8
Total		311	155	46	52	26	32

Footprint Migration Differences

The XC3S400AN is the only Spartan-3AN FPGA offered in the FGG400 package.

The XC3S400AN FPGA is pin compatible with the Spartan-3A XC3S400A FPGA in the FG(G)400 package, although the Spartan-3A FPGA requires an external configuration source.

Table 78: Spartan-3AN FGG484 Pinout (Cont'd)

Bank	Pin Name	FGG484 Ball	Type
0	IO_L29N_0	D6	I/O
0	IO_L29P_0	C6	I/O
0	IO_L30N_0	D8	I/O
0	IO_L30P_0	E9	I/O
0	IO_L31N_0	B4	I/O
0	IO_L31P_0	A4	I/O
0	IO_L32N_0	D5	I/O
0	IO_L32P_0	C5	I/O
0	IO_L33N_0	B3	I/O
0	IO_L33P_0	A3	I/O
0	IO_L34N_0	F8	I/O
0	IO_L34P_0	E7	I/O
0	IO_L35N_0	E6	I/O
0	IO_L35P_0	F7	I/O
0	IO_L36N_0/PUDC_B	A2	DUAL
0	IO_L36P_0/VREF_0	B2	VREF
0	IP_0	E16	INPUT
0	IP_0	E8	INPUT
0	IP_0	F10	INPUT
0	IP_0	F12	INPUT
0	IP_0	F16	INPUT
0	IP_0	G10	INPUT
0	IP_0	G11	INPUT
0	IP_0	G12	INPUT
0	IP_0	G13	INPUT
0	IP_0	G14	INPUT
0	IP_0	G15	INPUT
0	IP_0	G16	INPUT
0	IP_0	G7	INPUT
0	IP_0	G9	INPUT
0	IP_0	H10	INPUT
0	IP_0	H13	INPUT
0	IP_0	H14	INPUT
0	IP_0/VREF_0	G8	VREF
0	IP_0/VREF_0	H12	VREF
0	IP_0/VREF_0	H9	VREF
0	VCCO_0	B10	VCCO
0	VCCO_0	B14	VCCO
0	VCCO_0	B18	VCCO
0	VCCO_0	B5	VCCO

Table 78: Spartan-3AN FGG484 Pinout (Cont'd)

Bank	Pin Name	FGG484 Ball	Type
0	VCCO_0	F14	VCCO
0	VCCO_0	F9	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	AA22	DUAL
1	IO_L02N_1/LDC0	W20	DUAL
1	IO_L02P_1/LDC1	W19	DUAL
1	IO_L03N_1/A1	T18	DUAL
1	IO_L03P_1/A0	T17	DUAL
1	IO_L05N_1	W21	I/O
1	IO_L05P_1	Y22	I/O
1	IO_L06N_1	V20	I/O
1	IO_L06P_1	V19	I/O
1	IO_L07N_1	V22	I/O
1	IO_L07P_1	W22	I/O
1	IO_L09N_1	U21	I/O
1	IO_L09P_1	U22	I/O
1	IO_L10N_1	U19	I/O
1	IO_L10P_1	U20	I/O
1	IO_L11N_1	T22	I/O
1	IO_L11P_1	T20	I/O
1	IO_L13N_1	T19	I/O
1	IO_L13P_1	R20	I/O
1	IO_L14N_1	R22	I/O
1	IO_L14P_1	R21	I/O
1	IO_L15N_1/VREF_1	P22	VREF
1	IO_L15P_1	P20	I/O
1	IO_L17N_1/A3	P18	DUAL
1	IO_L17P_1/A2	R19	DUAL
1	IO_L18N_1/A5	N21	DUAL
1	IO_L18P_1/A4	N22	DUAL
1	IO_L19N_1/A7	N19	DUAL
1	IO_L19P_1/A6	N20	DUAL
1	IO_L20N_1/A9	N17	DUAL
1	IO_L20P_1/A8	N18	DUAL
1	IO_L21N_1/RHCLK1	L22	RHCLK
1	IO_L21P_1/RHCLK0	M22	RHCLK
1	IO_L22N_1/TRDY1/RHCLK3	L20	RHCLK
1	IO_L22P_1/RHCLK2	L21	RHCLK
1	IO_L24N_1/RHCLK5	M20	RHCLK
1	IO_L24P_1/RHCLK4	M18	RHCLK

User I/Os by Bank

Table 79 and Table 80 indicate how the user-I/O pins are distributed between the four I/O banks on the FGG484 package. The AWAKE pin is counted as a dual-purpose I/O.

Table 79: User I/Os Per Bank for the XC3S700AN in the FGG484 Package

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	92	58	17	1	8	8
Right	1	94	33	15	30	8	8
Bottom	2	92	43	11	21	9	8
Left	3	94	61	17	0	8	8
Total		372	195	60	52	33	32

Table 80: User I/Os Per Bank for the XC3S1400AN in the FGG484 Package

Package Edge	I/O Bank	Maximum I/Os	All Possible I/O Pins by Type				
			I/O	INPUT	DUAL	VREF	CLK
Top	0	92	58	17	1	8	8
Right	1	94	33	15	30	8	8
Bottom	2	95	43	13	21	10	8
Left	3	94	61	17	0	8	8
Total		375	195	62	52	34	32

Footprint Migration Differences

Table 81 summarizes the three footprint and functionality differences between the XC3S700AN and the XC3S1400AN FPGAs that can affect migration between devices available in the FGG484 package. All other pins unconditionally migrate between the Spartan-3AN devices available in the FGG484 package.

Spartan-3AN FPGAs are pin compatible with the same density Spartan-3A FPGAs in the FG(G)484 package, although the Spartan-3A FPGAs require an external configuration source.

In Table 81, the arrow (→) indicates that this pin can unconditionally migrate from the device on the left to the device on the right. Migration in the other direction is possible depending on how the pin is configured for the device on the right.

Table 81: FGG484 XC3S700AN to XC3S1400AN Footprint Migration/Differences

FGG484 Ball	Bank	XC3S700AN	Migration	XC3S1400AN
T8	2	N.C.	→	INPUT/VREF
U7	2	N.C.	→	INPUT
U16	2	N.C.	→	INPUT
Number of Differences:			3	

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
0	IO_L33N_0	B10	I/O
0	IO_L33P_0	A10	I/O
0	IO_L34N_0	D10	I/O
0	IO_L34P_0	C10	I/O
0	IO_L35N_0	H12	I/O
0	IO_L35P_0	G12	I/O
0	IO_L36N_0	B9	I/O
0	IO_L36P_0	A9	I/O
0	IO_L37N_0	D9	I/O
0	IO_L37P_0	E10	I/O
0	IO_L38N_0	B8	I/O
0	IO_L38P_0	A8	I/O
0	IO_L39N_0	K12	I/O
0	IO_L39P_0	J12	I/O
0	IO_L40N_0	D8	I/O
0	IO_L40P_0	C8	I/O
0	IO_L41N_0	C6	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L42P_0	B7	I/O
0	IO_L43N_0	K11	I/O
0	IO_L43P_0	J11	I/O
0	IO_L44N_0	D6	I/O
0	IO_L44P_0	C5	I/O
0	IO_L45N_0	B4	I/O
0	IO_L45P_0	A4	I/O
0	IO_L46N_0	H10	I/O
0	IO_L46P_0	G10	I/O
0	IO_L47N_0	H9	I/O
0	IO_L47P_0	G9	I/O
0	IO_L48N_0	E7	I/O
0	IO_L48P_0	F7	I/O
0	IO_L51N_0	B3	I/O
0	IO_L51P_0	A3	I/O
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L52P_0/VREF_0	F8	VREF
0	IP_0	A5	INPUT
0	IP_0	A7	INPUT
0	IP_0	A13	INPUT
0	IP_0	A17	INPUT

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
0	IP_0	A23	INPUT
0	IP_0	C4	INPUT
0	IP_0	D12	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	E11	INPUT
0	IP_0	E18	INPUT
0	IP_0	E20	INPUT
0	IP_0	F10	INPUT
0	IP_0	G14	INPUT
0	IP_0	G16	INPUT
0	IP_0	H13	INPUT
0	IP_0	H18	INPUT
0	IP_0	J10	INPUT
0	IP_0	J13	INPUT
0	IP_0	J15	INPUT
0	IP_0/VREF_0	D7	VREF
0	IP_0/VREF_0	D14	VREF
0	IP_0/VREF_0	G11	VREF
0	IP_0/VREF_0	J17	VREF
0	N.C.	A24	N.C.
0	N.C.	B24	N.C.
0	N.C.	D5	N.C.
0	N.C.	E9	N.C.
0	N.C.	F18	N.C.
0	N.C.	E6	N.C.
0	N.C.	F9	N.C.
0	N.C.	G18	N.C.
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
1	IO_L51P_1	G23	I/O
1	IO_L53N_1	K20	I/O
1	IO_L53P_1	L20	I/O
1	IO_L54N_1	F24	I/O
1	IO_L54P_1	F25	I/O
1	IO_L55N_1	L17	I/O
1	IO_L55P_1	L18	I/O
1	IO_L56N_1	F23	I/O
1	IO_L56P_1	E24	I/O
1	IO_L57N_1	K18	I/O
1	IO_L57P_1	K19	I/O
1	IO_L58N_1	G22	I/O
1	IO_L58P_1/VREF_1	F22	VREF
1	IO_L59N_1	J20	I/O
1	IO_L59P_1	J19	I/O
1	IO_L60N_1	D26	I/O
1	IO_L60P_1	E26	I/O
1	IO_L61N_1	D24	I/O
1	IO_L61P_1	D25	I/O
1	IO_L62N_1/A21	H21	DUAL
1	IO_L62P_1/A20	J21	DUAL
1	IO_L63N_1/A23	C25	DUAL
1	IO_L63P_1/A22	C26	DUAL
1	IO_L64N_1/A25	G21	DUAL
1	IO_L64P_1/A24	H20	DUAL
1	IP_L16N_1	Y26	INPUT
1	IP_L16P_1	W25	INPUT
1	IP_L20N_1/VREF_1	V26	VREF
1	IP_L20P_1	W26	INPUT
1	IP_L24N_1/VREF_1	U26	VREF
1	IP_L24P_1	U25	INPUT
1	IP_L28N_1	R24	INPUT
1	IP_L28P_1/VREF_1	R23	VREF
1	IP_L32N_1	N25	INPUT
1	IP_L32P_1	N26	INPUT
1	IP_L36N_1	N23	INPUT
1	IP_L36P_1/VREF_1	M24	VREF
1	IP_L40N_1	L23	INPUT
1	IP_L40P_1	K24	INPUT
1	IP_L44N_1	H25	INPUT

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
1	IP_L44P_1/VREF_1	H26	VREF
1	IP_L48N_1	H24	INPUT
1	IP_L48P_1	H23	INPUT
1	IP_L52N_1/VREF_1	G25	VREF
1	IP_L52P_1	G26	INPUT
1	IP_L65N_1	B25	INPUT
1	IP_L65P_1/VREF_1	B26	VREF
1	VCCO_1	AB25	VCCO
1	VCCO_1	E25	VCCO
1	VCCO_1	H22	VCCO
1	VCCO_1	L19	VCCO
1	VCCO_1	L25	VCCO
1	VCCO_1	N22	VCCO
1	VCCO_1	T19	VCCO
1	VCCO_1	T25	VCCO
1	VCCO_1	W22	VCCO
2	IO_L01N_2/M0	AD4	DUAL
2	IO_L01P_2/M1	AC4	DUAL
2	IO_L02N_2/CSO_B	AA7	DUAL
2	IO_L02P_2/M2	Y7	DUAL
2	IO_L05N_2	Y9	I/O
2	IO_L05P_2	W9	I/O
2	IO_L06N_2	AF3	I/O
2	IO_L06P_2	AE3	I/O
2	IO_L07N_2	AF4	I/O
2	IO_L07P_2	AE4	I/O
2	IO_L08N_2	AD6	I/O
2	IO_L08P_2	AC6	I/O
2	IO_L09N_2	W10	I/O
2	IO_L09P_2	V10	I/O
2	IO_L10N_2	AE6	I/O
2	IO_L10P_2	AF5	I/O
2	IO_L11N_2	AE7	I/O
2	IO_L11P_2	AD7	I/O
2	IO_L12N_2	AA10	I/O
2	IO_L12P_2	Y10	I/O
2	IO_L13N_2	U11	I/O
2	IO_L13P_2	V11	I/O
2	IO_L14N_2	AB7	I/O
2	IO_L14P_2	AC8	I/O

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
3	IP_L58N_3/VREF_3	AA5	VREF
3	IP_L58P_3	AA4	INPUT
3	IP_L62N_3	AB4	INPUT
3	IP_L62P_3	AB3	INPUT
3	IP_L66N_3/VREF_3	AE2	VREF
3	IP_L66P_3	AE1	INPUT
3	VCCO_3	AB2	VCCO
3	VCCO_3	E2	VCCO
3	VCCO_3	H5	VCCO
3	VCCO_3	L2	VCCO
3	VCCO_3	L8	VCCO
3	VCCO_3	P5	VCCO
3	VCCO_3	T2	VCCO
3	VCCO_3	T8	VCCO
3	VCCO_3	W5	VCCO
GND	GND	A1	GND
GND	GND	A6	GND
GND	GND	A11	GND
GND	GND	A16	GND
GND	GND	A21	GND
GND	GND	A26	GND
GND	GND	AA1	GND
GND	GND	AA6	GND
GND	GND	AA11	GND
GND	GND	AA16	GND
GND	GND	AA21	GND
GND	GND	AA26	GND
GND	GND	AD3	GND
GND	GND	AD8	GND
GND	GND	AD13	GND
GND	GND	AD18	GND
GND	GND	AD24	GND
GND	GND	AF1	GND
GND	GND	AF6	GND
GND	GND	AF11	GND
GND	GND	AF16	GND
GND	GND	AF21	GND
GND	GND	AF26	GND
GND	GND	C3	GND
GND	GND	C9	GND

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
GND	GND	C14	GND
GND	GND	C19	GND
GND	GND	C24	GND
GND	GND	F1	GND
GND	GND	F6	GND
GND	GND	F11	GND
GND	GND	F16	GND
GND	GND	F21	GND
GND	GND	F26	GND
GND	GND	H3	GND
GND	GND	H8	GND
GND	GND	H14	GND
GND	GND	H19	GND
GND	GND	J24	GND
GND	GND	K10	GND
GND	GND	K17	GND
GND	GND	L1	GND
GND	GND	L6	GND
GND	GND	L11	GND
GND	GND	L13	GND
GND	GND	L15	GND
GND	GND	L21	GND
GND	GND	L26	GND
GND	GND	M12	GND
GND	GND	M14	GND
GND	GND	M16	GND
GND	GND	N3	GND
GND	GND	N8	GND
GND	GND	N11	GND
GND	GND	N15	GND
GND	GND	P12	GND
GND	GND	P16	GND
GND	GND	P19	GND
GND	GND	P24	GND
GND	GND	R11	GND
GND	GND	R13	GND
GND	GND	R15	GND
GND	GND	T1	GND
GND	GND	T6	GND
GND	GND	T12	GND