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### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	1472
Number of Logic Elements/Cells	13248
Total RAM Bits	368640
Number of I/O	372
Number of Gates	700000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BBGA
Supplier Device Package	484-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc3s700an-5fgg484c">https://www.e-xfl.com/product-detail/xilinx/xc3s700an-5fgg484c</a>

## Introduction

The Spartan<sup>®</sup>-3AN FPGA family combines the best attributes of a leading edge, low cost FPGA with nonvolatile technology across a broad range of densities. The family combines all the features of the Spartan-3A FPGA family plus leading technology in-system Flash memory for configuration and nonvolatile data storage.

The Spartan-3AN FPGAs are part of the Extended Spartan-3A family, which also includes the Spartan-3A FPGAs and the higher density Spartan-3A DSP FPGAs. The Spartan-3AN FPGA family is excellent for space-constrained applications such as blade servers, medical devices, automotive infotainment, telematics, GPS, and other small consumer products. Combining FPGA and Flash technology minimizes chip count, PCB traces and overall size while increasing system reliability.

The Spartan-3AN FPGA internal configuration interface is completely self-contained, increasing design security. The family maintains full support for external configuration. The Spartan-3AN FPGA is the world's first nonvolatile FPGA with MultiBoot, supporting two or more configuration files in one device, allowing alternative configurations for field upgrades, test modes, or multiple system configurations.

## Features

- The new standard for low cost nonvolatile FPGA solutions
- Eliminates traditional nonvolatile FPGA limitations with the advanced 90 nm Spartan-3A device feature set
  - Memory, multipliers, DCMs, SelectIO, hot swap, power management, etc.
- Integrated robust configuration memory
  - Saves board space
  - Improves ease-of-use
  - Simplifies design
  - Reduces support issues
- Plentiful amounts of nonvolatile memory available to the user
  - Up to 11+ Mb available
  - MultiBoot support
  - Embedded processing and code shadowing
  - Scratchpad memory
- Robust 100K Flash memory program/erase cycles
- 20 years Flash memory data retention
- Security features provide bitstream anti-cloning protection
  - Buried configuration interface
  - Unique Device DNA serial number in each device for design Authentication to prevent unauthorized copying
  - Flash memory sector protection and lockdown
- Configuration watchdog timer automatically recovers from configuration errors
- Suspend mode reduces system power consumption
  - Retains all design state and FPGA configuration data
  - Fast response time, typically less than 100  $\mu$ s
- Full hot-swap compliance
- Multi-voltage, multi-standard SelectIO<sup>™</sup> interface pins
  - Up to 502 I/O pins or 227 differential signal pairs
  - LVCMOS, LVTTTL, HSTL, and SSTL single-ended signal standards
  - 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signaling
  - Up to 24 mA output drive
  - 3.3V  $\pm$ 10% compatibility and hot swap compliance
  - 622+ Mb/s data transfer rate per I/O
  - DDR/DDR2 SDRAM support up to 400 Mb/s
  - LVDS, RSDS, mini-LVDS, PPDS, and HSTL/SSTL differential I/O
- Abundant, flexible logic resources
  - Densities up to 25,344 logic cells
  - Optional shift register or distributed RAM support
  - Enhanced 18 x 18 multipliers with optional pipeline
- Hierarchical SelectRAM<sup>™</sup> memory architecture
  - Up to 576 Kbits of dedicated block RAM
  - Up to 176 Kbits of efficient distributed RAM
- Up to eight Digital Clock Managers (DCMs)
- Eight global clocks and eight additional clocks per each half of device, plus abundant low-skew routing
- Complete Xilinx<sup>®</sup> ISE<sup>®</sup> and WebPACK<sup>™</sup> software development system support
- MicroBlaze<sup>™</sup> and PicoBlaze<sup>™</sup> embedded processor cores
- Fully compliant 32-/64-bit 33 MHz PCI<sup>™</sup> technology support
- Low-cost QFP and BGA Pb-free (RoHS) packaging options
  - Pin-compatible with the same packages in the Spartan-3A FPGA family

**Table 2: Summary of Spartan-3AN FPGA Attributes**

Device	System Gates	Equivalent Logic Cells	CLBs	Slices	Distributed RAM Bits <sup>(1)</sup>	Block RAM Bits <sup>(1)</sup>	Dedicated Multipliers	DCMs	Maximum User I/O	Maximum Differential I/O Pairs	Bitstream Size <sup>(1)</sup>	In-System Flash Bits
XC3S50AN	50K	1,584	176	704	11K	54K	3	2	144	64	427K	1M
XC3S200AN	200K	4,032	448	1,792	28K	288K	16	4	195	90	1,168K	4M
XC3S400AN	400K	8,064	896	3,584	56K	360K	20	4	311	142	1,842K	4M
XC3S700AN	700K	13,248	1,472	5,888	92K	360K	20	8	372	165	2,669K	8M
XC3S1400AN	1400K	25,344	2,816	11,264	176K	576K	32	8	502	227	4,644K	16M

### Notes:

1. By convention, one Kb is equivalent to 1,024 bits and one Mb is equivalent to 1,024 Kb.

- Sector-based data protection and security features
  - Sector Protect: Write- and erase-protect a sector (changeable)
  - Sector Lockdown: Sector data is unchangeable (permanent)
- 128-byte Security Register
  - Separate from FPGA's unique Device DNA identifier
  - 64-byte factory-programmed identifier unique to the in-system Flash memory
  - 64-byte one-time programmable, user-programmable field
- 100,000 Program/Erase cycles
- 20-year data retention
- Comprehensive programming support
  - In-system prototype programming via JTAG using Xilinx [Platform Cable USB](#) and iMPACT software
  - Product programming support using BPM Microsystems programmers with appropriate programming adapter
  - Design examples demonstrating in-system programming from a Spartan-3AN FPGA application

## I/O Capabilities

The Spartan-3AN FPGA SelectIO interface supports many popular single-ended and differential standards. [Table 4](#) shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional, input-only pins as indicated in [Table 4](#).

Spartan-3AN FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz or 66 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

Spartan-3AN FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 4: Available User I/Os and Differential (Diff) I/O Pairs

Package <sup>(1)</sup>	TQ144 TQG144		FT256 FTG256		FG400 FGG400		FG484 FGG484		FG676 FGG676	
	20 x 20 <sup>(2)</sup>		17 x 17		21 x 21		23 x 23		27 x 27	
Device <sup>(3)</sup>	User	Diff	User	Diff	User	Diff	User	Diff	User	Diff
XC3S50AN	<b>108</b> <sup>(4)</sup> <i>(7)</i>	<b>50</b> <i>(24)</i>	<b>144</b> <i>(32)</i>	<b>64</b> <i>(32)</i>	–	–	–	–	–	–
XC3S200AN	–	–	<b>195</b> <i>(35)</i>	<b>90</b> <i>(50)</i>	–	–	–	–	–	–
XC3S400AN	–	–	<b>195</b> <i>(35)</i>	<b>90</b> <i>(50)</i>	<b>311</b> <i>(63)</i>	<b>142</b> <i>(78)</i>	–	–	–	–
XC3S700AN	–	–	–	–	–	–	<b>372</b> <i>(84)</i>	<b>165</b> <i>(93)</i>	–	–
XC3S1400AN	–	–	–	–	–	–	<b>375</b> <i>(87)</i>	<b>165</b> <i>(93)</i>	<b>502</b> <i>(94)</i>	<b>227</b> <i>(131)</i>

**Notes:**

1. See [Pb and Pb-Free Packaging, page 7](#) for details on Pb and Pb-free packaging options.
2. The footprint for the TQ(G)144 (22 mm x 22 mm) package is larger than the package body.
3. Each Spartan-3AN FPGA has a pin-compatible Spartan-3A FPGA equivalent, although Spartan-3A FPGAs do not have internal SPI flash and offer more part/package combinations.
4. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in *italics* indicates the number of input-only pins. The differential (Diff) input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

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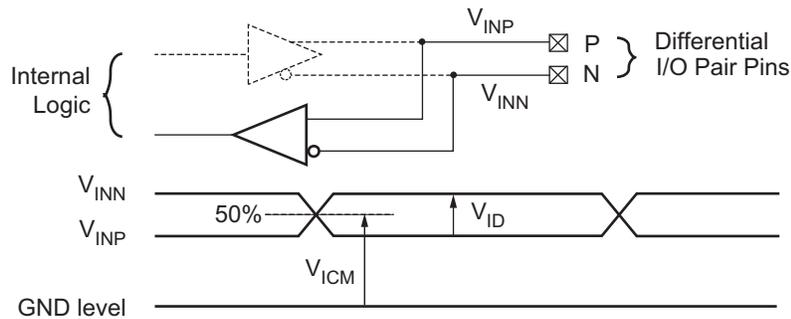
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## Differential I/O Standards

### Differential Input Pairs



$$V_{ICM} = \text{Input common mode voltage} = \frac{V_{INP} + V_{INN}}{2}$$

$$V_{ID} = \text{Differential input voltage} = |V_{INP} - V_{INN}|$$

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Figure 6: Differential Input Voltages

Table 15: Recommended Operating Conditions for User I/Os Using Differential Signal Standards

IOSTANDARD Attribute	$V_{CCO}$ for Drivers <sup>(1)</sup>			$V_{ID}$			$V_{ICM}$ <sup>(2)</sup>		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25 <sup>(3)</sup>	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33 <sup>(3)</sup>	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25 <sup>(4)</sup>	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25 <sup>(3)</sup>	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33 <sup>(3)</sup>	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25 <sup>(5)</sup>	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33 <sup>(5)</sup>	Inputs Only			100	800	1000	0.3	1.2	2.8 <sup>(6)</sup>
RSDS_25 <sup>(3)</sup>	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33 <sup>(3)</sup>	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33 <sup>(3,4,7)</sup>	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25 <sup>(3)</sup>	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33 <sup>(3)</sup>	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18 <sup>(8)</sup>	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18 <sup>(8,9)</sup>	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18 <sup>(8)</sup>	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I <sup>(8)</sup>	1.4	1.5	1.6	100	–	–	0.68	–	0.9
DIFF_HSTL_III <sup>(8)</sup>	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I <sup>(8)</sup>	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II <sup>(8,9)</sup>	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I <sup>(8)</sup>	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II <sup>(8,9)</sup>	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I <sup>(8)</sup>	3.0	3.3	3.6	100	–	–	1.1	–	1.9

## Device DNA Read Endurance

Table 17: Device DNA Identifier Memory Characteristics

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations	30,000,000	Read cycles

## In-System Flash Memory Data Retention, Program/Write Endurance

Table 18: In-System Flash (ISF) Memory Characteristics

Symbol	Description	Minimum <sup>(1)</sup>	Units
ISF_RETENTION	Data retention	20	Years
ISF_ACTIVE	Time that the ISF memory is selected and active. SPI_ACCESS design primitive pins CSB = Low, CLK toggling	2	Years
ISF_PAGE_CYCLES	Number of program/erase cycles, per ISF memory page	100,000	Cycles
ISF_PAGE_REWRITE	Number of cumulative random (non-sequential) page erase/program operations within a sector before pages must be rewritten	10,000	Cycles
ISF_SPR_CYCLES	Number of program/erase cycles for Sector Protection Register	10,000	Cycles
ISF_SEC_CYCLES	Number of program cycles for Sector Lockdown Register per sector, user-programmable field in Security Register, and Power-of-2 Page Size	1	Cycle

**Notes:**

1. Minimum value at which functionality is still guaranteed. Do not exceed these values.

Input Timing Adjustments

Table 26: Input Timing Adjustments by IOSTANDARD

Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
<b>Single-Ended Standards</b>			
LVTTTL	0.62	0.62	ns
LVC MOS33	0.54	0.54	ns
LVC MOS25	0	0	ns
LVC MOS18	0.83	0.83	ns
LVC MOS15	0.60	0.60	ns
LVC MOS12	0.31	0.31	ns
PCI33_3	0.41	0.41	ns
PCI66_3	0.41	0.41	ns
HSTL_I	0.72	0.72	ns
HSTL_III	0.77	0.77	ns
HSTL_I_18	0.69	0.69	ns
HSTL_II_18	0.69	0.69	ns
HSTL_III_18	0.79	0.79	ns
SSTL18_I	0.71	0.71	ns
SSTL18_II	0.71	0.71	ns
SSTL2_I	0.68	0.68	ns
SSTL2_II	0.68	0.68	ns
SSTL3_I	0.78	0.78	ns
SSTL3_II	0.78	0.78	ns

Table 26: Input Timing Adjustments by IOSTANDARD

Convert Input Time from LVC MOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below		Units
	Speed Grade		
	-5	-4	
<b>Differential Standards</b>			
LVDS_25	0.76	0.76	ns
LVDS_33	0.79	0.79	ns
BLVDS_25	0.79	0.79	ns
MINI_LVDS_25	0.78	0.78	ns
MINI_LVDS_33	0.79	0.79	ns
LVPECL_25	0.78	0.78	ns
LVPECL_33	0.79	0.79	ns
RSDS_25	0.79	0.79	ns
RSDS_33	0.77	0.77	ns
TMDS_33	0.79	0.79	ns
PPDS_25	0.79	0.79	ns
PPDS_33	0.79	0.79	ns
DIFF_HSTL_I_18	0.74	0.74	ns
DIFF_HSTL_II_18	0.72	0.72	ns
DIFF_HSTL_III_18	1.05	1.05	ns
DIFF_HSTL_I	0.72	0.72	ns
DIFF_HSTL_III	1.05	1.05	ns
DIFF_SSTL18_I	0.71	0.71	ns
DIFF_SSTL18_II	0.71	0.71	ns
DIFF_SSTL2_I	0.74	0.74	ns
DIFF_SSTL2_II	0.75	0.75	ns
DIFF_SSTL3_I	1.06	1.06	ns
DIFF_SSTL3_II	1.06	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 30 and are based on the operating conditions set forth in Table 10, Table 13, and Table 15.
2. These adjustments are used to convert input path times originally specified for the LVC MOS25 standard to times that correspond to other signal standards.

Table 32: Recommended Number of Simultaneously Switching Outputs per V<sub>CCO</sub>-GND Pair

Signal Standard (IOSTANDARD)		Package Type				
		TQG144		FTG256, FGG400, FGG484, FGG676		
		Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3	
<b>Single-Ended Standards</b>						
LVTTL	Slow	2	20	20	60	60
		4	10	10	41	41
		6	10	10	29	29
		8	6	6	22	22
		12	6	6	13	13
		16	5	5	11	11
		24	4	4	9	9
		Fast	2	10	10	10
	4		6	6	6	6
	6		5	5	5	5
	8		3	3	3	3
	12		3	3	3	3
	16		3	3	3	3
	24		2	2	2	2
	QuietIO		2	40	40	80
		4	24	24	48	48
		6	20	20	36	36
		8	16	16	27	27
		12	12	12	16	16
		16	9	9	13	13
		24	9	9	12	12

Table 32: Recommended Number of Simultaneously Switching Outputs per V<sub>CCO</sub>-GND Pair (Cont'd)

Signal Standard (IOSTANDARD)		Package Type				
		TQG144		FTG256, FGG400, FGG484, FGG676		
		Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3	
LVCMOS33	Slow	2	24	24	76	76
		4	14	14	46	46
		6	11	11	27	27
		8	10	10	20	20
		12	9	9	13	13
		16	8	8	10	10
		24	–	8	–	9
		Fast	2	10	10	10
	4		8	8	8	8
	6		5	5	5	5
	8		4	4	4	4
	12		4	4	4	4
	16		2	2	2	2
	24		–	2	–	2
	QuietIO		2	36	36	76
		4	32	32	46	46
		6	24	24	32	32
		8	16	16	26	26
		12	16	16	18	18
		16	12	12	14	14
		24	–	10	–	10

Table 32: Recommended Number of Simultaneously Switching Outputs per V<sub>CCO</sub>-GND Pair (Cont'd)

Signal Standard (IOSTANDARD)			Package Type			
			TQG144		FTG256, FGG400, FGG484, FGG676	
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3
LVCMOS25	Slow	2	16	16	76	76
		4	10	10	46	46
		6	8	8	33	33
		8	7	7	24	24
		12	6	6	18	18
		16	–	6	–	11
		24	–	5	–	7
	Fast	2	12	12	18	18
		4	10	10	14	14
		6	8	8	6	6
		8	6	6	6	6
		12	3	3	3	3
		16	–	3	–	3
		24	–	2	–	2
	QuietIO	2	36	36	76	76
		4	30	30	60	60
		6	24	24	48	48
		8	20	20	36	36
		12	12	12	36	36
		16	–	12	–	36
		24	–	8	–	8

Table 32: Recommended Number of Simultaneously Switching Outputs per V<sub>CCO</sub>-GND Pair (Cont'd)

Signal Standard (IOSTANDARD)			Package Type				
			TQG144		FTG256, FGG400, FGG484, FGG676		
			Top, Bottom Banks 0,2	Left, Right Banks 1,3	Top, Bottom Banks 0,2	Left, Right Banks 1,3	
LVCMOS18	Slow	2	13	13	64	64	
		4	8	8	34	34	
		6	8	8	22	22	
		8	7	7	18	18	
		12	–	5	–	13	
		16	–	5	–	10	
		24	–	5	–	7	
	Fast	2	13	13	18	18	
		4	8	8	9	9	
		6	7	7	7	7	
		8	4	4	4	4	
		12	–	4	–	4	
		16	–	3	–	3	
		24	–	3	–	3	
	QuietIO	2	30	30	64	64	
		4	24	24	64	64	
		6	20	20	48	48	
		8	16	16	36	36	
		12	–	12	–	36	
		16	–	12	–	24	
		24	–	12	–	24	
	LVCMOS15	Slow	2	12	12	55	55
			4	7	7	31	31
			6	7	7	18	18
8			–	6	–	15	
12			–	5	–	10	
16			–	5	–	10	
24			–	5	–	10	
Fast		2	10	10	25	25	
		4	7	7	10	10	
		6	6	6	6	6	
		8	–	4	–	4	
		12	–	3	–	3	
		16	–	3	–	3	
		24	–	3	–	3	
QuietIO		2	30	30	70	70	
		4	21	21	40	40	
		6	18	18	31	31	
		8	–	12	–	31	
		12	–	12	–	20	
		16	–	12	–	20	
		24	–	12	–	20	

Table 34: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
<b>Clock-to-Output Times</b>						
$T_{SHCKO}$	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	1.69	–	2.01	ns
<b>Setup Times</b>						
$T_{DS}$	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.07	–	–0.02	–	ns
$T_{AS}$	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.18	–	0.36	–	ns
$T_{WS}$	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.30	–	0.59	–	ns
<b>Hold Times</b>						
$T_{DH}$	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	0.13	–	ns
$T_{AH}, T_{WH}$	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	0.01	–	ns
<b>Clock Pulse Width</b>						
$T_{WPH}, T_{WPL}$	Minimum High or Low pulse width at CLK input	0.88	–	1.01	–	ns

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 10.

Table 35: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		-5		-4		
		Min	Max	Min	Max	
<b>Clock-to-Output Times</b>						
$T_{REG}$	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.11	–	4.82	ns
<b>Setup Times</b>						
$T_{SRLDS}$	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.13	–	0.18	–	ns
<b>Hold Times</b>						
$T_{SRLDH}$	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	0.16	–	ns
<b>Clock Pulse Width</b>						
$T_{WPH}, T_{WPL}$	Minimum High or Low pulse width at CLK input	0.90	–	1.01	–	ns

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in Table 10.

Table 52: Master Mode CCLK Output Frequency by ConfigRate Option Setting

Symbol	Description	ConfigRate Setting	Temperature Range	Minimum	Maximum	Units
F <sub>CCLK1</sub>	Equivalent CCLK clock frequency by <b>ConfigRate</b> setting	1 (power-on value)	Commercial	0.400	0.797	MHz
			Industrial		0.847	MHz
F <sub>CCLK3</sub>		3	Commercial	1.20	2.42	MHz
			Industrial		2.57	MHz
F <sub>CCLK6</sub>		6 (default)	Commercial	2.40	4.83	MHz
			Industrial		5.13	MHz
F <sub>CCLK7</sub>		7	Commercial	2.80	5.61	MHz
			Industrial		5.96	MHz
F <sub>CCLK8</sub>		8	Commercial	3.20	6.41	MHz
			Industrial		6.81	MHz
F <sub>CCLK10</sub>		10	Commercial	4.00	8.12	MHz
			Industrial		8.63	MHz
F <sub>CCLK12</sub>		12	Commercial	4.80	9.70	MHz
			Industrial		10.31	MHz
F <sub>CCLK13</sub>		13	Commercial	5.20	10.69	MHz
			Industrial		11.37	MHz
F <sub>CCLK17</sub>		17	Commercial	6.80	13.74	MHz
			Industrial		14.61	MHz
F <sub>CCLK22</sub>		22	Commercial	8.80	18.44	MHz
			Industrial		19.61	MHz
F <sub>CCLK25</sub>	25	Commercial	10.00	20.90	MHz	
		Industrial		22.23	MHz	
F <sub>CCLK27</sub>	27	Commercial	10.80	22.39	MHz	
		Industrial		23.81	MHz	
F <sub>CCLK33</sub>	33	Commercial	13.20	27.48	MHz	
		Industrial		29.23	MHz	
F <sub>CCLK44</sub>	44	Commercial	17.60	37.60	MHz	
		Industrial		40.00	MHz	
F <sub>CCLK50</sub>	50	Commercial	20.00	44.80	MHz	
		Industrial		47.66	MHz	
F <sub>CCLK100</sub>	100	Commercial	40.00	88.68	MHz	
		Industrial		94.34	MHz	

Table 53: Master Mode CCLK Output Minimum Low and High Time

Symbol	Description		ConfigRate Setting																Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T <sub>MCCL</sub> , T <sub>MCCH</sub>	Master Mode CCLK Minimum Low and High Time	Commercial	595	196	98.3	84.5	74.1	58.4	48.9	44.1	34.2	25.6	22.3	20.9	17.1	12.3	10.4	5.3	ns
		Industrial	560	185	92.6	79.8	69.8	55.0	46.0	41.8	32.3	24.2	21.4	20.0	16.2	11.9	10.0	5.0	ns

Table 61: Timing for the JTAG<sup>(2)</sup> Test Access Port

Symbol	Description	All Speed Grades		Units	
		Min	Max		
<b>Clock-to-Output Times</b>					
T <sub>TCKTDO</sub>	The time from the falling transition on the TCK pin to data appearing at the TDO pin	1.0	11.0	ns	
<b>Setup Times</b>					
T <sub>TDITCK</sub>	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	All devices and functions except those shown below	7.0	–	ns
		Boundary-Scan commands (INTEST, EXTEST, SAMPLE) on XC3S700AN and XC3S1400AN FPGAs	11.0		
T <sub>TMSTCK</sub>	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin	7.0	–	ns	
<b>Hold Times</b>					
T <sub>TCKTDI</sub>	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	All functions except those shown below	0	–	ns
		Configuration commands (CFG_IN, ISC_PROGRAM)	2.0		
T <sub>TCKTMS</sub>	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin	0	–	ns	
<b>Clock Timing</b>					
T <sub>CCH</sub>	The High pulse width at the TCK pin	All functions except ISC_DNA command	5	–	ns
T <sub>CCL</sub>	The Low pulse width at the TCK pin		5	–	ns
T <sub>CCHDNA</sub>	The High pulse width at the TCK pin	During ISC_DNA command	10	10,000	ns
T <sub>CCLDNA</sub>	The Low pulse width at the TCK pin		10	10,000	ns
F <sub>TCK</sub>	Frequency of the TCK signal	All operations on XC3S50AN, XC3S200AN, and XC3S400AN FPGAs and for BYPASS or HIGHZ instructions on all FPGAs	0	33	MHz
		All operations on XC3S700AN and XC3S1400AN FPGAs, except for BYPASS or HIGHZ instructions		20	

**Notes:**

1. The numbers in this table are based on the operating conditions set forth in [Table 10](#).
2. For details on JTAG, see Chapter 9, “JTAG Configuration Mode and Boundary-Scan” in [UG332 Spartan-3 Generation Configuration User Guide](#).

Table 64: Maximum User I/O by Package

Device	Package	Maximum User I/Os and Input-Only	Maximum Input-Only	Maximum Differential Pairs	All Possible I/Os by Type					
					I/O	INPUT	DUAL	VREF (1)	CLK	N.C.
XC3S50AN	TQG144	108	7	50	42	2	26	8	30	0
	FTG256	144	32	64	53	20	26	15	30	51
XC3S200AN	FTG256	195	35	90	69	21	52	21	32	0
XC3S400AN	FTG256	195	35	90	69	21	52	21	32	0
	FGG400	311	63	142	155	46	52	26	32	0
XC3S700AN	FGG484	372	84	165	194	61	52	33	32	3
XC3S1400AN	FGG484	375	87	165	195	62	52	34	32	0
	FGG676	502	94	227	313	67	52	38	32	17

**Notes:**

1. Some VREFs are on INPUT pins. See pinout tables for details.

Electronic versions of the package pinout tables and foot-prints are available for download from the Xilinx website at:

[http://www.xilinx.com/support/documentation/data\\_sheets/s3a\\_pin.zip](http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip)

Using a spreadsheet program, the data can be sorted and reformatted according to any specific needs. Similarly, the ASCII-text file is easily parsed by most scripting programs.

## Package Overview

Table 65 shows the five low-cost, space-saving production package styles for the Spartan-3AN family.

Table 65: Spartan-3AN Family Package Options

Package	Leads	Type	Maximum I/Os	Lead Pitch (mm)	Body Area (mm)	Height (mm)
TQ144/TQG144	144	Thin Quad Flat Pack (TQFP)	108	0.5	20 x 20	1.60
FT256/FTG256	256	Fine-pitch Thin Ball Grid Array (FBGA)	195	1.0	17 x 17	1.55
FG400/FGG400	400	Fine-pitch Ball Grid Array (FBGA)	311	1.0	21 x 21	2.43
FG484/FGG484	484	Fine-pitch Ball Grid Array (FBGA)	375	1.0	23 x 23	2.60
FG676/FGG676	676	Fine-pitch Ball Grid Array (FBGA)	502	1.0	27 x 27	2.60

**Notes:**

1. For mass, refer to the MDDS files (see Table 66).

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra “G” in the package style name. For example, the standard “CS484” package becomes “CSG484” when ordered as the Pb-free option. Leaded (Pb) packages are available for selected devices, with the same pinout and without the “G” in the ordering code; See Table 5, page 7 for more information. The mechanical dimensions of the Pb and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 66.

For additional package information, see [UG112: Device Package User Guide](#).

Table 68: Spartan-3AN TQG144 Pinout (Cont'd)

Bank	Pin Name	Pin	Type
2	IO_L05P_2	P46	I/O
2	IO_L06N_2/D6	P49	DUAL
2	IO_L06P_2	P47	I/O
2	IO_L07N_2/D4	P51	DUAL
2	IO_L07P_2/D5	P50	DUAL
2	IO_L08N_2/GCLK15	P55	GCLK
2	IO_L08P_2/GCLK14	P54	GCLK
2	IO_L09N_2/GCLK1	P59	GCLK
2	IO_L09P_2/GCLK0	P57	GCLK
2	IO_L10N_2/GCLK3	P60	GCLK
2	IO_L10P_2/GCLK2	P58	GCLK
2	IO_L11N_2/DOOUT	P64	DUAL
2	IO_L11P_2/AWAKE	P63	PWR MGMT
2	IO_L12N_2/D3	P68	DUAL
2	IO_L12P_2/INIT_B	P67	DUAL
2	IO_L13N_2/D0/DIN/MISO	P71	DUAL
2	IO_L13P_2/D2	P69	DUAL
2	IO_L14N_2/CCLK	P72	DUAL
2	IO_L14P_2/D1	P70	DUAL
2	IP_2/VREF_2	P53	VREF
2	VCCO_2	P40	VCCO
2	VCCO_2	P61	VCCO
3	IO_L01N_3	P6	I/O
3	IO_L01P_3	P4	I/O
3	IO_L02N_3	P5	I/O
3	IO_L02P_3	P3	I/O
3	IO_L03N_3	P8	I/O
3	IO_L03P_3	P7	I/O
3	IO_L04N_3/VREF_3	P11	VREF
3	IO_L04P_3	P10	I/O
3	IO_L05N_3/LHCLK1	P13	LHCLK
3	IO_L05P_3/LHCLK0	P12	LHCLK
3	IO_L06N_3/IRDY2/LHCLK3	P16	LHCLK
3	IO_L06P_3/LHCLK2	P15	LHCLK
3	IO_L07N_3/LHCLK5	P20	LHCLK
3	IO_L07P_3/LHCLK4	P18	LHCLK
3	IO_L08N_3/LHCLK7	P21	LHCLK
3	IO_L08P_3/TRDY2/LHCLK6	P19	LHCLK
3	IO_L09N_3	P25	I/O
3	IO_L09P_3	P24	I/O
3	IO_L10N_3	P29	I/O
3	IO_L10P_3	P27	I/O

Table 68: Spartan-3AN TQG144 Pinout (Cont'd)

Bank	Pin Name	Pin	Type
3	IO_L11N_3	P30	I/O
3	IO_L11P_3	P28	I/O
3	IO_L12N_3	P32	I/O
3	IO_L12P_3	P31	I/O
3	IP_L13N_3/VREF_3	P35	VREF
3	IP_L13P_3	P33	INPUT
3	VCCO_3	P14	VCCO
3	VCCO_3	P23	VCCO
GND	GND	P9	GND
GND	GND	P17	GND
GND	GND	P26	GND
GND	GND	P34	GND
GND	GND	P56	GND
GND	GND	P65	GND
GND	GND	P81	GND
GND	GND	P89	GND
GND	GND	P100	GND
GND	GND	P106	GND
GND	GND	P118	GND
GND	GND	P128	GND
GND	GND	P137	GND
VCCAUX	SUSPEND	P74	PWR MGMT
VCCAUX	DONE	P73	CONFIG
VCCAUX	PROG_B	P144	CONFIG
VCCAUX	TCK	P109	JTAG
VCCAUX	TDI	P2	JTAG
VCCAUX	TDO	P107	JTAG
VCCAUX	TMS	P1	JTAG
VCCAUX	VCCAUX	P36	VCCAUX
VCCAUX	VCCAUX	P66	VCCAUX
VCCAUX	VCCAUX	P108	VCCAUX
VCCAUX	VCCAUX	P133	VCCAUX
VCCINT	VCCINT	P22	VCCINT
VCCINT	VCCINT	P52	VCCINT
VCCINT	VCCINT	P94	VCCINT
VCCINT	VCCINT	P122	VCCINT

Table 70: Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN) (Cont'd)

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
1	IO_L10P_1	IO_L10P_1/A8	J12	DUAL
1	IO_L11N_1/RHCLK1	IO_L11N_1/RHCLK1	K14	RHCLK
1	IO_L11P_1/RHCLK0	IO_L11P_1/RHCLK0	K15	RHCLK
1	IO_L12N_1/TRDY1/RHCLK3	IO_L12N_1/TRDY1/RHCLK3	J16	RHCLK
1	IO_L12P_1/RHCLK2	IO_L12P_1/RHCLK2	K16	RHCLK
1	IO_L14N_1/RHCLK5	IO_L14N_1/RHCLK5	H14	RHCLK
1	IO_L14P_1/RHCLK4	IO_L14P_1/RHCLK4	J14	RHCLK
1	IO_L15N_1/RHCLK7	IO_L15N_1/RHCLK7	H16	RHCLK
1	IO_L15P_1/IRDY1/RHCLK6	IO_L15P_1/IRDY1/RHCLK6	H15	RHCLK
1	N.C.	IO_L16N_1/A11	F16	DUAL
1	N.C.	IO_L16P_1/A10	G16	DUAL
1	N.C.	IO_L17N_1/A13	G14	DUAL
1	N.C.	IO_L17P_1/A12	H13	DUAL
1	N.C.	IO_L18N_1/A15	F15	DUAL
1	N.C.	IO_L18P_1/A14	E16	DUAL
1	N.C.	IO_L19N_1/A17	F14	DUAL
1	N.C.	IO_L19P_1/A16	G13	DUAL
1	IO_L20N_1	IO_L20N_1/A19	F13	DUAL
1	IO_L20P_1	IO_L20P_1/A18	E14	DUAL
1	IO_L22N_1	IO_L22N_1/A21	D15	DUAL
1	IO_L22P_1	IO_L22P_1/A20	D16	DUAL
1	IO_L23N_1	IO_L23N_1/A23	D14	DUAL
1	IO_L23P_1	IO_L23P_1/A22	E13	DUAL
1	IO_L24N_1	IO_L24N_1/A25	C15	DUAL
1	IO_L24P_1	IO_L24P_1/A24	C16	DUAL
1	IP_L04N_1/VREF_1	IP_L04N_1/VREF_1	K12	VREF
1	IP_L04P_1	IP_L04P_1	K11	INPUT
1	N.C.	IP_L09N_1	J11	INPUT
1	N.C.	IP_L09P_1/VREF_1	J10	VREF
1	IP_L13N_1	IP_L13N_1	H11	INPUT
1	IP_L13P_1	IP_L13P_1	H10	INPUT
1	IP_L21N_1	IP_L21N_1	G11	INPUT
1	IP_L21P_1/VREF_1	IP_L21P_1/VREF_1	G12	VREF
1	IP_L25N_1	IP_L25N_1	F11	INPUT
1	IP_L25P_1/VREF_1	IP_L25P_1/VREF_1	F12	VREF
1	VCCO_1	VCCO_1	E15	VCCO
1	VCCO_1	VCCO_1	H12	VCCO
1	VCCO_1	VCCO_1	J15	VCCO
1	VCCO_1	VCCO_1	N15	VCCO

Table 70: Spartan-3AN FTG256 Pinout (XC3S50AN, XC3S200AN, XC3S400AN) (Cont'd)

Bank	XC3S50AN Pin Name	XC3S200AN/XC3S400AN Pin Name	FTG256 Ball	Type
2	IP_2	IP_2	L7	INPUT
2	IP_2	IP_2	L8	INPUT
2	IP_2/VREF_2	IP_2/VREF_2	L9	VREF
2	IP_2/VREF_2	IP_2/VREF_2	L10	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M7	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M8	VREF
2	IP_2/VREF_2	IP_2/VREF_2	M11	VREF
2	IP_2/VREF_2	IP_2/VREF_2	N5	VREF
2	VCCO_2	VCCO_2	M9	VCCO
2	VCCO_2	VCCO_2	R4	VCCO
2	VCCO_2	VCCO_2	R8	VCCO
2	VCCO_2	VCCO_2	R12	VCCO
3	IO_L01N_3	IO_L01N_3	C1	I/O
3	IO_L01P_3	IO_L01P_3	C2	I/O
3	IO_L02N_3	IO_L02N_3	D3	I/O
3	IO_L02P_3	IO_L02P_3	D4	I/O
3	IO_L03N_3	IO_L03N_3	E1	I/O
3	IO_L03P_3	IO_L03P_3	D1	I/O
3	N.C.	IO_L05N_3	E2	I/O
3	N.C.	IO_L05P_3	E3	I/O
3	N.C.	IO_L07N_3	G4	I/O
3	N.C.	IO_L07P_3	F3	I/O
3	IO_L08N_3/VREF_3	IO_L08N_3/VREF_3	G1	VREF
3	IO_L08P_3	IO_L08P_3	F1	I/O
3	N.C.	IO_L09N_3	H4	I/O
3	N.C.	IO_L09P_3	G3	I/O
3	N.C.	IO_L10N_3	H5	I/O
3	N.C.	IO_L10P_3	H6	I/O
3	IO_L11N_3/LHCLK1	IO_L11N_3/LHCLK1	H1	LHCLK
3	IO_L11P_3/LHCLK0	IO_L11P_3/LHCLK0	G2	LHCLK
3	IO_L12N_3/IRDY2/LHCLK3	IO_L12N_3/IRDY2/LHCLK3	J3	LHCLK
3	IO_L12P_3/LHCLK2	IO_L12P_3/LHCLK2	H3	LHCLK
3	IO_L14N_3/LHCLK5	IO_L14N_3/LHCLK5	J1	LHCLK
3	IO_L14P_3/LHCLK4	IO_L14P_3/LHCLK4	J2	LHCLK
3	IO_L15N_3/LHCLK7	IO_L15N_3/LHCLK7	K1	LHCLK
3	IO_L15P_3/TRDY2/LHCLK6	IO_L15P_3/TRDY2/LHCLK6	K3	LHCLK
3	N.C.	IO_L16N_3	L2	I/O
3	N.C.	IO_L16P_3/VREF_3	L1	VREF
3	N.C.	IO_L17N_3	J6	I/O
3	N.C.	IO_L17P_3	J4	I/O

## FGG400: 400-Ball Fine-Pitch Ball Grid Array

The 400-ball fine-pitch ball grid array, FGG400, supports the XC3S400AN FPGA as shown in [Table 76](#) and [Figure 22](#).

[Table 76](#) lists all the FGG400 package pins. They are sorted by bank number and then by pin name. Pins that form a differential I/O pair appear together in the table. The table also shows the pin number for each pin and the pin type (as defined in [Table 62](#)).

An electronic version of this package pinout table and footprint diagram is available for download from the Xilinx website at: [www.xilinx.com/support/documentation/data\\_sheets/s3a\\_pin.zip](http://www.xilinx.com/support/documentation/data_sheets/s3a_pin.zip).

### Pinout Table

Table 76: Spartan-3AN FGG400 Pinout

Bank	Pin Name	FGG400 Ball	Type
0	IO_L01N_0	A18	I/O
0	IO_L01P_0	B18	I/O
0	IO_L02N_0	C17	I/O
0	IO_L02P_0/VREF_0	D17	VREF
0	IO_L03N_0	E15	I/O
0	IO_L03P_0	D16	I/O
0	IO_L04N_0	A17	I/O
0	IO_L04P_0/VREF_0	B17	VREF
0	IO_L05N_0	A16	I/O
0	IO_L05P_0	C16	I/O
0	IO_L06N_0	C15	I/O
0	IO_L06P_0	D15	I/O
0	IO_L07N_0	A14	I/O
0	IO_L07P_0	C14	I/O
0	IO_L08N_0	A15	I/O
0	IO_L08P_0	B15	I/O
0	IO_L09N_0	F13	I/O
0	IO_L09P_0	E13	I/O
0	IO_L10N_0/VREF_0	C13	VREF
0	IO_L10P_0	D14	I/O
0	IO_L11N_0	C12	I/O
0	IO_L11P_0	B13	I/O
0	IO_L12N_0	F12	I/O
0	IO_L12P_0	D12	I/O
0	IO_L13N_0	A12	I/O
0	IO_L13P_0	B12	I/O
0	IO_L14N_0	C11	I/O
0	IO_L14P_0	B11	I/O
0	IO_L15N_0/GCLK5	E11	GCLK
0	IO_L15P_0/GCLK4	D11	GCLK
0	IO_L16N_0/GCLK7	C10	GCLK

Table 76: Spartan-3AN FGG400 Pinout (Cont'd)

Bank	Pin Name	FGG400 Ball	Type
0	IO_L16P_0/GCLK6	A10	GCLK
0	IO_L17N_0/GCLK9	E10	GCLK
0	IO_L17P_0/GCLK8	D10	GCLK
0	IO_L18N_0/GCLK11	A8	GCLK
0	IO_L18P_0/GCLK10	A9	GCLK
0	IO_L19N_0	C9	I/O
0	IO_L19P_0	B9	I/O
0	IO_L20N_0	C8	I/O
0	IO_L20P_0	B8	I/O
0	IO_L21N_0	D8	I/O
0	IO_L21P_0	C7	I/O
0	IO_L22N_0/VREF_0	F9	VREF
0	IO_L22P_0	E9	I/O
0	IO_L23N_0	F8	I/O
0	IO_L23P_0	E8	I/O
0	IO_L24N_0	A7	I/O
0	IO_L24P_0	B7	I/O
0	IO_L25N_0	C6	I/O
0	IO_L25P_0	A6	I/O
0	IO_L26N_0	B5	I/O
0	IO_L26P_0	A5	I/O
0	IO_L27N_0	F7	I/O
0	IO_L27P_0	E7	I/O
0	IO_L28N_0	D6	I/O
0	IO_L28P_0	C5	I/O
0	IO_L29N_0	C4	I/O
0	IO_L29P_0	A4	I/O
0	IO_L30N_0	B3	I/O
0	IO_L30P_0	A3	I/O
0	IO_L31N_0	F6	I/O
0	IO_L31P_0	E6	I/O

Bank 0											Bank 1	
12	13	14	15	16	17	18	19	20	21	22		
I/O L18P_0 GCLK6	I/O L16N_0	I/O L13N_0	I/O L12N_0 VREF_0	I/O L12P_0	I/O L10N_0	I/O L05N_0	I/O L06N_0	I/O L03N_0	TCK	GND	A	
GND	I/O L16P_0	VCCO_0	I/O L13P_0	GND	I/O L10P_0	VCCO_0	I/O L06P_0 VREF_0	I/O L03P_0	I/O L45N_1 A23	I/O L45P_1 A22	B	
I/O L17P_0 GCLK4	I/O L15N_0	I/O L09P_0	I/O L11N_0	I/O L08N_0	I/O L07N_0	I/O L05P_0	I/O L02N_0	GND	I/O L44N_1 A21	I/O L44P_1 A20	C	
VCCAUX	I/O L15P_0	GND	I/O L11P_0	I/O L08P_0	I/O L07P_0	I/O L01N_0	I/O L02P_0 VREF_0	I/O L42N_1	I/O L42P_1	I/O L41N_1	D	
I/O L17N_0 GCLK5	I/O L14N_0	I/O L09N_0	I/O L04P_0	INPUT	I/O L01P_0	VCCAUX	TDO	I/O L38P_1	VCCO_1	I/O L41P_1	E	
INPUT	I/O L14P_0	VCCO_0	I/O L04N_0	INPUT	GND	I/O L40N_1	I/O L40P_1	I/O L38N_1	I/O L34N_1 A19	I/O L34P_1 A18	F	
INPUT	INPUT	INPUT	INPUT	INPUT	I/O L46N_1 A25	I/O L46P_1 A24	I/O L36P_1	I/O L36N_1	GND	I/O L30N_1 A15	G	
INPUT VREF_0	INPUT	INPUT	INPUT L47N_1	INPUT L47P_1 VREF_1	INPUT L39P_1	INPUT L39N_1	I/O L37N_1	I/O L33N_1 A17	I/O L33P_1 A16	I/O L30P_1 A14	H	
VCCINT	GND	GND	INPUT L43N_1 VREF_1	INPUT L43P_1	VCCO_1	I/O L37P_1	GND	I/O L29N_1 A13	I/O L29P_1 A12	I/O L26N_1 A11	J	
GND	VCCINT	INPUT L35P_1 VREF_1	INPUT L35N_1	INPUT L31N_1	I/O L32P_1	I/O L32N_1	I/O L25N_1 RHCLK7	I/O L25P_1 IRDY1 RHCLK6	VCCO_1	I/O L26P_1 A10	K	
VCCINT	GND	VCCINT	INPUT L31P_1	INPUT L27N_1	GND	I/O L28P_1	I/O L28N_1	I/O L22N_1 TRDY1 RHCLK3	I/O L22P_1 RHCLK2	I/O L21N_1 RHCLK1	L	
GND	VCCINT	GND	INPUT L27P_1 VREF_1	INPUT L23N_1	INPUT L23P_1	I/O L24P_1 RHCLK4	VCCAUX	I/O L24N_1 RHCLK5	GND	I/O L21P_1 RHCLK0	M	
VCCINT	GND	VCCINT	INPUT L16P_1	INPUT L16N_1 VREF_1	INPUT L20N_1 A9	I/O L20P_1 A8	I/O L19N_1 A7	I/O L19P_1 A6	I/O L18N_1 A5	I/O L18P_1 A4	N	
INPUT	VCCINT	GND	INPUT L08P_1	INPUT L08N_1	VCCO_1	I/O L17N_1 A3	GND	I/O L15P_1	VCCO_1	I/O L15N_1 VREF_1	P	
INPUT VREF_2	INPUT VREF_2	INPUT VREF_2	INPUT L04P_1	INPUT L04N_1 VREF_1	INPUT L12P_1	INPUT L12N_1 VREF_1	I/O L17P_1 A2	I/O L13P_1	I/O L14P_1	I/O L14N_1	R	
GND	INPUT	INPUT	INPUT VREF_2	INPUT VREF_2	I/O L03P_1 A0	I/O L03N_1 A1	I/O L13N_1	I/O L11P_1	GND	I/O L11N_1	T	
I/O L20N_2 GCLK3	I/O L26N_2 D3	VCCO_2	INPUT	INPUT ◆	GND	SUSPEND	I/O L10N_1	I/O L10P_1	I/O L09N_1	I/O L09P_1	U	
I/O L20P_2 GCLK2	I/O L26P_2 INIT_B	I/O L30P_2	I/O L30N_2	I/O L31N_2	I/O L33N_2	VCCAUX	I/O L06P_1	I/O L06N_1	VCCO_1	I/O L07N_1	V	
I/O L18P_2 GCLK14	I/O L23P_2	GND	I/O L25P_2	I/O L31P_2	I/O L34N_2	I/O L33P_2	I/O L02P_1 LDC1	I/O L02N_1 LDC0	I/O L05N_1	I/O L07P_1	W	
I/O L18N_2 GCLK15	I/O L21N_2	I/O L23N_2	I/O L25N_2	I/O L27N_2	I/O L28N_2 D1	I/O L34P_2	DONE	GND	I/O L01N_1 LDC2	I/O L05P_1	Y	
I/O L19P_2 GCLK0	VCCO_2	I/O L22P_2	I/O L24N_2 DOUT	GND	I/O L28P_2 D2	VCCO_2	I/O L32N_2	I/O L36N_2 CCLK	I/O L35N_2	I/O L01P_1 HDC	A A	
I/O L19N_2 GCLK1	I/O L21P_2	I/O L22N_2 MOSI CSI_B	I/O L24P_2 AWAKE	I/O L27P_2	I/O L29P_2	I/O L29N_2	I/O L32P_2	I/O L36P_2 D0 DIN/MISO	I/O L35P_2	GND	A B	
Bank 2												

Right Half of FGG484 Package (Top View)

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Figure 23: FGG484 Package Footprint (Top View)

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
0	IO_L33N_0	B10	I/O
0	IO_L33P_0	A10	I/O
0	IO_L34N_0	D10	I/O
0	IO_L34P_0	C10	I/O
0	IO_L35N_0	H12	I/O
0	IO_L35P_0	G12	I/O
0	IO_L36N_0	B9	I/O
0	IO_L36P_0	A9	I/O
0	IO_L37N_0	D9	I/O
0	IO_L37P_0	E10	I/O
0	IO_L38N_0	B8	I/O
0	IO_L38P_0	A8	I/O
0	IO_L39N_0	K12	I/O
0	IO_L39P_0	J12	I/O
0	IO_L40N_0	D8	I/O
0	IO_L40P_0	C8	I/O
0	IO_L41N_0	C6	I/O
0	IO_L41P_0	B6	I/O
0	IO_L42N_0	C7	I/O
0	IO_L42P_0	B7	I/O
0	IO_L43N_0	K11	I/O
0	IO_L43P_0	J11	I/O
0	IO_L44N_0	D6	I/O
0	IO_L44P_0	C5	I/O
0	IO_L45N_0	B4	I/O
0	IO_L45P_0	A4	I/O
0	IO_L46N_0	H10	I/O
0	IO_L46P_0	G10	I/O
0	IO_L47N_0	H9	I/O
0	IO_L47P_0	G9	I/O
0	IO_L48N_0	E7	I/O
0	IO_L48P_0	F7	I/O
0	IO_L51N_0	B3	I/O
0	IO_L51P_0	A3	I/O
0	IO_L52N_0/PUDC_B	G8	DUAL
0	IO_L52P_0/VREF_0	F8	VREF
0	IP_0	A5	INPUT
0	IP_0	A7	INPUT
0	IP_0	A13	INPUT
0	IP_0	A17	INPUT

Table 82: Spartan-3AN FGG676 Pinout (Cont'd)

Bank	Pin Name	FGG676 Ball	Type
0	IP_0	A23	INPUT
0	IP_0	C4	INPUT
0	IP_0	D12	INPUT
0	IP_0	D15	INPUT
0	IP_0	D19	INPUT
0	IP_0	E11	INPUT
0	IP_0	E18	INPUT
0	IP_0	E20	INPUT
0	IP_0	F10	INPUT
0	IP_0	G14	INPUT
0	IP_0	G16	INPUT
0	IP_0	H13	INPUT
0	IP_0	H18	INPUT
0	IP_0	J10	INPUT
0	IP_0	J13	INPUT
0	IP_0	J15	INPUT
0	IP_0/VREF_0	D7	VREF
0	IP_0/VREF_0	D14	VREF
0	IP_0/VREF_0	G11	VREF
0	IP_0/VREF_0	J17	VREF
0	N.C.	A24	N.C.
0	N.C.	B24	N.C.
0	N.C.	D5	N.C.
0	N.C.	E9	N.C.
0	N.C.	F18	N.C.
0	N.C.	E6	N.C.
0	N.C.	F9	N.C.
0	N.C.	G18	N.C.
0	VCCO_0	B5	VCCO
0	VCCO_0	B11	VCCO
0	VCCO_0	B16	VCCO
0	VCCO_0	B22	VCCO
0	VCCO_0	E8	VCCO
0	VCCO_0	E13	VCCO
0	VCCO_0	E19	VCCO
0	VCCO_0	H11	VCCO
0	VCCO_0	H16	VCCO
1	IO_L01N_1/LDC2	Y21	DUAL
1	IO_L01P_1/HDC	Y20	DUAL
1	IO_L02N_1/LDC0	AD25	DUAL

Bank 0														Bank 1																	
14	15	16	17	18	19	20	21	22	23	24	25	26		14	15	16	17	18	19	20	21	22	23	24	25	26					
I/O L26N_0 GCLK7	I/O L23N_0	GND	INPUT	I/O L18N_0	I/O L15N_0	I/O L14N_0	GND	I/O L07N_0	INPUT	N.C.	TCK	GND	A	I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E		
I/O L26P_0 GCLK6	I/O L23P_0	VCCO_0	I/O L19N_0	I/O L18P_0	I/O L15P_0	I/O L14P_0 VREF_0	I/O L09N_0	VCCO_0	I/O L07P_0	N.C.	INPUT L65N_1	INPUT L65P_1 VREF_1	B	I/O L24P_0	I/O L20N_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E				
GND	I/O L22N_0	I/O L21N_0	I/O L21P_0	I/O L17N_0	GND	I/O L11N_0	I/O L09P_0	I/O L05N_0	I/O L06N_0	GND	I/O L63N_1 A23	I/O L63P_1 A22	C	I/O L24N_0	I/O L20P_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E				
INPUT VREF_0	INPUT	I/O L22P_0	I/O L21P_0	I/O L17P_0	INPUT	I/O L11P_0	I/O L10N_0	I/O L05P_0	I/O L06P_0	I/O L61N_1	I/O L61P_1	I/O L60N_1	D	I/O L24N_0	I/O L20P_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E				
I/O L24P_0	I/O L20N_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E	I/O L24N_0	I/O L20P_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E				
I/O L24N_0	I/O L20P_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E	I/O L24N_0	I/O L20P_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E				
INPUT	I/O L16P_0	INPUT	I/O L08N_0	N.C.	I/O L02P_0 VREF_0	I/O L01P_0	I/O L64N_1 A25	I/O L58N_1	I/O L51P_1	I/O L51N_1	INPUT L52N_1 VREF_1	INPUT L52P_1	G	I/O L24N_0	I/O L20P_0 VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E				
GND	I/O L16N_0	VCCO_0	I/O L08P_0	INPUT	GND	I/O L64P_1 A24	I/O L62N_1 A21	VCCO_1	INPUT L48P_1	INPUT L48N_1	INPUT L44N_1	INPUT L44P_1 VREF_1	H	I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E		
I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E	I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E
I/O L25P_0 GCLK4	VCCINT	I/O L12N_0	GND	I/O L57N_1	I/O L57P_1	I/O L53N_1	I/O L50N_1	I/O L46N_1	I/O L46P_1	INPUT L40P_1	I/O L41P_1	I/O L41N_1	K	I/O L25N_0 GCLK5	INPUT	I/O L12P_0	INPUT VREF_0	VCCAUX	I/O L13N_0	INPUT	VCCO_0	INPUT	I/O L10P_0	VCCAUX	TDO	I/O L56P_1	VCCO_1	I/O L60P_1	E		
VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND	L	I/O L25P_0 GCLK4	VCCINT	I/O L12N_0	GND	I/O L57N_1	I/O L57P_1	I/O L53N_1	I/O L50N_1	I/O L46N_1	I/O L46P_1	INPUT L40P_1	I/O L41P_1	I/O L41N_1	K				
GND	VCCINT	GND	VCCINT	I/O L47N_1	I/O L47P_1	I/O L42N_1 A17	I/O L45P_1	I/O L45N_1	I/O L38N_1 A13	INPUT L36P_1 VREF_1	I/O L35N_1 A11	I/O L35P_1 A10	M	VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND	L				
VCCINT	GND	VCCINT	I/O L39N_1 A15	I/O L39P_1 A14	I/O L34N_1 RHCLK7	I/O L42P_1 A16	I/O L37N_1	VCCO_1	INPUT L36N_1	I/O L33N_1 RHCLK5	INPUT L32N_1	INPUT L32P_1	N	GND	VCCINT	GND	VCCINT	I/O L47N_1	I/O L47P_1	I/O L42N_1 A17	I/O L45P_1	I/O L45N_1	I/O L38N_1 A13	INPUT L36P_1 VREF_1	I/O L35N_1 A11	I/O L35P_1 A10	M				
VCCINT	VCCINT	GND	VCCAUX	I/O L34P_1 IRDY1 RHCLK6	GND	I/O L30N_1 RHCLK1	I/O L30P_1 RHCLK0	I/O L37P_1	I/O L33P_1 RHCLK4	GND	I/O L31N_1 TRDY1 RHCLK3	I/O L31P_1 RHCLK2	P	VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND	L				
VCCINT	GND	VCCINT	I/O L27N_1 A7	I/O L27P_1 A6	I/O L22P_1	I/O L22N_1	I/O L25P_1 A2	I/O L25N_1 A3	INPUT L28P_1 VREF_1	INPUT L28N_1	I/O L29P_1 A8	I/O L29N_1 A9	R	VCCINT	VCCINT	GND	VCCAUX	I/O L34P_1 IRDY1 RHCLK6	GND	I/O L30N_1 RHCLK1	I/O L30P_1 RHCLK0	I/O L37P_1	I/O L33P_1 RHCLK4	GND	I/O L31N_1 TRDY1 RHCLK3	I/O L31P_1 RHCLK2	P				
GND	VCCINT	GND	I/O L17N_1	I/O L17P_1	VCCO_1	I/O L14N_1	GND	VCCAUX	I/O L26P_1 A4	I/O L26N_1 A5	VCCO_1	GND	T	VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND	L				
VCCAUX	I/O L35N_2	I/O L42N_2	GND	I/O L12N_1	I/O L12P_1	I/O L10N_1	I/O L14P_1	I/O L21N_1	I/O L23P_1	I/O L23N_1 VREF_1	INPUT L24P_1	INPUT L24N_1 VREF_1	U	GND	VCCINT	GND	VCCINT	I/O L47N_1	I/O L47P_1	I/O L42N_1 A17	I/O L45P_1	I/O L45N_1	I/O L38N_1 A13	INPUT L36P_1 VREF_1	I/O L35N_1 A11	I/O L35P_1 A10	M				
I/O L31P_2	I/O L35P_2	I/O L42P_2	I/O L46N_2	I/O L08P_1	I/O L08N_1	SUSPEND	I/O L10P_1	I/O L18N_1	I/O L21P_1	I/O L19P_1	I/O L19N_1	INPUT L20N_1 VREF_1	V	VCCINT	GND	VCCINT	I/O L55N_1	I/O L55P_1	VCCO_1	I/O L53P_1	GND	I/O L50P_1	INPUT L40N_1	I/O L38P_1 A12	VCCO_1	GND	L				
GND	I/O L31N_2	VCCO_2	I/O L46P_2	N.C.	GND	I/O L04P_1	I/O L04N_1	VCCO_1	I/O L18P_1	GND	INPUT L16P_1	INPUT L20P_1	W	I/O L31P_2	I/O L35P_2	I/O L42P_2	I/O L46N_2	I/O L08P_1	I/O L08N_1	SUSPEND	I/O L10P_1	I/O L18N_1	I/O L21P_1	I/O L19P_1	I/O L19N_1	INPUT L20N_1 VREF_1	V				
I/O L27P_2 GCLK0	I/O L34N_2 D3	INPUT VREF_2	I/O L43N_2	N.C.	N.C.	I/O L01P_1 HDC	I/O L01N_1 LDC2	I/O L13P_1	I/O L13N_1	I/O L15P_1	I/O L15N_1	INPUT L16N_1	Y	GND	VCCINT	GND	VCCINT	I/O L47N_1	I/O L47P_1	I/O L42N_1 A17	I/O L45P_1	I/O L45N_1	I/O L38N_1 A13	INPUT L36P_1 VREF_1	I/O L35N_1 A11	I/O L35P_1 A10	M				
I/O L27N_2 GCLK1	I/O L34P_2 INIT_B	GND	I/O L43P_2	I/O L47N_2	INPUT	INPUT VREF_2	GND	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	GND	A	I/O L27N_2 GCLK1	I/O L34P_2 INIT_B	GND	I/O L43P_2	I/O L47N_2	INPUT	INPUT VREF_2	GND	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	GND	A				
VCCO_2	I/O L30N_2 MOSI CSL_B	I/O L38N_2	INPUT	I/O L47P_2	VCCO_2	INPUT	DONE	VCCAUX	I/O L07P_1	I/O L07N_1 VREF_1	VCCO_1	I/O L06N_1	A	I/O L27N_2 GCLK1	I/O L34P_2 INIT_B	GND	I/O L43P_2	I/O L47N_2	INPUT	INPUT VREF_2	GND	I/O L09P_1	I/O L09N_1	I/O L11P_1	I/O L11N_1	GND	A				
I/O L29N_2	I/O L30P_2	I/O L38P_2	INPUT	INPUT	I/O L40N_2	I/O L41N_2	I/O L45N_2	N.C.	I/O L03P_1 A0	I/O L03N_1 A1	I/O L05N_1	I/O L06P_1	C	VCCO_2	I/O L30N_2 MOSI CSL_B	I/O L38N_2	INPUT	I/O L47P_2	VCCO_2	INPUT	DONE	VCCAUX	I/O L07P_1	I/O L07N_1 VREF_1	VCCO_1	I/O L06N_1	A				
I/O L29P_2	I/O L32P_2 AWAKE	INPUT	I/O L33N_2	GND	I/O L40P_2	I/O L41P_2	I/O L44N_2	I/O L45P_2	N.C.	GND	I/O L02N_1 LDC0	I/O L05P_1	D	I/O L29N_2	I/O L30P_2	I/O L38P_2	INPUT	INPUT	I/O L40N_2	I/O L41N_2	I/O L45N_2	N.C.	I/O L03P_1 A0	I/O L03N_1 A1	I/O L05N_1	I/O L06P_1	C				
I/O L28N_2 GCLK3	I/O L32N_2 DOUT	VCCO_2	I/O L33P_2	I/O L36N_2 D1	I/O L37N_2	I/O L39N_2	I/O L44P_2	VCCO_2	I/O L48N_2	I/O L52N_2 CCLK	I/O L51N_2	I/O L02P_1 LDC1	E	I/O L29P_2	I/O L32P_2 AWAKE	INPUT	I/O L33N_2	GND	I/O L40P_2	I/O L41P_2	I/O L44N_2	I/O L45P_2	N.C.	GND	I/O L02N_1 LDC0	I/O L05P_1	D				
I/O L28P_2 GCLK2	INPUT VREF_2	GND	INPUT VREF_2	I/O L36P_2 D2	I/O L37P_2	I/O L39P_2	GND	INPUT VREF_2	I/O L48P_2	I/O L52P_2 DO DIN/MISO	I/O L51P_2	GND	F	I/O L28N_2 GCLK3	I/O L32N_2 DOUT	VCCO_2	I/O L33P_2	I/O L36N_2 D1	I/O L37N_2	I/O L39N_2	I/O L44P_2	VCCO_2	I/O L48N_2	I/O L52N_2 CCLK	I/O L51N_2	I/O L02P_1 LDC1	E				
I/O L28P_2 GCLK2	INPUT VREF_2	GND	INPUT VREF_2	I/O L36P_2 D2	I/O L37P_2	I/O L39P_2	GND	INPUT VREF_2	I/O L48P_2	I/O L52P_2 DO DIN/MISO	I/O L51P_2	GND	F	I/O L28P_2 GCLK2	INPUT VREF_2	GND	INPUT VREF_2	I/O L36P_2 D2	I/O L37P_2	I/O L39P_2	GND	INPUT VREF_2	I/O L48P_2	I/O L52P_2 DO DIN/MISO	I/O L51P_2	GND	F				

Right Half of FGG676 Package (Top View)

Figure 24: FGG676 Package Footprint (Top View)

DS557-4\_08\_030911

## Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/26/07	1.0	Initial release.
08/16/07	2.0	Updated for Production release of initial device. Noted that family is available in Pb-free packages only.
09/12/07	2.0.1	Minor updates to text.
09/24/07	2.1	Update thermal characteristics in <a href="#">Table 67</a> .
12/12/07	3.0	Updated to Production status with Production release of final family member, XC3S50AN. Noted that non-Pb-free packages may be available for selected devices. Updated thermal characteristics in <a href="#">Table 67</a> . Updated links.
06/02/08	3.1	Add <a href="#">Package Overview</a> section. Removed VREF and INPUT designations and diamond symbols on unconnected N.C. pins for XC3S700AN FGG484 in <a href="#">Table 78</a> and <a href="#">Figure 22</a> and for XC3S1400AN FGG676 in <a href="#">Table 82</a> and <a href="#">Figure 23</a> .
11/19/09	3.2	Renamed package 'Footprint Area' to 'Body Area' throughout document. Noted in <a href="#">Introduction</a> that references to Pb-free package code also apply to the Pb package. Added Pb packages to <a href="#">Table 65</a> and <a href="#">Table 66</a> . Changed Body Area of TQ144/TQG144 packages in <a href="#">Table 65</a> . Corrected bank designation for SUSPEND to VCCAUX. Noted that non-Pb-free (Pb) packages are available for selected devices. Updated <a href="#">Table 79</a> and <a href="#">Figure 22</a> for I/O vs. Input pin counts.
12/02/10	4.0	Upgraded <a href="#">Notice of Disclaimer</a> .
04/01/11	4.1	Updated the CLK description in <a href="#">Table 62</a> . In <a href="#">Table 64</a> , added device/package combinations for the XC3S50AN and XC3S400AN in the FT(G)256 package and the XC3S1400AN in the FG(G)484 package. In <a href="#">Table 65</a> , updated the maximum I/Os for the FG484/FGG484 packages, removed the Mass column, and updated Note 1. In <a href="#">Table 65</a> , changed the FTG256 link from <a href="#">PK115_FTG256</a> , FGG676 link from <a href="#">PK111_FGG676</a> , and the TQG144 link from <a href="#">PK126_TQG144</a> . Completely replaced the section <a href="#">FTG256: 256-Ball Fine-Pitch, Thin Ball Grid Array</a> with new information on the added device/package combinations and new figures and tables. Revised U16, U7, and T8 in <a href="#">Table 78</a> . Added <a href="#">Table 80</a> and <a href="#">Table 81</a> and updated <a href="#">Figure 23</a> .