Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 1x20b, 1x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5566axi-061

PSoC's nonvolatile subsystem consists of flash and byte-writeable EEPROM. It provides up to 256 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling boot loaders. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Two KB of byte-writable EEPROM is available on-chip to store application data.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive, flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow V_{OH} to be set independently of VDDIO when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with FS USB, the USB physical interface is also provided (USBIO). When not using USB, these pins may also be used for limited digital functionality and device programming. All the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 24 of this datasheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The Internal Main Oscillator (IMO) is the master clock base for the system, and has 5% accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 48 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate system clock frequencies up to 67 MHz from the IMO, external crystal, or external reference clock. It also contains a separate, very low-power ILO for the sleep and watchdog timers. A 32.768 kHz external watch crystal is also supported for use in RTC applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C55 family supports a wide supply operating range from 2.7 to 5.5 V. This allows operation from regulated supplies such as 3.3 V ± 10% or 5.0 V ± 10%, or directly from a wide range of battery types.

PSoC supports a wide range of low power modes. These include a 300-nA hibernate mode with RAM retention and a 2-µA sleep mode.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 6 mA when the CPU is running at 6 MHz.

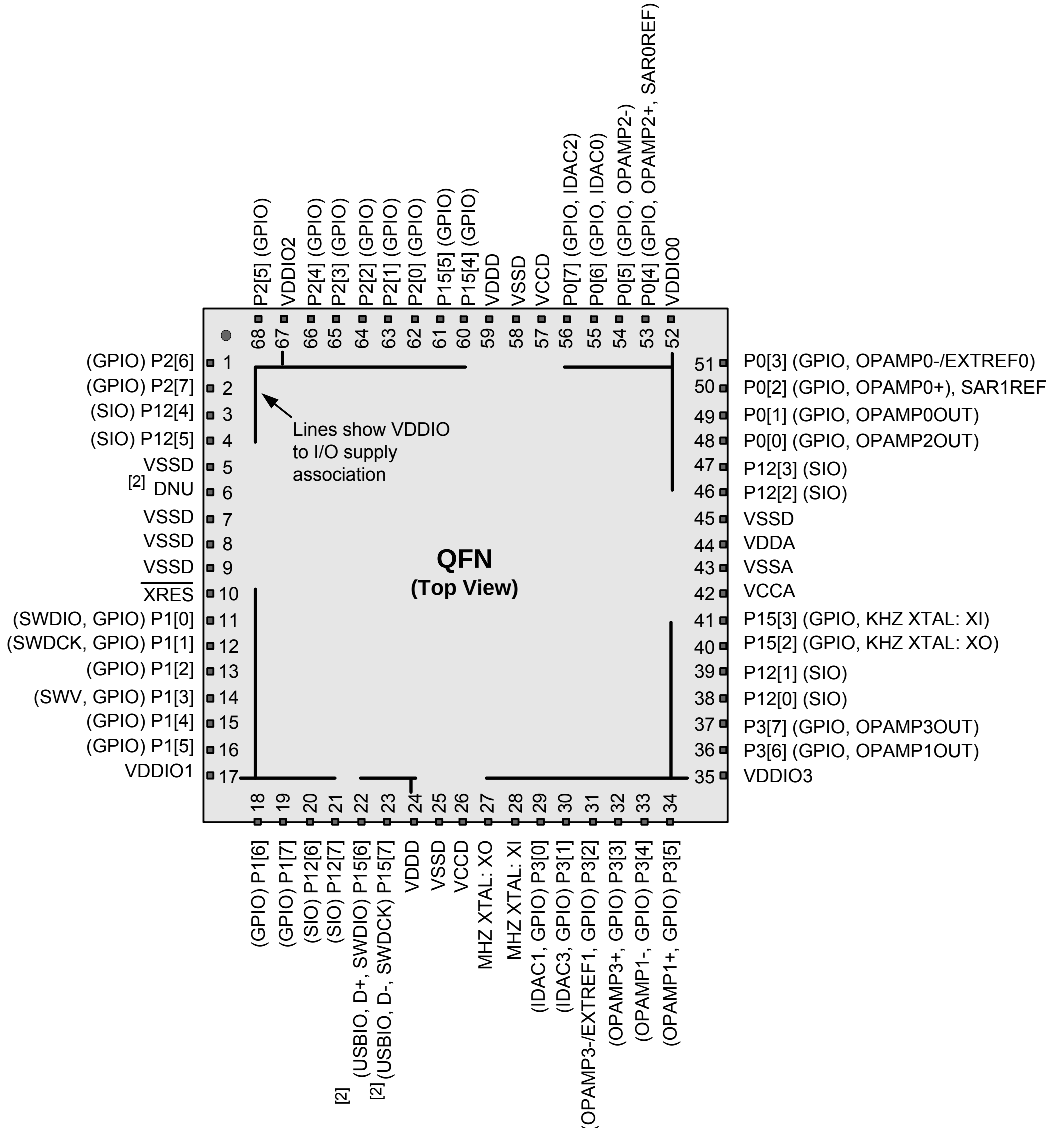
The details of the PSoC power modes are covered in the "Power System" section on page 21 of this data sheet.

PSoC uses a SWD interface for programming, debug, and test. Using this standard interface enables the designer to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. The Cortex-M3 debug and trace modules include FPB, DWT, and ITM. These modules have many features to help solve difficult debug and trace problems. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 53 of this data sheet.

2. Pinouts

The VDDIO pin that supplies a particular set of pins is indicated by the black lines drawn on the pinout diagrams in Figure 2-1 and Figure 2-2. Using the VDDIO pins, a single PSoC can support multiple interface voltage levels, eliminating the need for off-chip level shifters. Each VDDIO may sink up to 20 mA total to its associated I/O pins and opamps, and each set of VDDIO associated pins may sink up to 100 mA.

Figure 2-1. 68-pin QFN Part Pinout[3]



Notes

2. Pins labeled Do Not Use (DNU) must be left floating. USB pins on devices without USB are DNU.
3. The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

The Cortex-M3 does not support ARM instructions.

- Bit-band support for the SRAM region. Atomic bit-level write and read operations for SRAM addresses.
- Unaligned data storage and access. Contiguous storage of data of different byte lengths.
- Operation at two privilege levels (privileged and user) and in two modes (thread and handler). Some instructions can only be executed at the privileged level. There are also two stack pointers: Main (MSP) and Process (PSP). These features support a multitasking operating system running one or more user-level processes.
- Extensive interrupt and system exception support.

4.1.2 Cortex-M3 Operating Modes

The Cortex-M3 operates at either the privileged level or the user level, and in either the thread mode or the handler mode. Because the handler mode is only enabled at the privileged level, there are actually only three states, as shown in Table 4-1.

Table 4-1. Operational Level

Condition	Privileged	User
Running an exception	Handler mode	Not used
Running main program	Thread mode	Thread mode

At the user level, access to certain instructions, special registers, configuration registers, and debugging components is blocked. Attempts to access them cause a fault exception. At the privileged level, access to all instructions and registers is allowed.

The processor runs in the handler mode (always at the privileged level) when handling an exception, and in the thread mode when not.

4.1.3 CPU Registers

The Cortex-M3 CPU registers are listed in Table 4-2. Registers R0-R15 are all 32 bits wide.

Table 4-2. Cortex M3 CPU Registers

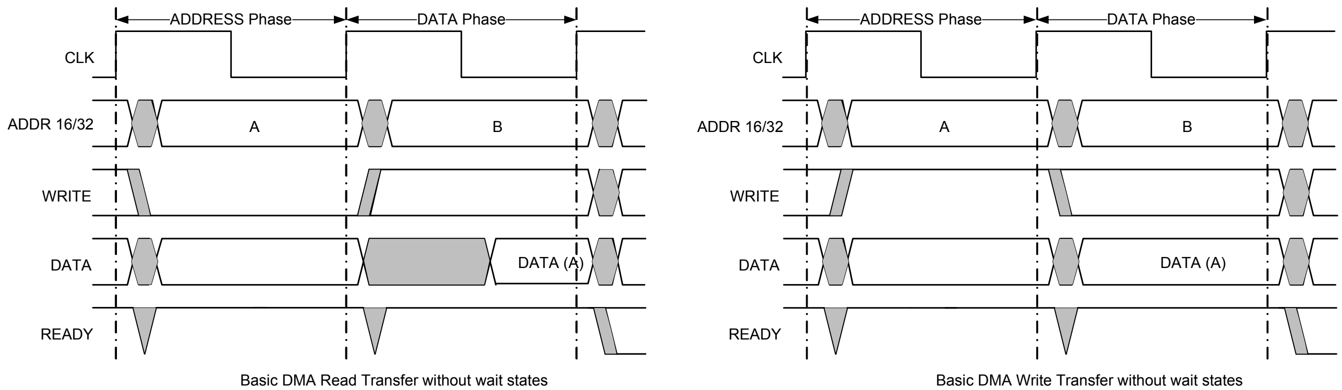
Register	Description
R0-R12	General purpose registers R0-R12 have no special architecturally defined uses. Most instructions that specify a general purpose register specify R0-R12. ■ Low registers: Registers R0-R7 are accessible by all instructions that specify a general purpose register. ■ High registers: Registers R8-R12 are accessible by all 32-bit instructions that specify a general purpose register; they are not accessible by all 16-bit instructions.

Table 4-2. Cortex M3 CPU Registers (continued)

Register	Description
R13	R13 is the stack pointer register. It is a banked register that switches between two 32-bit stack pointers: the main stack pointer (MSP) and the process stack pointer (PSP). The PSP is used only when the CPU operates at the user level in thread mode. The MSP is used in all other privilege levels and modes. Bits[0:1] of the SP are ignored and considered to be 0, so the SP is always aligned to a word (4 byte) boundary.
R14	R14 is the link register (LR). The LR stores the return address when a subroutine is called.
R15	R15 is the program counter (PC). Bit 0 of the PC is ignored and considered to be 0, so instructions are always aligned to a half word (2 byte) boundary.
xPSR	The program status registers are divided into three status registers, which are accessed either together or separately: ■ Application program status register (APSR) holds program execution status bits such as zero, carry, negative, in bits[27:31]. ■ Interrupt program status register (IPSR) holds the current exception number in bits[0:8]. ■ Execution program status register (EPSR) holds control bits for interrupt continuable and IF-THEN instructions in bits[10:15] and [25:26]. Bit 24 is always set to 1 to indicate Thumb mode. Trying to clear it causes a fault exception.
PRIMASK	A 1-bit interrupt mask register. When set, it allows only the nonmaskable interrupt (NMI) and hard fault exception. All other exceptions and interrupts are masked.
FAULTMASK	A 1-bit interrupt mask register. When set, it allows only the NMI. All other exceptions and interrupts are masked.
BASEPRI	A register of up to nine bits that define the masking priority level. When set, it disables all interrupts of the same or higher priority value. If set to 0 then the masking function is disabled.
CONTROL	A 2-bit register for controlling the operating mode. Bit 0: 0 = privileged level in thread mode, 1 = user level in thread mode. Bit 1: 0 = default stack (MSP) is used, 1 = alternate stack is used. If in thread mode or user level then the alternate stack is the PSP. There is no alternate stack for handler mode; the bit must be 0 while in handler mode.

to the Technical Reference Manual.

Figure 4-2. DMA Timing Diagram



4.3.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.3.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.3.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.3.4.5 Indexed DMA

In an indexed DMA case, an external master requires access to locations on the system bus as if those locations were shared memory. As an example, a peripheral may be configured as an SPI or I^2C slave where an address is received by the external master. That address becomes an index or offset into the internal system bus memory space. This is accomplished with an initial “address fetch” TD that reads the target address location from the peripheral and writes that value into a subsequent TD in the chain. This modifies the TD chain on the fly. When the “address fetch” TD completes it moves on to the next TD, which has the new address information embedded in it. This TD then carries out the data transfer with the address location required by the external master.

4.3.4.6 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.3.4.7 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.3.4.8 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

5. Memory

5.1 Static RAM

CY8C55 static RAM (SRAM) is used for temporary data storage. Code can be executed at full speed from the portion of SRAM that is located in the code space. This process is slower from SRAM above 0x20000000. The device provides up to 64 KB of SRAM. The CPU or the DMA controller can access all of SRAM. The SRAM can be accessed simultaneously by the Cortex-M3 CPU and the DMA controller if accessing different 32-KB blocks.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data and bulk data storage. The main flash memory area contains up to 256 KB of user program space.

Up to an additional 32 KB of flash space is available for storing device configuration data and bulk user data. User code may not be run out of this flash memory section. The flash output is 9 bytes wide with 8 bytes of data and 1 additional byte.

The flash programming interface performs flash erasing, programming and setting code protection levels. Flash In System Serial Programming (ISSP), typically used for production programming, is possible through the SWD interface. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I^2C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of configuration or general-purpose data.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the “Device Security” section on page 55). For more information on how to take full advantage of the security features in PSoC, see the PSoC 5 TRM.

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	–
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte addressable nonvolatile memory. The CY8C55 has 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into two sections, each containing 64 rows of 16 bytes each.

The CPU cannot execute out of EEPROM.

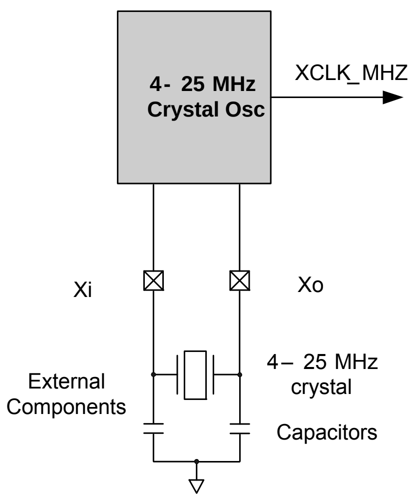
The fast timewheel is a 100 kHz, 5-bit counter clocked by the ILO that can also be used to generate periodic interrupts. The fast timewheel settings are programmable, and the counter automatically resets when the terminal count is reached. This enables flexible, periodic interrupts to the CPU at a higher rate than is allowed using the central timewheel. The fast timewheel can generate an optional interrupt each time the terminal count is reached. The 33 kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768 kHz ECO clock with no need for a crystal. The fast timewheel cannot be used as a wakeup source and must be turned off before entering sleep or hibernate mode.

6.1.2 External Oscillators

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports crystals in the range of 4 to 25 MHz. When used in conjunction with the PLL, it can generate CPU and system clocks up to the device's maximum frequency (see Phase-Locked Loop on page 19). The MHzECO with a 24 MHz crystal can be used with the clock doubler to generate a 48 MHz clock for the USB. If a crystal is not used then Xi must be shorted to ground and Xo must be left floating. MHzECO accuracy depends on the crystal chosen.

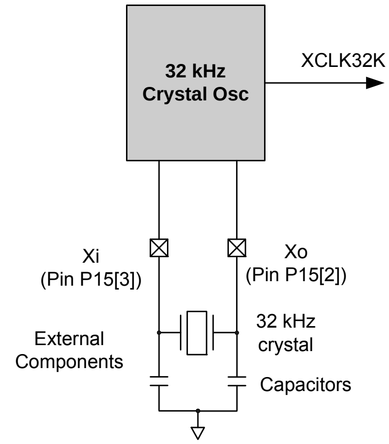
Figure 6-2. MHzECO Block Diagram



6.1.2.2 32.768 kHz ECO

The 32.768 kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768 kHz watch crystal (see Figure 6-3). The RTC uses a 1 second interrupt to implement the RTC functionality in firmware. The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the "GPIO" section on page 61.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs. While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system's bus clock used for data transfers and the CPU. The CPU clock is directly derived from the bus clock.

- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADCs and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50% duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

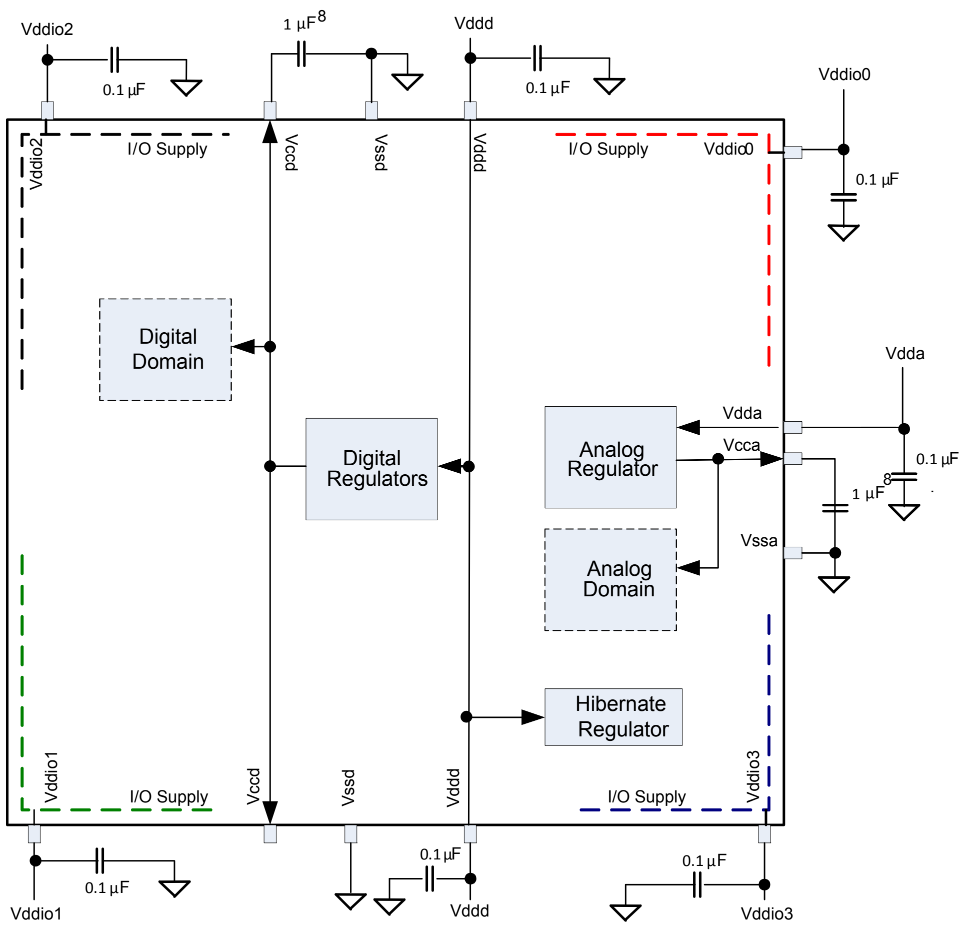
6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from the MHzECO or DSI signal.

6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and $VDDIO_X$, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in Figure 6-4 (10 µF is required for sleep mode. See Table 11-3). The two VCCD pins must be shorted together, with as short a trace as possible. The power system also contains a hibernate regulator.

Figure 6-4. PSoC Power System

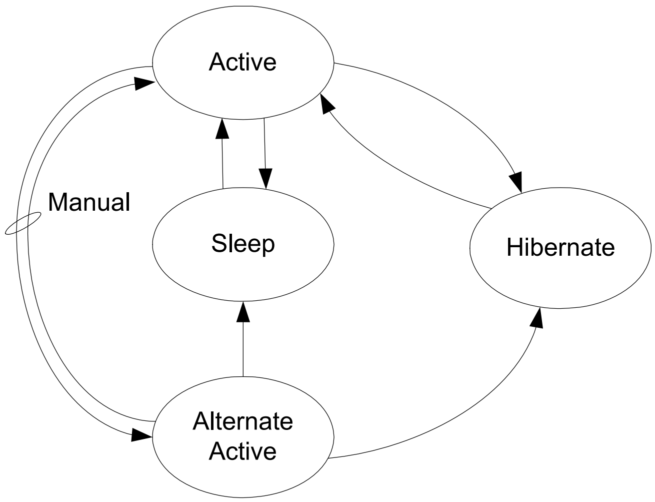


Note The two V_{CCD} pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-4.

Note

8. 10 µF is required for sleep mode. See Table 11-3.

Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode powers down the CPU and other internal circuitry to reduce power consumption. However, supervisory services such as the central timewheel (CTW) remain available in this mode. The device can wake up using CTW or system reset. The wake up time from sleep mode is 125 µs (typical).

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external reset (XRES).

6.2.1.5 Wakeup Events

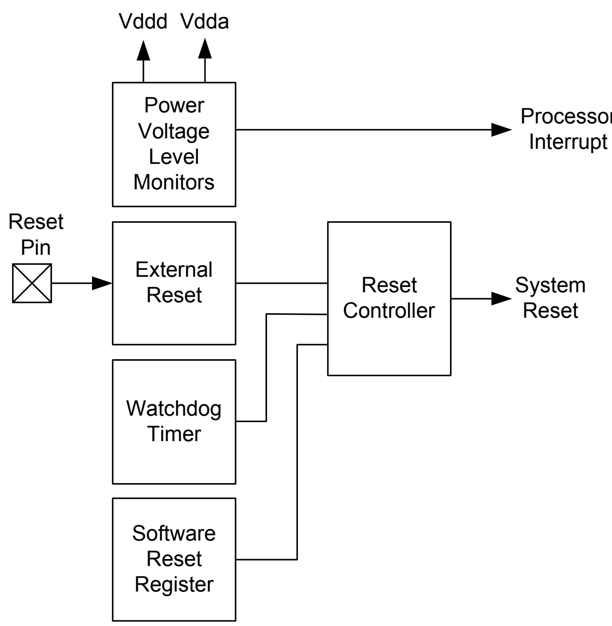
Wakeup events can come from the central timewheel or device reset. A wakeup event restores the system to active mode. The central timewheel allows the system to periodically wake up, poll peripherals, do voltage monitoring, or perform real-time functions. Reset event sources include the external reset pin (XRES).

6.3 Reset

CY8C55 has multiple internal and external reset sources available. The reset sources are:

- Power source monitoring - The analog and digital power voltages, VDDA, VDDD, VCCA, and VCCD are monitored in several different modes during power up and active mode. The monitors are programmable to generate an interrupt to the processor under certain conditions.
- External - The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to VDDIO1. VDDD, VDDA, and VDDIO1 must all have voltage applied before the part comes out of reset.
- Watchdog timer - A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset. The watchdog timer can be used only when the part remains in active mode.
- Software - The device can be reset under program control.

Figure 6-6. Resets



6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-5. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-10 depicts a simplified pin view based on each of the eight drive modes. Table 6-5 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-10. Drive Mode

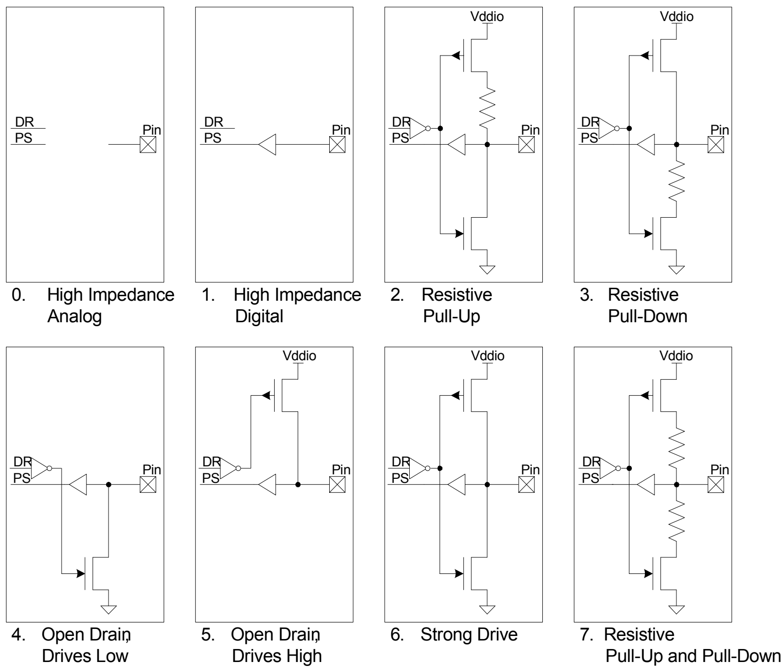


Table 6-5. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedence analog	0	0	0	High-Z	High-Z
1	High Impedance digital	0	0	1	High-Z	High-Z
2	Resistive pull-up[12]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down[12]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High-Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High-Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down[12]	1	1	1	Res High (5K)	Res Low (5K)

- High Impedance Analog

  The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

  To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

- High Impedance Digital

  The input buffer is enabled for digital signal input. This is the standard high impedance (HiZ) state recommended for digital inputs.

Note

12. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

■ Resistive Pull-up or Resistive Pull-down

Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

■ Open Drain, Drives High and Open Drain, Drives Low

Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I²C bus signal lines.

■ Strong Drive

Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

■ Resistive Pull-up and Pull-down

Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably. All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

6.4.3 Bidirectional Mode

High speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRTxDM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer. The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRTxSLW registers.

6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to "1" and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

While level sensitive interrupts are not directly supported; Universal Digital Blocks (UDB) provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip's analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin. The SIO port pins support an additional regulated high output capability, as described in Adjustable Output Level.

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, select pins provide direct connections to specific analog features such as the high current DACs or uncommitted opamps.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders[13]. See the "CapSense" section on page 51 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the "LCD Direct Drive" section on page 50 for details.

Note

13. GPIOs with opamp outputs are not recommended for use with CapSense.

should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

8.2.2.4 Multi Sample (Turbo)

The multi sample (turbo) mode operates identical to the Multi-sample mode for resolutions of 8 to 16 bits. For resolutions of 17 to 20 bits, the performance is about four times faster than the multi sample mode, because the ADC is only reset once at the end of conversion.

More information on output formats is provided in the Technical Reference Manual.

8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

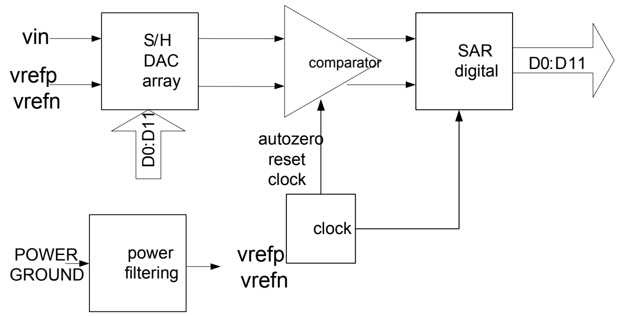
8.3 Successive Approximation ADC

The CY8C55 family of devices has two Successive Approximation (SAR) ADCs. These ADCs are 12-bit at up to 700 ksps, with single-ended or differential inputs, making them useful for a wide variety of sampling and control applications.

8.3.1 Functional Description

In a SAR ADC an analog input signal is sampled and compared with the output of a DAC. A binary search algorithm is applied to the DAC and used to determine the output bits in succession from MSB to LSB. A block diagram of one SAR ADC is shown in Figure 8-5.

Figure 8-5. SAR ADC Block Diagram



The input is connected to the analog globals and muxes. The maximum clock rate is 14 MHz.

8.3.2 Conversion Signals

Writing a start bit or assertion of a start of frame (SOF) signal is used to start a conversion. SOF can be used in applications where the sampling period is longer than the conversion time, or when the ADC needs to be synchronized to other hardware. This signal is optional and does not need to be connected if the SAR ADC is running in a continuous mode. A digital clock or UDB output can be used to drive this input. When the SAR is first powered up or awakened from any of the sleeping modes, there is a power up wait time of 10 µs before it is ready to start the first conversion.

When the conversion is complete, a status bit is set and the output signal end of frame (EOF) asserts and remains asserted until the value is read by either the DMA controller or the CPU. The EOF signal may be used to trigger an interrupt or a DMA request.

8.3.3 Operational Modes

A ONE_SHOT control bit is used to set the SAR ADC conversion mode to either continuous or one conversion per SOF signal. DMA transfer of continuous samples, without CPU intervention, is supported.

8.4 Comparators

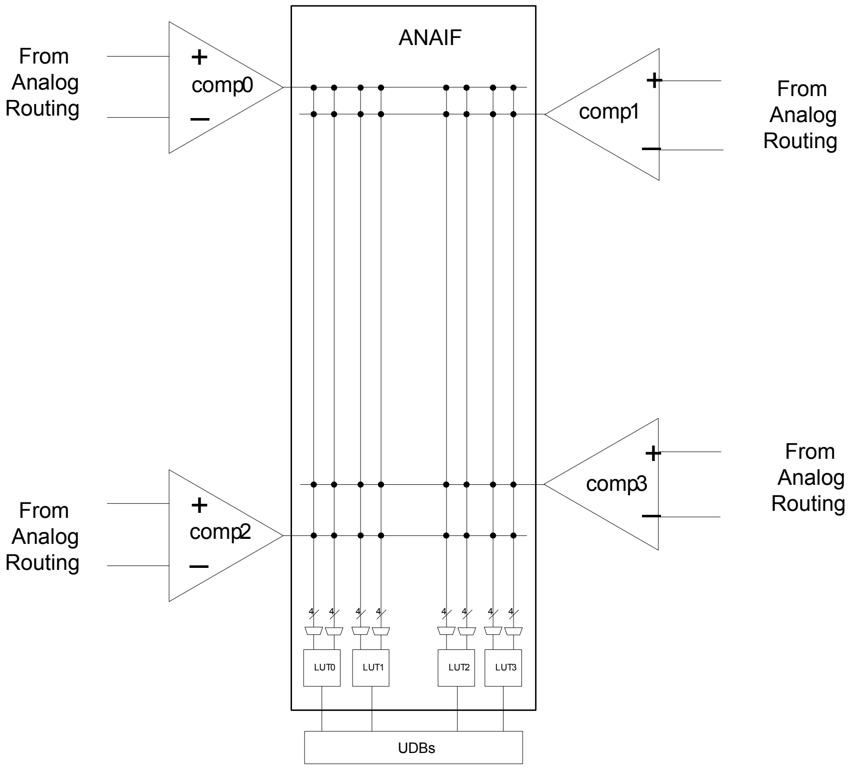
The CY8C55 family of devices contains four comparators. Comparators have these features:

- Input offset factory trimmed to less than 15 mV
- Rail-to-rail common mode input range (VSSA to VCCA)
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low power
- Comparator outputs can be routed to look up tables to perform simple logic functions and can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO, DAC outputs and SC block outputs

8.4.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB DSI.

Figure 8-6. Analog Comparator



8.4.2 LUT

The CY8C55 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

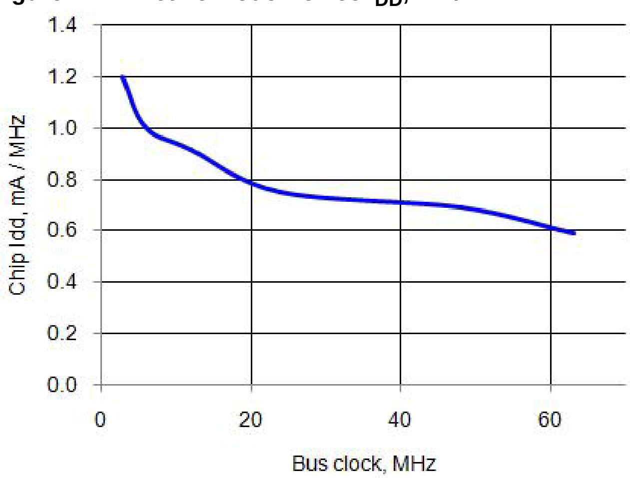
Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	**FALSE** ('0')
0001b	**A** AND **B**
0010b	**A** AND (NOT **B**)
0011b	A
0100b	(NOT **A**) AND **B**
0101b	B
0110b	**A** XOR **B**
0111b	**A** OR **B**
1000b	**A** NOR **B**
1001b	**A** XNOR **B**
1010b	NOT **B**
1011b	**A** OR (NOT **B**)
1100b	NOT **A**
1101b	(NOT **A**) OR **B**
1110b	**A** NAND **B**
1111b	**TRUE** ('1')

Table 11-2. DC Specifications (continued)

Parameter	Description	Conditions			Min	Typ	Max	Units
		Device Configuration	**$V_{DD} = V_{DDIO}$**	**Temp**				
	Sleep Mode[21]	CPU = OFF SleepTimer=ON POR = ON	4.5 V to 5.5 V	–40 °C	–	1.4	–	µA
				25 °C	–	2.2	–	
				85 °C	–	11	–	
			2.7 V to 3.6 V	–40 °C	–	1.2	–	
				25 °C	–	2	–	
				85 °C	–	10	–	
	Hibernate Mode	All oscillators and regulators off, except hibernate regulator. SRAM retention	4.5 V to 5.5 V	–40 °C	–	0.3	–	µA
				25 °C	–	0.6	–	
				85 °C	–	10	–	
			2.7 V to 3.6 V	–40 °C	–	0.2	–	
				25 °C	–	0.3	–	
				85 °C	–	8	–	
I_{DDAR}	Analog current consumption while device is reset[20]	$V_{DDA} \le 3.6$ V			–	0.3	–	mA
		$V_{DDA} > 3.6$ V			–	1.4	–	mA
I_{DDDR}	Digital current consumption while device is reset[20]	$V_{DDD} \le 3.6$ V			–	1.1	–	mA
		$V_{DDD} > 3.6$ V			–	0.7	–	mA

Figure 11-1. Active Mode Device I_{DD}, mA/MHz



Note

20. Based on device characterization (not production tested). USBIO pins tied to ground (VSSD).

Table 11-8. SIO DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
C_{IN}	Input capacitance[29]		–	–	7	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[29]	Single ended mode (GPIO mode)	–	150	–	mV
		Differential mode	–	35	–	mV
Idiode	Current through protection diode to V_{SSIO}		–	–	100	µA

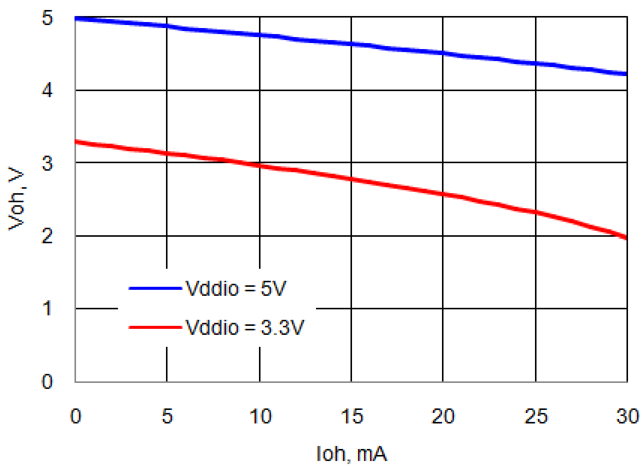


Figure 11-9. SIO Output High Voltage and Current, Unregulated Mode

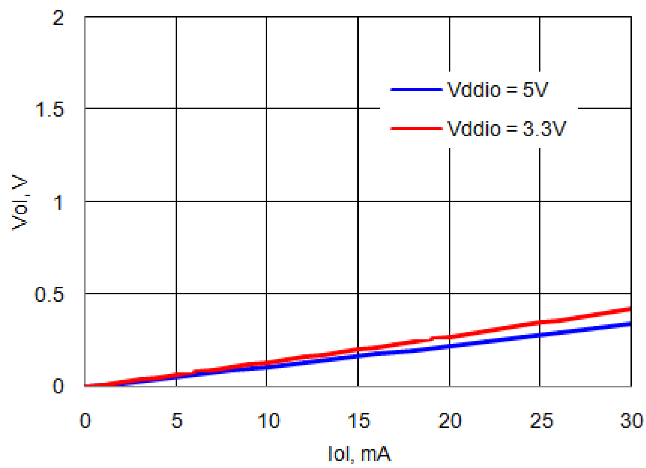


Figure 11-11. SIO Output Low Voltage and Current, Unregulated Mode

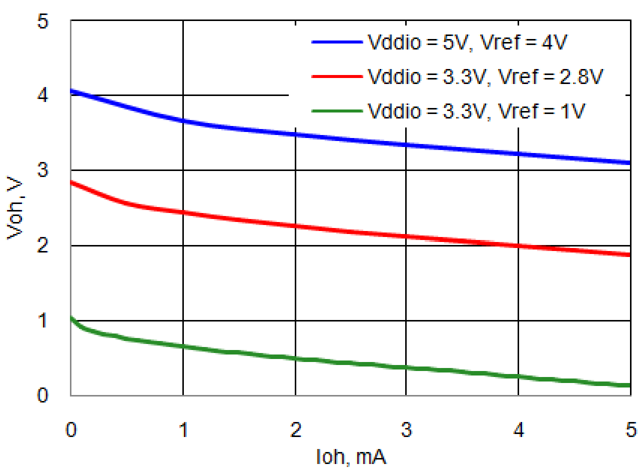


Figure 11-10. SIO Output High Voltage and Current, Regulated Mode

Table 11-9. SIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in fast strong mode (90/10%)[30]	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns
TfallF	Fall time in fast strong mode (90/10%)[30]	Cload = 25 pF, V_{DDIO} = 3.3 V	–	–	12	ns

Note
30. Based on device characterization (Not production tested).

Table 11-9. SIO AC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseS	Rise time in slow strong mode (90/10%)[30]	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	75	ns
TfallS	Fall time in slow strong mode (90/10%)[30]	Cload = 25 pF, V_{DDIO} = 3.0 V	–	–	60	ns
Fsioout	SIO output operating frequency					
	Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	2.7 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency	90/10% V_{DDIO}	–	–	66	MHz

Figure 11-12. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

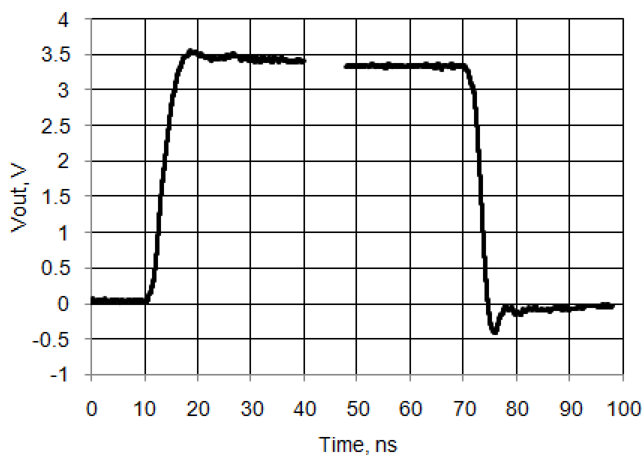


Figure 11-13. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

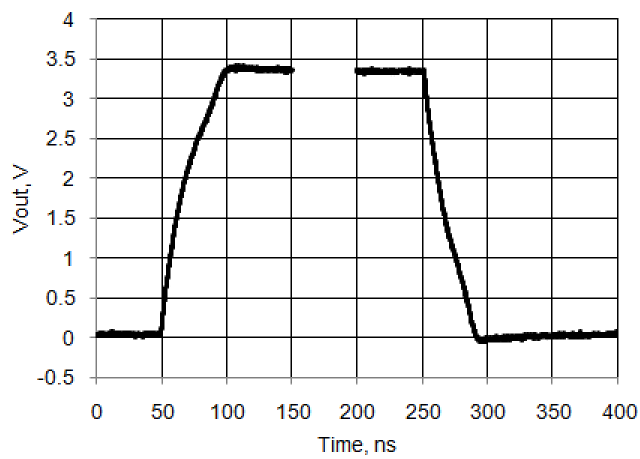


Table 11-11. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate	Using external 24 MHz crystal	12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	$3\ V \le V_{DDD} \le 5.5\ V$	–	–	20	MHz
		V_{DDD} = 2.7 V	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 2.7 V, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 2.7 V, 25 pF load	–	–	40	ns

Figure 11-16. USBIO Output Rise and Fall Times, GPIO Mode, V_{DDD} = 3.3 V, 25 pF Load

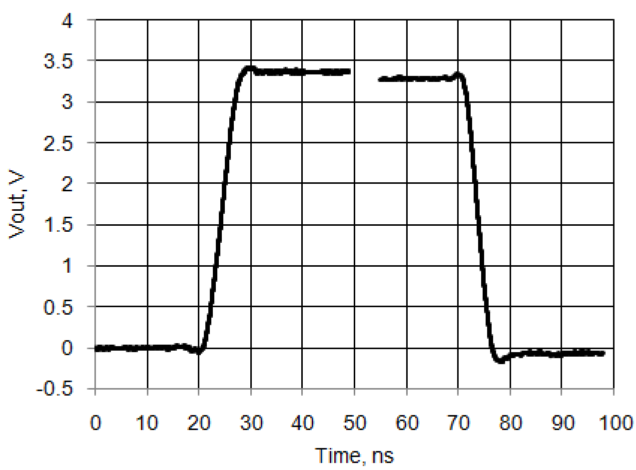


Table 11-12. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5}, $V_{USB\_3.3}$, see USB DC Specifications on page 92	80%	–	135%	
Vcrs	Output signal crossover voltage		1.1	–	2.3	V

Table 11-18. Delta-sigma ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion, 16-bit[37]	Unbuffered, Range ±1.024 V	–	–	0.006	%
20-Bit Resolution Mode						
SR20	Sample Rate, 20-bit[37]	Differential range ±1.024 V	7.8	–	187	sps
BW20	Bandwidth, 20-bit[37]	Differential range ±1.024 V	–	40	–	Hz
16-Bit Resolution Mode						
SR16	Sample Rate, 16-bit[37]	Differential range ±1.024 V	2	–	48	ksps
BW16	Bandwidth, 16-bit[37]	Differential range ±1.024 V	–	11	–	kHz
SINAD16int	Signal to noise + distortion - 16-bit, internal reference[37]	Unbuffered, Range = ±1.024 V,	81	–	–	dB
SINAD_16ext	Signal to noise + distortion - 16-bit, external reference[37]	Unbuffered, Range = ±1.024 V,	84	–	–	dB
12-Bit Resolution Mode						
SR12	Sample Rate, 12-bit[37]	Differential range ±1.024 V	4	–	192	kSps
BW12	Bandwidth, 12-bit[37]	Differential range ±1.024 V	–	44	–	kHz
SINAD12int	Signal to noise + distortion - 12-bit, internal reference[37]	Unbuffered, Range = ±1.024 V,	66	–	–	dB
8-Bit Resolution Mode						
SR8	Sample Rate, 8-bit[37]	Differential range ±1.024 V	8	–	384	kSps
BW8	Bandwidth, 8-bit[37]	Differential range ±1.024 V	–	88	–	kHz
SINAD8int	Signal to noise + distortion - 8-bit, internal reference[37]	Unbuffered, Range = ±1.024 V,	43	–	–	dB

Note
37. Based on device characterization (not production tested).

Table 11-31. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	5.5	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	180	ns
	Current noise	Range = 255 µA, source mode, fast mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-42. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V

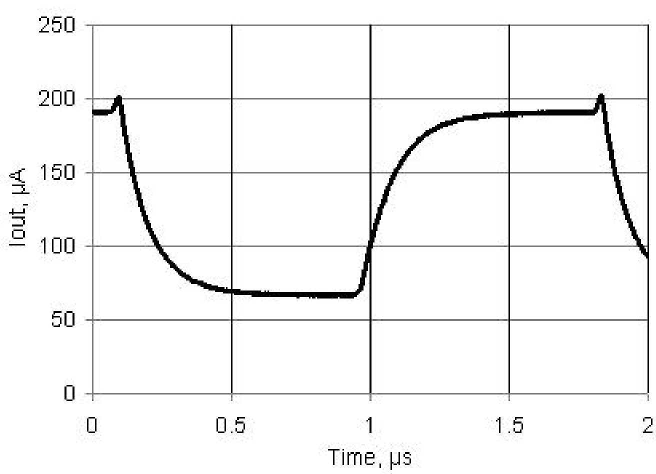


Figure 11-44. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V

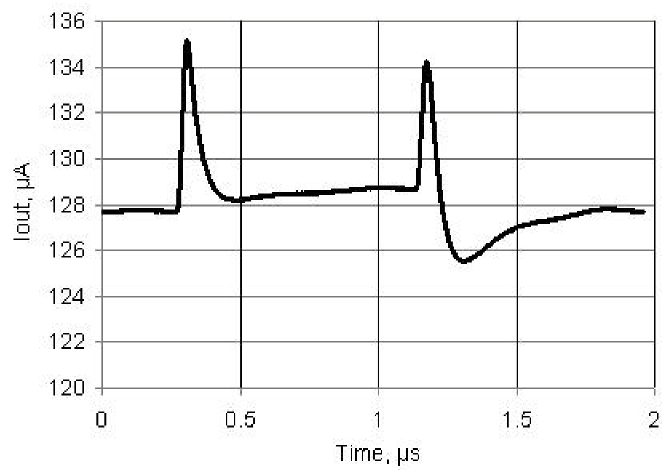


Figure 11-43. IDAC PSRR vs Frequency

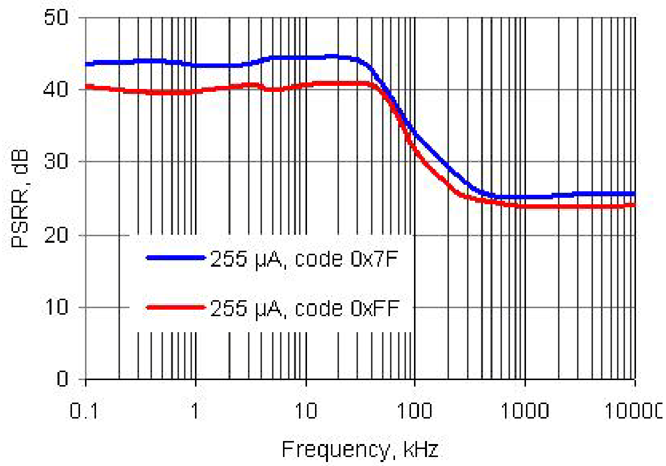
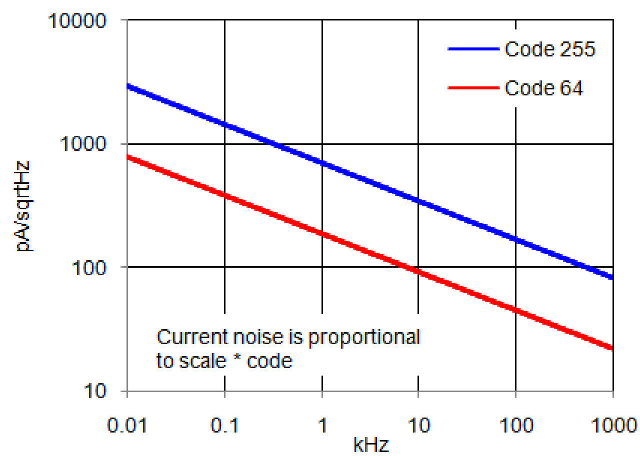


Figure 11-45. IDAC Current Noise, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V



Examples

CY8C 5 5 6 8 AX/LT I - x x x

	Cypress Prefix	CY8C
5: PSoC 5	Architecture	5
5: CY8C55 Family	Family Group within Architecture	5
6: 67 MHz	Speed Grade	6
8: 256 KB	Flash Capacity	8
AX: TQFP, LT: QFN	Package Code	AX/LT
I: Industrial	Temperature Range	I
	Peripheral Set	x x x

All devices in the PSoC 5 CY8C55 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25	85	°C
T_J	Operating junction temperature		–40	–	100	°C
Tja	Package θJA (68-pin QFN)		–	15	–	°C/Watt
Tja	Package θJA (100-pin TQFP)		–	34	–	°C/Watt
Tjc	Package θJC (68-pin QFN)		–	13	–	°C/Watt
Tjc	Package θJC (100-pin TQFP)		–	10	–	°C/Watt

Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
68-pin QFN	MSL 3
100-pin TQFP	MSL 3

Figure 13-1. 68-pin QFN 8 × 8 with 0.4 mm Pitch Package Outline (Sawn Version)