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What is "Embedded - Microcontrollers"?

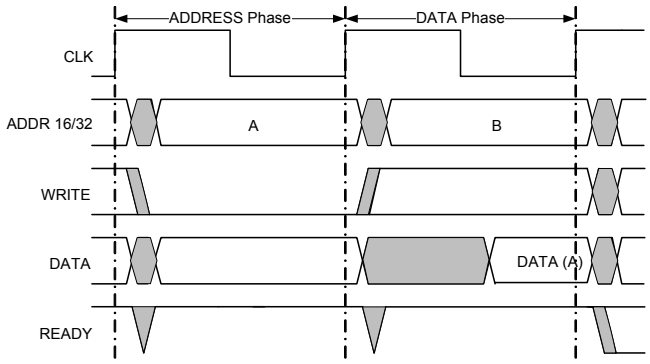
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

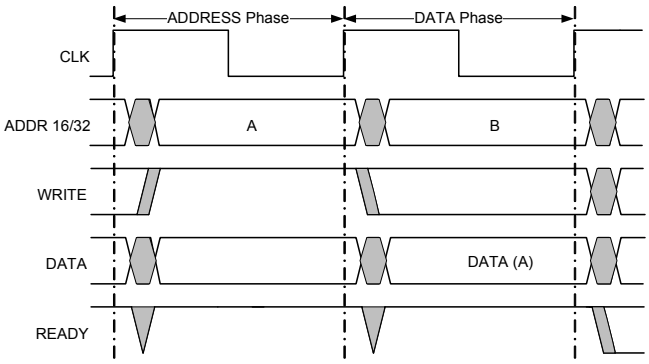
Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 1x20b, 1x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5567axi-019

to the Technical Reference Manual.

Figure 4-2. DMA Timing Diagram



Basic DMA Read Transfer without wait states



Basic DMA Write Transfer without wait states

4.3.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.3.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.3.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

4.3.4.5 Indexed DMA

In an indexed DMA case, an external master requires access to locations on the system bus as if those locations were shared memory. As an example, a peripheral may be configured as an SPI or I^2C slave where an address is received by the external master. That address becomes an index or offset into the internal system bus memory space. This is accomplished with an initial “address fetch” TD that reads the target address location from the peripheral and writes that value into a subsequent TD in the chain. This modifies the TD chain on the fly. When the “address fetch” TD completes it moves on to the next TD, which has the new address information embedded in it. This TD then carries out the data transfer with the address location required by the external master.

4.3.4.6 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.3.4.7 Packet Queuing DMA

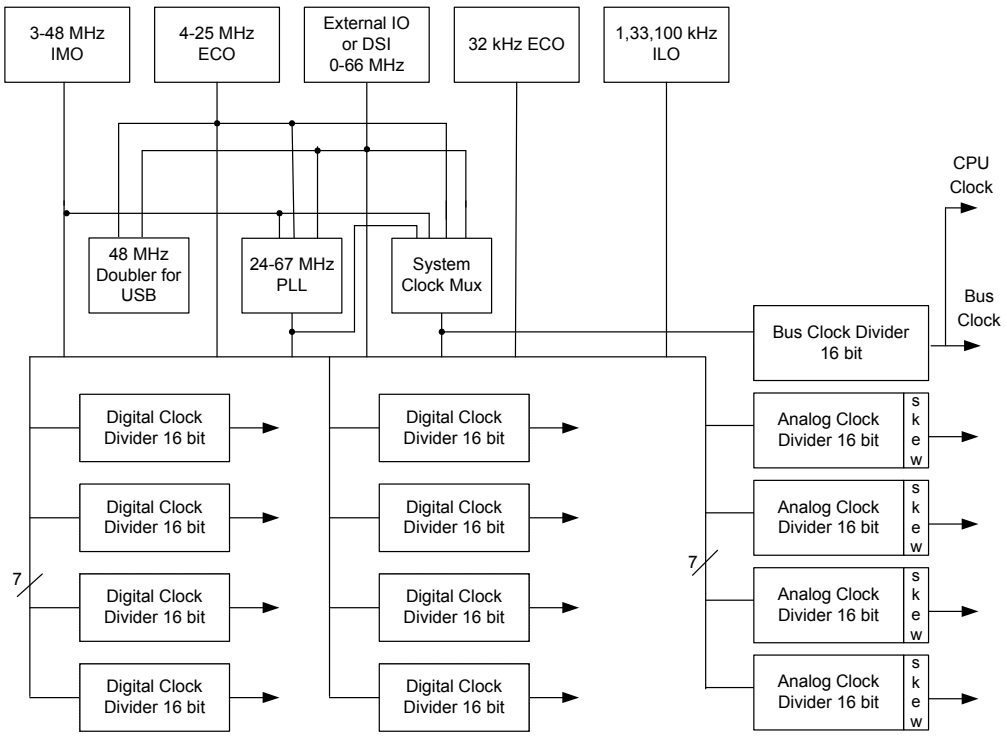
Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.3.4.8 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

Figure 6-1. Clocking Subsystem



6.1.1 Internal Oscillators

6.1.1.1 Internal Main Oscillator

The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from ±5% at 3 MHz, up to ±10% at 48 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency. The IMO provides clock outputs at 3, 6, 12, 24, and 48 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works at input frequency of 24 MHz, providing 48 MHz for the USB. It can be configured to use a clock from the MHzECO or the DSI (external pin). The doubler is typically used to clock the USB.

6.1.1.3 Phase-Locked Loop

The PLL allows low frequency, high accuracy clocks to be multiplied to higher frequencies. This is a tradeoff between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 67 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 µs (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO, or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low power modes.

6.1.1.4 Internal Low-Speed Oscillator

The ILO provides clock frequencies for low power consumption, including the sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz.

The 1 kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to long sleep intervals using the central timewheel (CTW). The central timewheel is a free running counter clocked by the ILO 1 kHz output. The central timewheel is always enabled except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low power mode. Firmware can reset the central timewheel.

The central timewheel can be programmed to wake the system periodically and optionally issue an interrupt. This enables flexible, periodic wakeups from low power modes or coarse timing applications. Systems that require accurate timing should use the RTC capability instead of the central timewheel. The 100 kHz clock (CLK100K) works as a low power system clock to run the CPU. It can also generate fast time intervals using the fast timewheel.

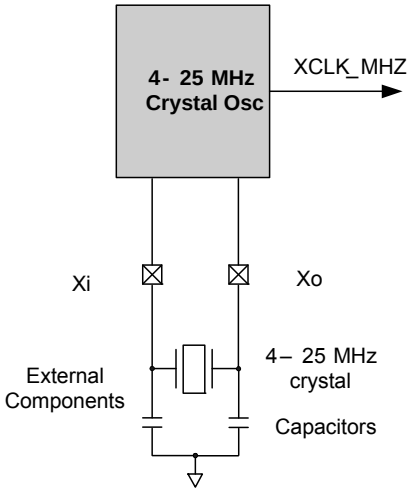
The fast timewheel is a 100 kHz, 5-bit counter clocked by the ILO that can also be used to generate periodic interrupts. The fast timewheel settings are programmable, and the counter automatically resets when the terminal count is reached. This enables flexible, periodic interrupts to the CPU at a higher rate than is allowed using the central timewheel. The fast timewheel can generate an optional interrupt each time the terminal count is reached. The 33 kHz clock (CLK33K) comes from a divide-by-3 operation on CLK100K. This output can be used as a reduced accuracy version of the 32.768 kHz ECO clock with no need for a crystal. The fast timewheel cannot be used as a wakeup source and must be turned off before entering sleep or hibernate mode.

6.1.2 External Oscillators

6.1.2.1 MHz External Crystal Oscillator

The MHzECO provides high frequency, high precision clocking using an external crystal (see Figure 6-2). It supports crystals in the range of 4 to 25 MHz. When used in conjunction with the PLL, it can generate CPU and system clocks up to the device's maximum frequency (see Phase-Locked Loop on page 19). The MHzECO with a 24 MHz crystal can be used with the clock doubler to generate a 48 MHz clock for the USB. If a crystal is not used then Xi must be shorted to ground and Xo must be left floating. MHzECO accuracy depends on the crystal chosen.

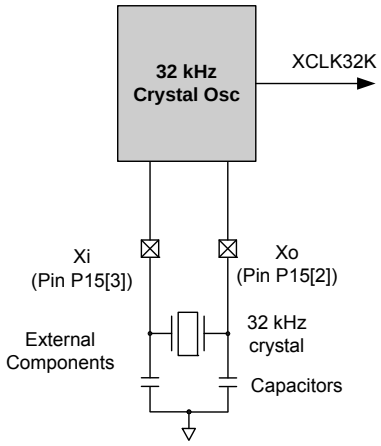
Figure 6-2. MHzECO Block Diagram



6.1.2.2 32.768 kHz ECO

The 32.768 kHz external crystal oscillator (32kHzECO) provides precision timing with minimal power consumption using an external 32.768 kHz watch crystal (see Figure 6-3). The RTC uses a 1 second interrupt to implement the RTC functionality in firmware. The oscillator works in two distinct power modes. This allows users to trade off power consumption with noise immunity from neighboring circuits. The GPIO pins connected to the external crystal and capacitors are fixed.

Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the “GPIO” section on page 61.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and UDBs. While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design’s requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The system clock is used to select and supply the fastest clock in the system for general system clock requirements and clock synchronization of the PSoC device.
- Bus clock 16-bit divider uses the system clock to generate the system’s bus clock used for data transfers and the CPU. The CPU clock is directly derived from the bus clock.

- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the UDBs and fixed function timer/counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADCs and mixers. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50% duty cycle clocks, system clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

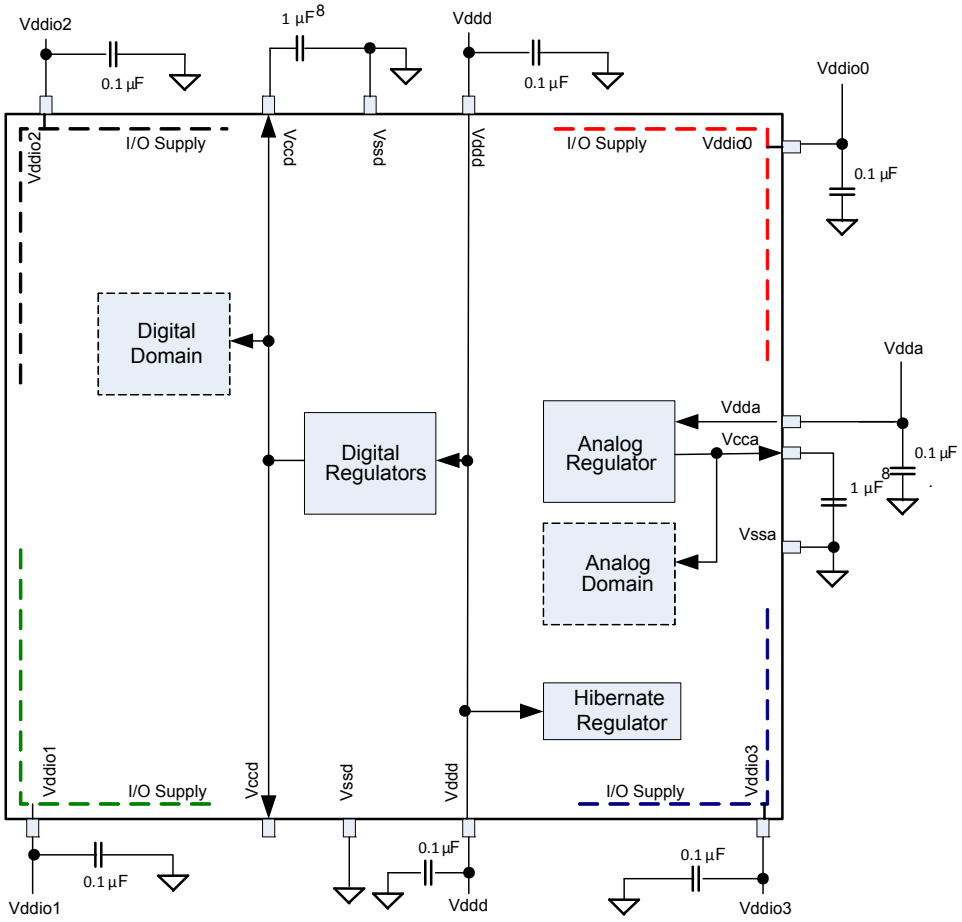
6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from the MHzECO or DSI signal.

6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and $VDDIO_X$, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in Figure 6-4 (10 µF is required for sleep mode. See Table 11-3). The two VCCD pins must be shorted together, with as short a trace as possible. The power system also contains a hibernate regulator.

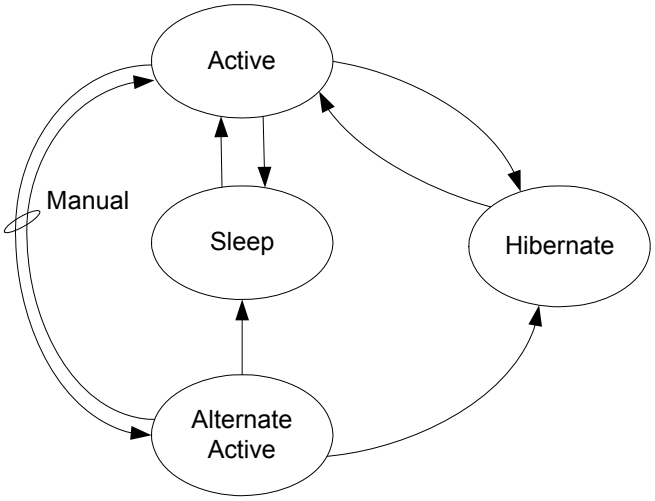
Figure 6-4. PSoC Power System



Note The two V_{CCD} pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-4.

Note
8. 10 µF is required for sleep mode. See Table 11-3.

Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode powers down the CPU and other internal circuitry to reduce power consumption. However, supervisory services such as the central timewheel (CTW) remain available in this mode. The device can wake up using CTW or system reset. The wake up time from sleep mode is 125 µs (typical).

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external reset (XRES).

6.2.1.5 Wakeup Events

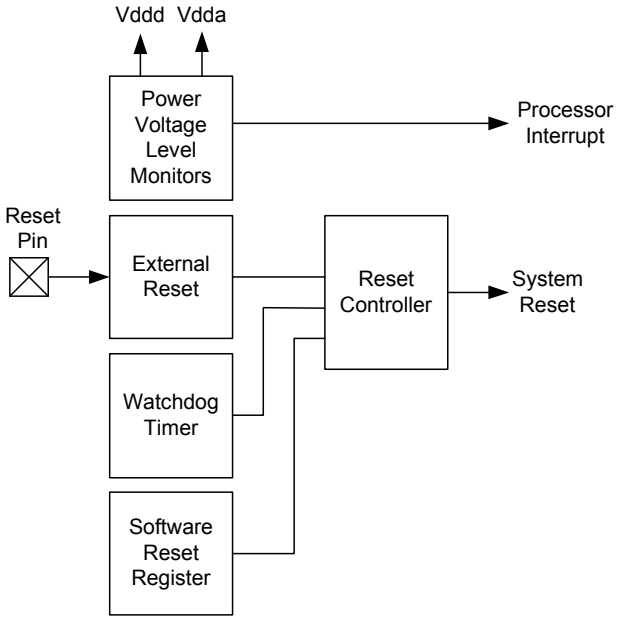
Wakeup events can come from the central timewheel or device reset. A wakeup event restores the system to active mode. The central timewheel allows the system to periodically wake up, poll peripherals, do voltage monitoring, or perform real-time functions. Reset event sources include the external reset pin (XRES).

6.3 Reset

CY8C55 has multiple internal and external reset sources available. The reset sources are:

- Power source monitoring - The analog and digital power voltages, VDDA, VDDD, VCCA, and VCCD are monitored in several different modes during power up and active mode. The monitors are programmable to generate an interrupt to the processor under certain conditions.
- External - The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to VDDIO1. VDDD, VDDA, and VDDIO1 must all have voltage applied before the part comes out of reset.
- Watchdog timer - A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset. The watchdog timer can be used only when the part remains in active mode.
- Software - The device can be reset under program control.

Figure 6-6. Resets



The term **system reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Power Voltage Level Monitors

- IPOR - Initial Power on Reset

  At initial power on, IPOR monitors the power voltages VDDD and VDDA, both directly at the pins and at the outputs of the corresponding internal regulators. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 100 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

  To save power the IPOR circuit is disabled when the internal digital supply is stable. When the voltage is high enough, the IMO starts.

- ALVI, DLVI, AHVI - Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

  Interrupt circuits are available to detect when VDDA and VDDD go outside a voltage range. For AHVI, VDDA is compared to a fixed trip level. For ALVI and DLVI, VDDA and VDDD are compared to trip levels that are programmable, as listed in Table 6-4.

Table 6-4. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	VDDD	2.7 V-5.5 V	2.45 V-5.45 V in 250 mV increments. The 2.45 V setting is used for LVD.
ALVI	VDDA	2.7 V-5.5 V	2.45 V-5.45 V in 250 mV increments. The 2.45 V setting is used for LVD.
AHVI	VDDA	2.7 V-5.5 V	5.75 V

The monitors are disabled until after IPOR. The monitors are not available in low-power modes. To monitor voltages in sleep mode, wake up periodically using the CTW. After wakeup, the 2.45 V LVI interrupt may trigger. Voltage monitoring is not available in hibernate mode.

6.3.2 Other Reset Sources

- XRES - External Reset

  CY8C55 has a dedicated XRES pin which holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset. The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

- SRES - Software Reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- WRES - Watchdog Timer Reset

  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power on reset event. The watchdog timer can be used only when the part remains in active mode.

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both general purpose I/O (GPIO) and special I/O (SIO) provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense[11], and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

Note
11. GPIOs with opamp outputs are not recommended for use with CapSense.

Figure 6-7. GPIO Block Diagram

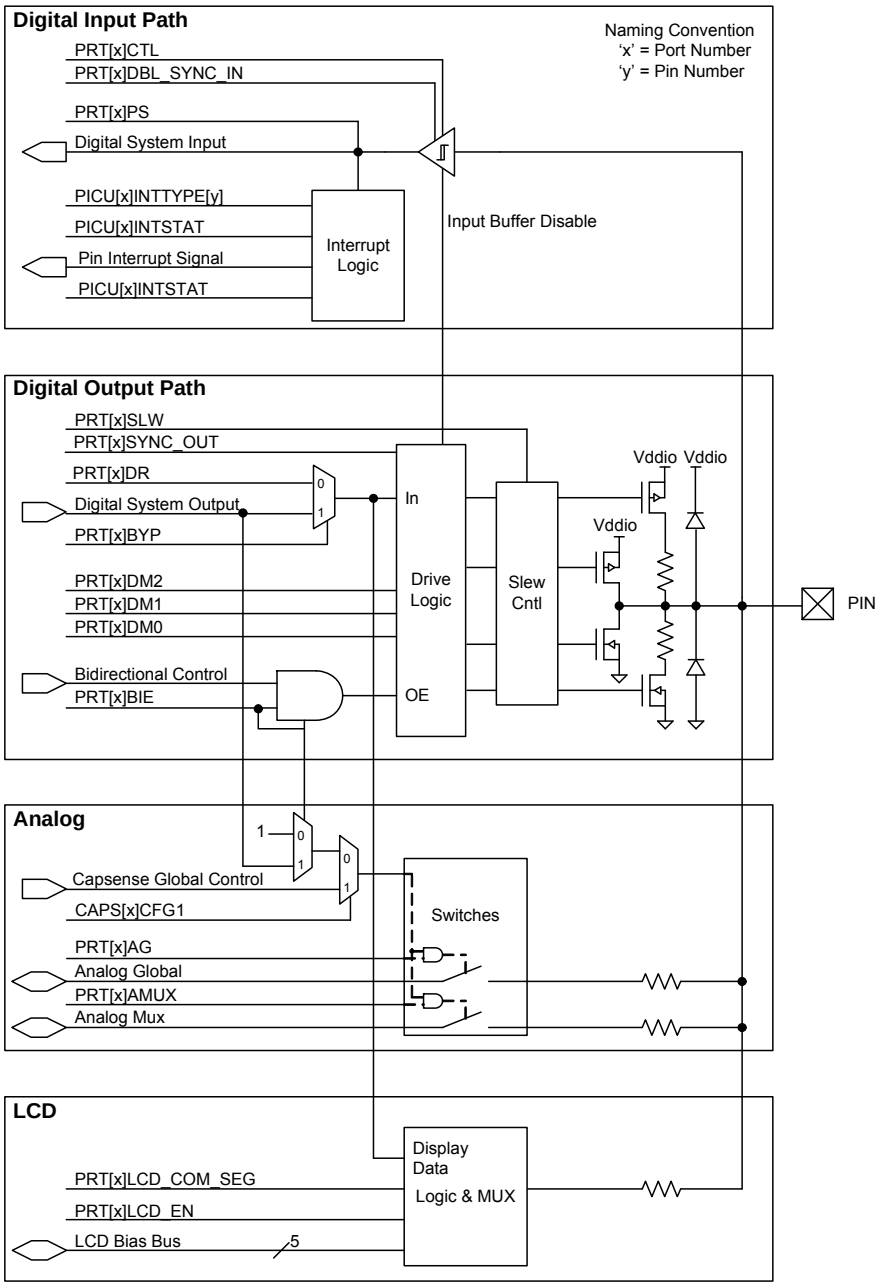
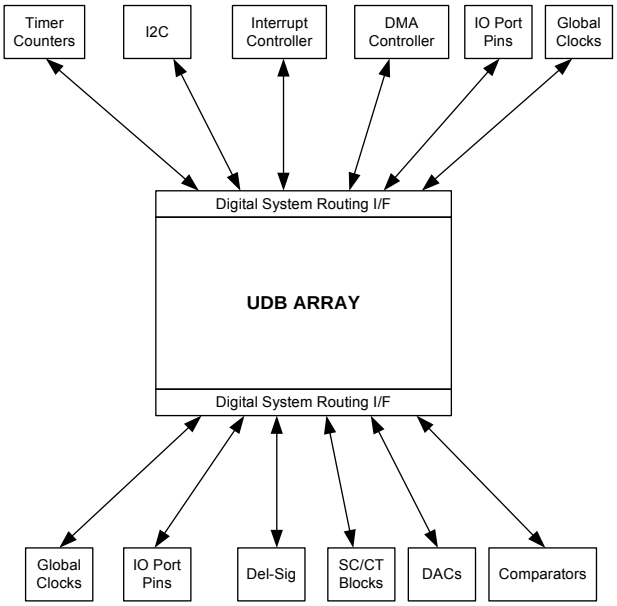
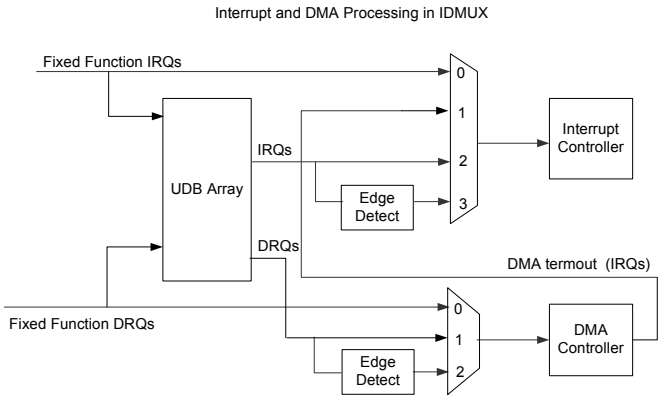


Figure 7-6. Digital System Interconnect



Interrupt and DMA routing is very flexible in the CY8C55 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-7 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-7. Interrupt and DMA Processing in the IDMUX



7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the system clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-8. I/O Pin Synchronization Routing

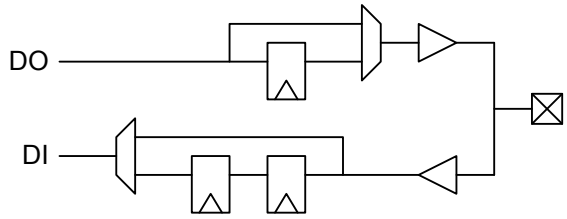
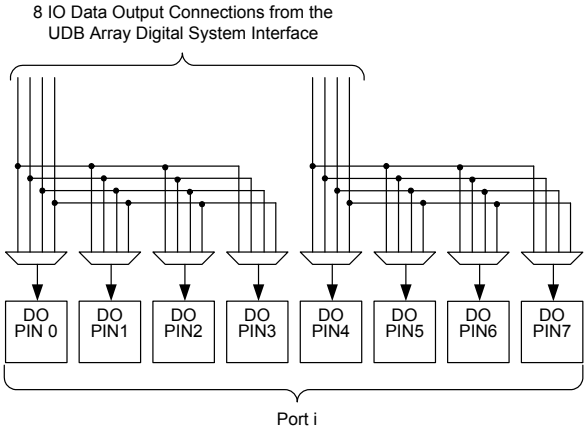
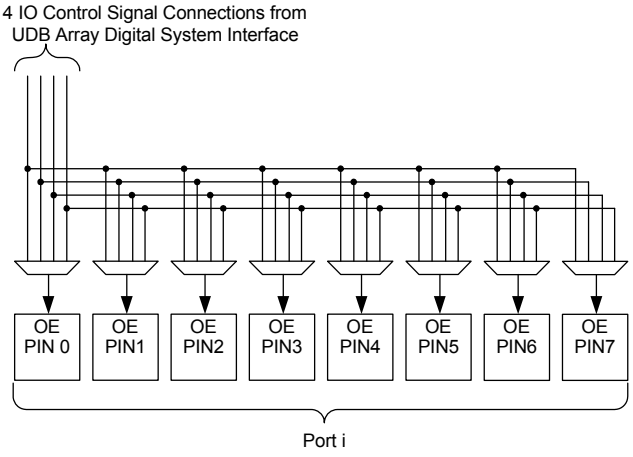


Figure 7-9. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Figure 7-10. I/O Pin Output Enable Connectivity

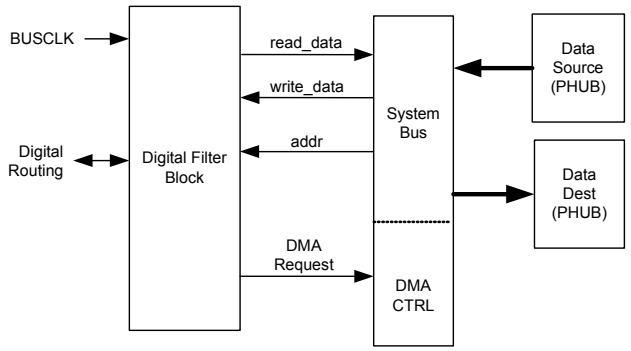


7.8 Digital Filter Block

Some devices in the CY8C55 family of devices have a dedicated HW accelerator block used for digital filtering. The DFB has a dedicated multiplier and accumulator that calculates a 24-bit by 24-bit multiply accumulate in one system clock cycle. This enables the mapping of a direct form FIR filter that approaches a computation rate of one FIR tap for each clock cycle. The MCU can implement any of the functions performed by this block, but at a slower rate that consumes significant MCU bandwidth.

The PSoC Creator interface provides a wizard to implement FIR and IIR digital filters with coefficients for LPF, BPF, HPF, Notch and arbitrary shape filters. 64 pairs of data and coefficients are stored. This enables a 64 tap FIR filter or up to 4 16 tap filters of either FIR or IIR formulation.

Figure 7-14. DFB Application Diagram (pwr/gnd not shown)



The typical use model is for data to be supplied to the DFB over the system bus from another on-chip system data source such as an ADC. The data typically passes through main memory or is directly transferred from another chip resource through DMA. The DFB processes this data and passes the result to another on chip resource such as a DAC or main memory through DMA on the system bus.

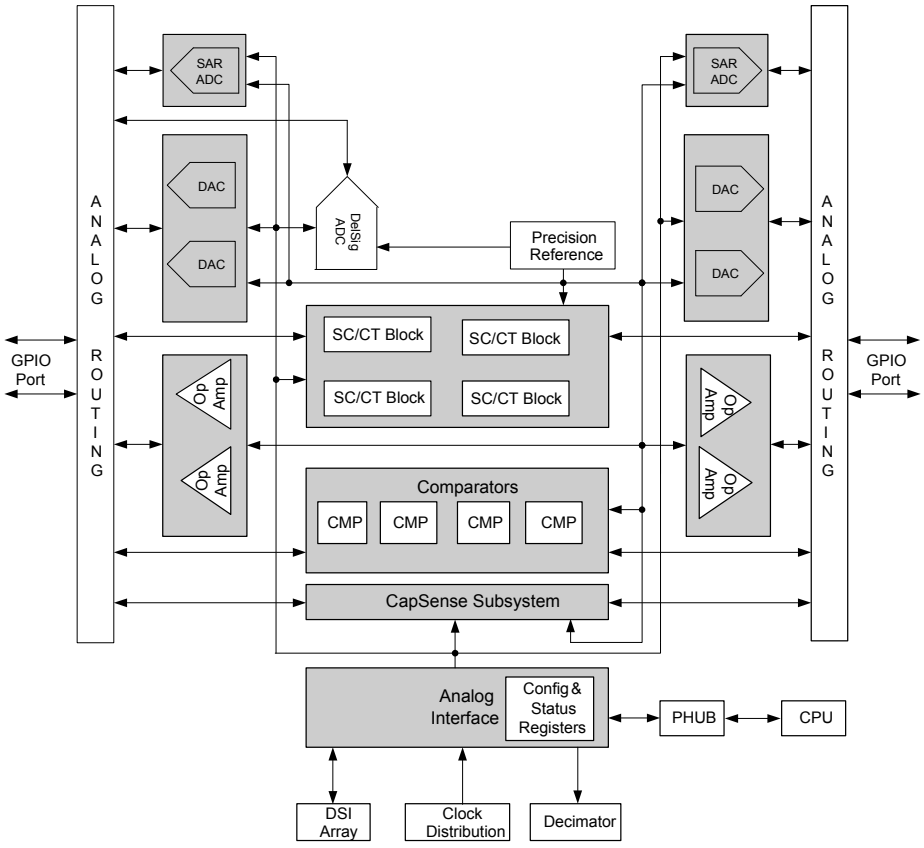
Data movement in or out of the DFB is typically controlled by the system DMA controller but can be moved directly by the MCU.

8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

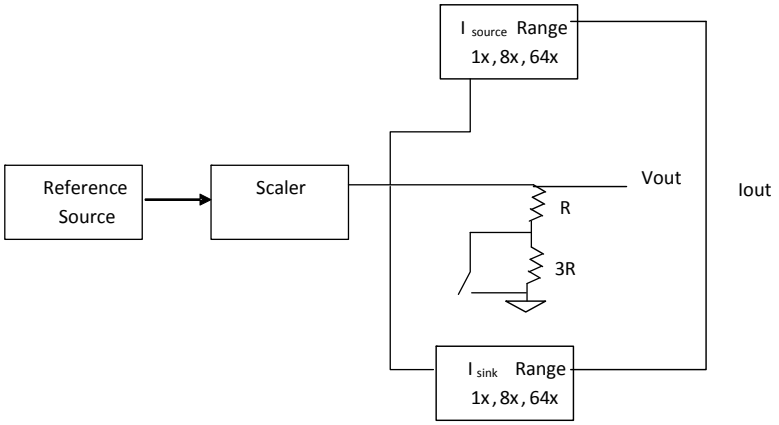
- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses
- High resolution Delta-Sigma ADC
- Two successive approximation (SAR) ADCs
- Four 8-bit DACs that provide either voltage or current output
- Four comparators with optional connection to configurable LUT outputs
- Four configurable switched capacitor/continuos time (SC/CT) blocks for functions that include opamp, unity gain buffer, programmable gain amplifier, transimpedance amplifier, and mixer
- Four opamps for internal use and connection to GPIO that can be used as high current output buffers
- CapSense subsystem to enable capacitive touch sensing
- Precision reference for generating an accurate analog voltage for internal analog blocks

Figure 8-1. Analog Subsystem Block Diagram



The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and also connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

Figure 8-12. DAC Block Diagram



8.10.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.10.2 Voltage DAC

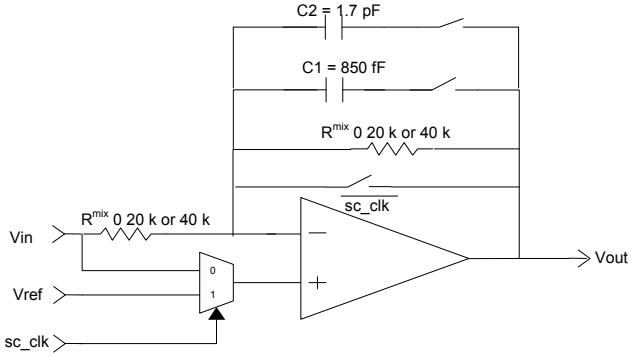
For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

8.11 Up/Down Mixer

In continuous time mode, the SC/CT block components are used to build an up or down mixer. Any mixing application contains an input signal frequency and a local oscillator frequency. The polarity of the clock, Fclk, switches the amplifier between inverting or noninverting gain. The output is the product of the input and the switching function from the local oscillator, with frequency components at the local oscillator plus and minus the signal frequency (Fclk + Fin and Fclk - Fin) and reduced-level frequency components at odd integer multiples of the local oscillator frequency. The local oscillator frequency is provided by the selected clock source for the mixer.

Continuous time up and down mixing works for applications with input signals and local oscillator frequencies up to 1 MHz.

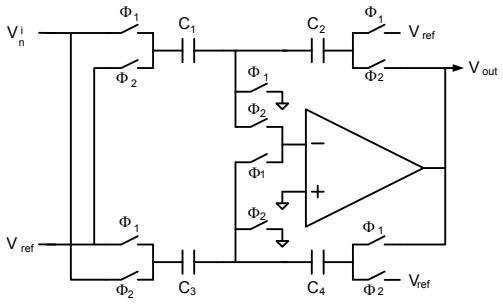
Figure 8-13. Mixer Configuration



8.12 Sample and Hold

The main application for a sample and hold, is to hold a value stable while an ADC is performing a conversion. Some applications require multiple signals to be sampled simultaneously, such as for power calculations (V and I).

Figure 8-14. Sample and Hold Topology (Φ1 and Φ2 are opposite phases of a clock)



8.12.1 Down Mixer

The S+H can be used as a mixer to down convert an input signal. This circuit is a high bandwidth passive sample network that can sample input signals up to 14 MHz. This sampled value is then held using the opamp with a maximum clock rate of 4 MHz. The output frequency is at the difference between the input frequency and the highest integer multiple of the Local Oscillator that is less than the input.

8.12.2 First Order Modulator - SC Mode

A first order modulator is constructed by placing the switched capacitor block in an integrator mode and using a comparator to provide a 1-bit feedback to the input. Depending on this bit, a reference voltage is either subtracted or added to the input signal. The block output is the output of the comparator and not the integrator in the modulator case. The signal is downshifted and buffered and then processed by a decimator to make a delta-sigma converter or a counter to make an incremental converter. The accuracy of the sampled data from the first-order modulator is determined from several factors. The main application for this modulator is for a low frequency ADC with high accuracy. Applications include strain gauges, thermocouples, precision voltage, and current measurement.

9.3 Debug Features

The CY8C55 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Six program address breakpoints and two literal access breakpoints
- Data watchpoint events to CPU
- Patch and remap instruction from flash to SRAM
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger

9.4 Trace Features

The following trace features are supported:

- Data watchpoint on access to data address, address range, or data value
- Software event monitoring, “printf-style” debugging

9.5 SWV Interface

The SWV interface provides trace data to a debug host via the Cypress MiniProg3 or an external trace port analyzer.

9.6 Programming Features

The SWD interface provides full programming support. The entire device can be erased, programmed, and verified. Designers can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 5 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0x50536F43) to a Write Once Latch (WOL). The WOL must be programmed at VDDD ≤ 3.3 V and T_J = 25 °C ±15 °C.

The WOL is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a ‘1’ if a super-majority (28 of 32) of its bits match a pre-determined pattern (0x50536F43); it outputs a ‘0’ if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0x50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see “Flash Security” section on page 16). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out via SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 5 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable.”

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

Table 11-6. GPIO DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
C_{IN}	Input capacitance[24]	GPIOs not shared with opamp outputs or kHzECO or SAR ADC external reference inputs	–	4	7	pF
		GPIOs shared with kHzECO[25]	–	5	7	pF
		GPIOs shared with opamp outputs	–	–	18	pF
		GPIOs shared with SAR ADC external reference inputs	–	–	30	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[27]		–	150	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA
Rglobal	Resistance pin to analog global bus	25 °C, V_{DDIO} = 3.0 V	–	320	–	Ω
Rmux	Resistance pin to analog mux bus	25 °C, V_{DDIO} = 3.0 V	–	220	–	Ω

Figure 11-5. GPIO Output High Voltage and Current

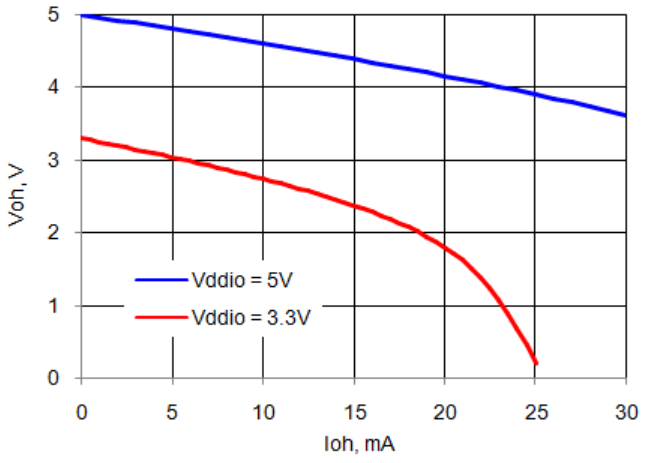


Figure 11-6. GPIO Output Low Voltage and Current

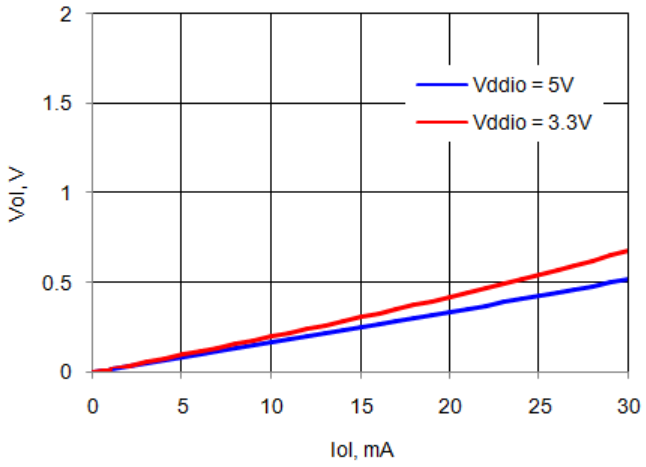


Table 11-7. GPIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode[27]	3.3 V V_{DDIO} Cload = 25 pF	–	–	12	ns
TfallF	Fall time in Fast Strong Mode[27]	3.3 V V_{DDIO} Cload = 25 pF	–	–	12	ns
TriseS	Rise time in Slow Strong Mode[27]	3.3 V V_{DDIO} Cload = 25 pF	–	–	60	ns
TfallS	Fall time in Slow Strong Mode[27]	3.3 V V_{DDIO} Cload = 25 pF	–	–	60	ns
Fgpioout	GPIO output operating frequency					
	Fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	3.3 V ≤ V_{DDIO} ≤ 5.5 V, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	7	MHz
	2.7 V ≤ V_{DDIO} < 3.3 V, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	3.5	MHz
Fgpioin	GPIO input operating frequency					
	2.7 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	66	MHz

Note
27. Based on device characterization (Not production tested).

11.5.4 SAR ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- Fclk = 14 MHz
- Input range = ± V_{REF}
- Bypass capacitor of 10 µF

Table 11-25. SAR ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	12	bits
	Number of channels – single-ended		–	–	No of GPIO	
	Number of channels – differential	Differential pair is formed using a pair of neighboring GPIO.	–	–	No of GPIO/2	
	Monotonicity[39]		Yes	–	–	
Ge	Gain error	External reference	–	–	±0.2	%
V_{OS}	Input offset voltage	V_{CM} = 0 V	–	–	±2	mV
		V_{CM} = $V_{DD/2}$			±6	
I_{DD}	Current consumption		–	–	1	mA
	Input voltage range – single-ended[39]		V_{SSA}	–	V_{DDA}	V
	Input voltage range – differential[39]		V_{SSA}	–	V_{DDA}	V
PSRR	Power supply rejection ratio[39]		70	–	–	dB
CMRR	Common mode rejection ratio		35	–	–	dB
INL	Integral non linearity[39]	Internal reference from V_{BG}	–	–	±2	LSB
DNL	Differential non linearity[39]	Internal reference from V_{BG}	–	–	±2	LSB

Figure 11-26. SAR ADC DNL vs Output Code, Bypassed Internal Reference Mode

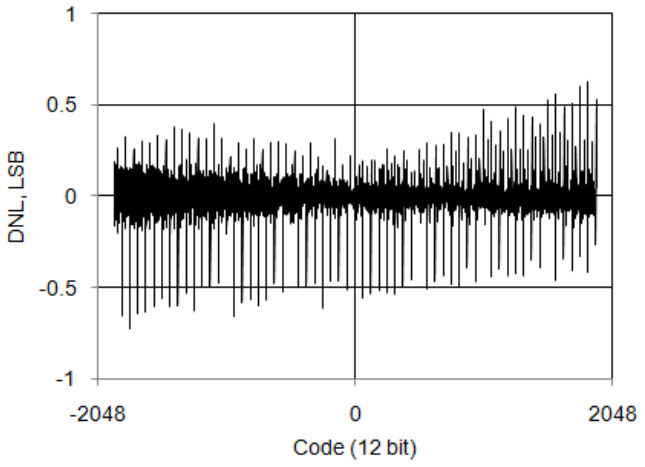
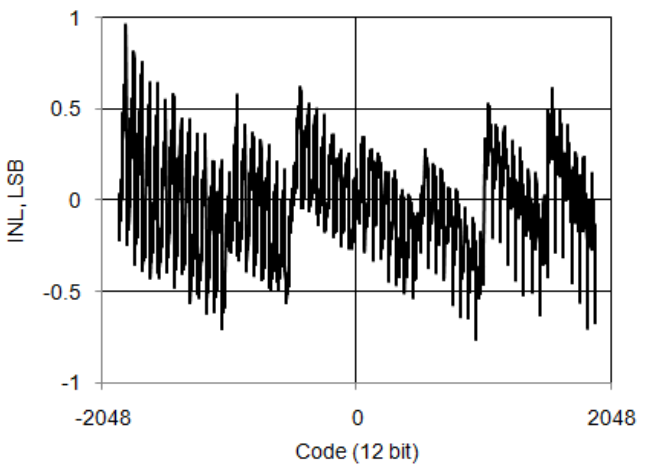


Figure 11-27. SAR ADC INL vs Output Code, Bypassed Internal Reference Mode



11.5.7 Current Digital-to-analog Converter (IDAC)

All specifications are based on use of the low-resistance IDAC output pins (see Pin Descriptions on page 9 for details). See the IDAC component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-30. IDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	8	bits
I_{OUT}	Output current at code = 255	Range = 2.04 mA, code = 255, Rload = 600 Ω	–	2.04	–	mA
		Range = 255 µA, code = 255, Rload = 600 Ω	–	255	–	µA
		Range = 31.875 µA, code = 255, Rload = 600 Ω	–	31.875	–	µA
	Monotonicity		–	–	Yes	
Ezs	Zero scale error		–	0	±2.5	LSB
Eg	Gain error		–	–	±5	%
TC_Eg	Temperature coefficient of gain error	Range = 2.04 mA	–	–	0.04	% / °C
		Range = 255 µA	–	–	0.04	% / °C
		Range = 31.875 µA	–	–	0.05	% / °C
INL	Integral nonlinearity	Range = 255 µA, Codes 8 – 255, Rload = 600 Ω, Cload = 15 pF	–	–	±3	LSB
DNL	Differential nonlinearity, non-monotonic	Range = 255 µA, Rload = 600 Ω, Cload = 15 pF	–	–	±1.6	LSB
Vcompliance	Dropout voltage, source or sink mode	Voltage headroom at max current, Rload to V_{DDA} or Rload to V_{SSA}, V_{DIFF} from V_{DDA}	1	–	–	V
I_{DD}	Operating current, code = 0	Slow mode, source mode, range = 31.875 µA	–	44	100	µA
		Slow mode, source mode, range = 255 µA,	–	33	100	µA
		Slow mode, source mode, range = 2.04 mA	–	33	100	µA
		Slow mode, sink mode, range = 31.875 µA	–	36	100	µA
		Slow mode, sink mode, range = 255 µA	–	33	100	µA
		Slow mode, sink mode, range = 2.04 mA	–	33	100	µA
		Fast mode, source mode, range = 31.875 µA	–	310	500	µA
		Fast mode, source mode, range = 255 µA	–	305	500	µA
		Fast mode, source mode, range = 2.04 mA	–	305	500	µA
		Fast mode, sink mode, range = 31.875 µA	–	310	500	µA
		Fast mode, sink mode, range = 255 µA	–	300	500	µA
		Fast mode, sink mode, range = 2.04 mA	–	300	500	µA

Table 11-31. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	5.5	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	180	ns
	Current noise	Range = 255 µA, source mode, fast mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-42. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V

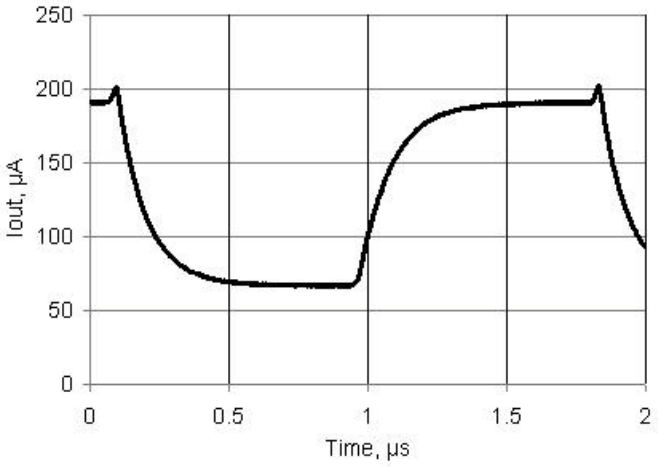


Figure 11-43. IDAC PSRR vs Frequency

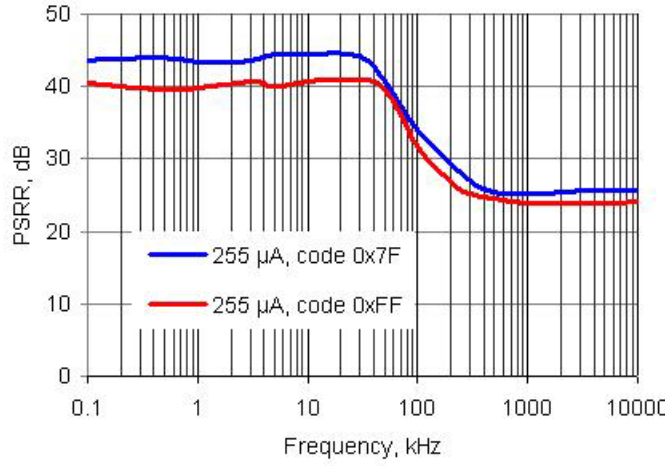


Figure 11-44. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V

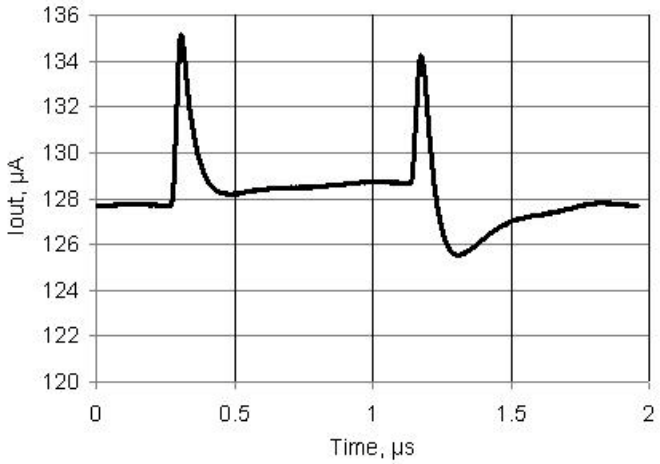
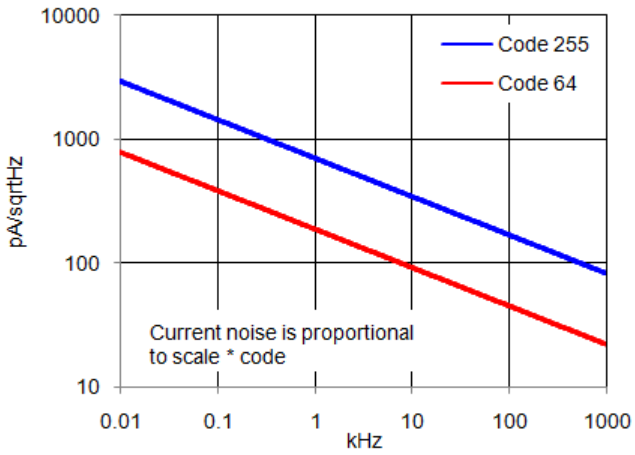


Figure 11-45. IDAC Current Noise, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V



11.5.11 Programmable Gain Amplifier

The PGA is created using a SC/CT analog block; see the PGA component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-38. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vin	Input voltage range	Power mode = minimum	V_{SSA}	–	V_{DDA}	V
Vos	Input offset voltage	Power mode = high, gain = 1	–	–	20	mV
TCVos	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
Ge1	Gain error, gain = 1		–	–	±2	%
Ge16	Gain error, gain = 16		–	–	±8	%
Ge50	Gain error, gain = 50		–	–	±10	%
Vonl	DC output nonlinearity	Gain = 1	–	–	±0.1	% of FSR
Cin	Input capacitance		–	–	7	pF
Voh	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	V_{DDA} – 0.15	–	–	V
Vol	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	–	–	V_{SSA} + 0.15	V
Vsrc	Output voltage under load	Iload = 250 µA, power mode = high	–	–	300	mV
Idd	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

Table 11-39. PGA AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1, noninverting mode, 300 mV ≤ VIN ≤ V_{DDA} – 1.2 V, CI ≤ 25 pF	6	8	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	–	–	V/µs
e_n	Input noise density	Power mode = high, V_{DDA} = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

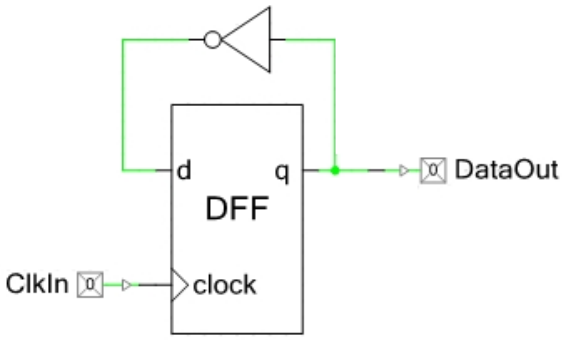
11.6.7 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component datasheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-53. UDB AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F_{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		–	–	67.01	MHz
F_{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		–	–	67.01	MHz
F_{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	67.01	MHz
PLD Performance						
F_{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	67.01	MHz
Clock to Output Performance						
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-60.	25 °C	–	20	28	ns
t_{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-60.	Worst-case placement, routing, and pin selection	–	–	55	ns

Figure 11-60. Clock to Output Performance



11.9.3 Internal Low Speed Oscillator

Table 11-70. ILO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time, all frequencies	Turbo mode	–	–	2.5	ms
F_{ILO}	ILO frequencies (trimmed)					
	100 kHz		45	100	200	kHz
	1 kHz		0.5	1	2	kHz
	ILO frequencies (untrimmed)					
	100 kHz		30	100	300	kHz
	1 kHz		0.3	1	3.5	kHz

Figure 11-65. ILO Frequency Variation vs. Temperature

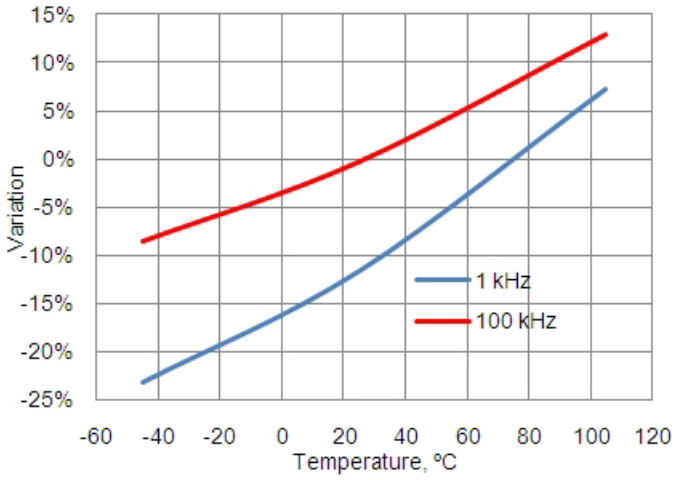
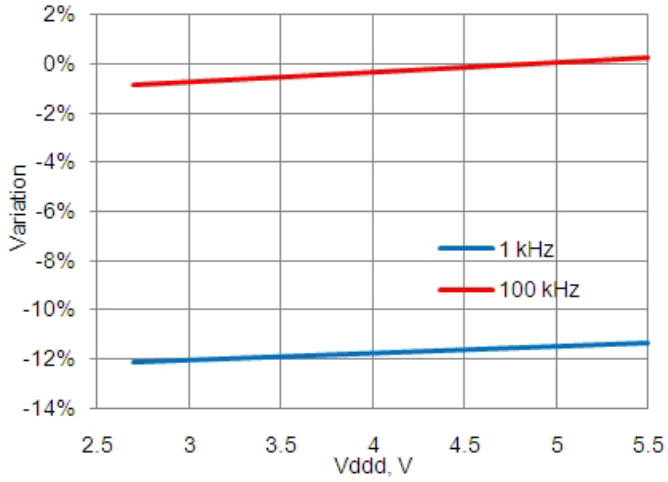


Figure 11-66. ILO Frequency Variation vs. V_{DD}



11.9.4 MHz External Crystal Oscillator (MHzECO)

For more information on crystal or ceramic resonator selection for the MHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-71. MHzECO Crystal Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency		4	–	25	MHz
C_L	Crystal load capacitance		–	–	20	pF
C0	Crystal shunt capacitance		–	–	7	pF
ESR	Crystal effective series resistance	4 MHz ≤ F < 8 MHz	–	–	125	Ω
		8 MHz ≤ F < 12 MHz	–	–	75	Ω
		12 MHz ≤ F ≤ 25 MHz	–	–	50	Ω
DL	Crystal drive level tolerance	No Rs, see AN54439	500	–	–	µW
C_{IN}	Capacitance at Pins MHz-XTAL:Xi and MHz-XTAL:Xo[50]		–	4	–	pF

Note
50. Based on device characterization (Not production tested).

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts