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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I ² C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 1x20b, 1x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5567lti-079

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Figure 2-2. 100-pin TQFP Part Pinout

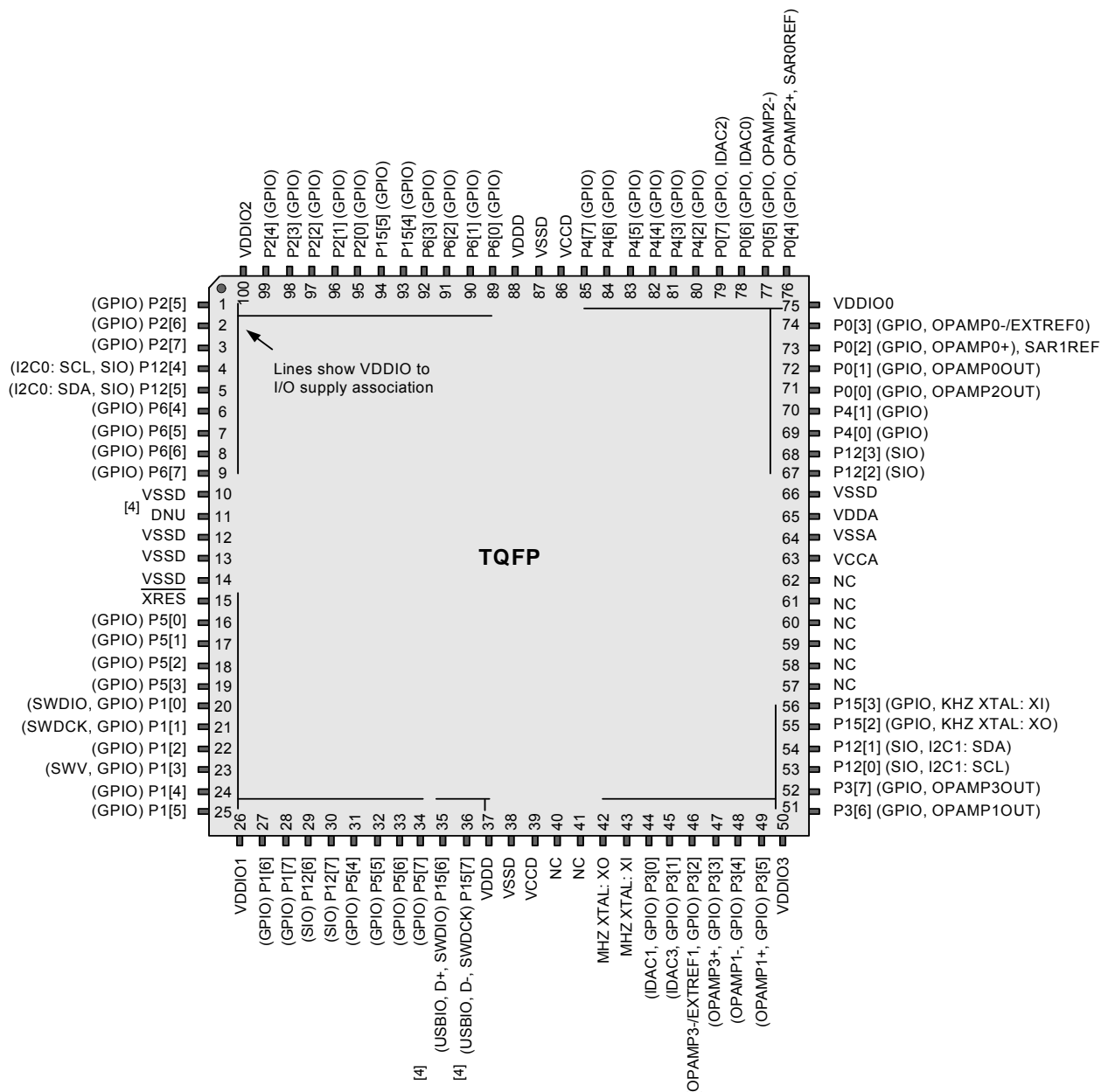


Figure 2-3 and Figure 2-4 on page 9 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-3 and Power System on page 21. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled VSSD must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note [AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5](#).

Note

4. Pins labeled Do Not Use (DNU) must be left floating. USB pins on devices without USB are DNU.

4.2 Cache Controller

The CY8C55 family has 128 bytes of direct mapped instruction cache between the CPU and the flash memory. This allows the CPU to access instructions much faster. The cache is enabled by default but user have the option to disable it.

4.3 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.3.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8-, 16-, 24-, and 32-bit addressing and data

Table 4-3. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU
2	PHUB local configuration, Power manager, Clocks, IC, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, I ² C, Timers, Counters, and PWMs
5	DFB
6	UDBs group 1
7	UDBs group 2

4.3.2 DMA Features

- 24 DMA channels
- Each channel has one or more transaction descriptors (TDs) to configure channel behavior. Up to 127 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel

- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64k bytes
- Large transactions may be broken into smaller bursts of 1 to 127 bytes
- TDs may be nested and/or chained for complex transactions

4.3.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100% of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in [Table 4-4](#) after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

Table 4-4. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

4.3.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

4.3.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in [Figure 4-2](#). For more description on other transfer modes, refer

4.4 Interrupt Controller

The Cortex-M3 NVIC supports 16 system exceptions and 32 interrupts from peripherals, as shown in [Table 4-5](#).

Table 4-5. Cortex-M3 Exceptions and Interrupts

Exception Number	Exception Type	Priority	Exception Table Address Offset	Function
			0x00	Starting value of R13 / MSP
1	Reset	–3 (highest)	0x04	Reset
2	NMI	–2	0x08	Non maskable interrupt
3	Hard fault	–1	0x0C	All classes of fault, when the corresponding fault handler cannot be activated because it is currently disabled or masked
4	MemManage	Programmable	0x10	Memory management fault, for example, instruction fetch from a nonexecutable region
5	Bus fault	Programmable	0x14	Error response received from the bus system; caused by an instruction prefetch abort or data access error
6	Usage fault	Programmable	0x18	Typically caused by invalid instructions or trying to switch to ARM mode
7-10	–	–	0x1C – 0x28	Reserved
11	SVC	Programmable	0x2C	System service call via SVC instruction
12	Debug monitor	Programmable	0x30	Debug monitor
13	–	–	0x34	Reserved
14	PendSV	Programmable	0x38	Deferred request for system service
15	SYSTICK	Programmable	0x3C	System tick timer
16-47	IRQ	Programmable	0x40 – 0x3FC	Peripheral interrupt request #0 - #31

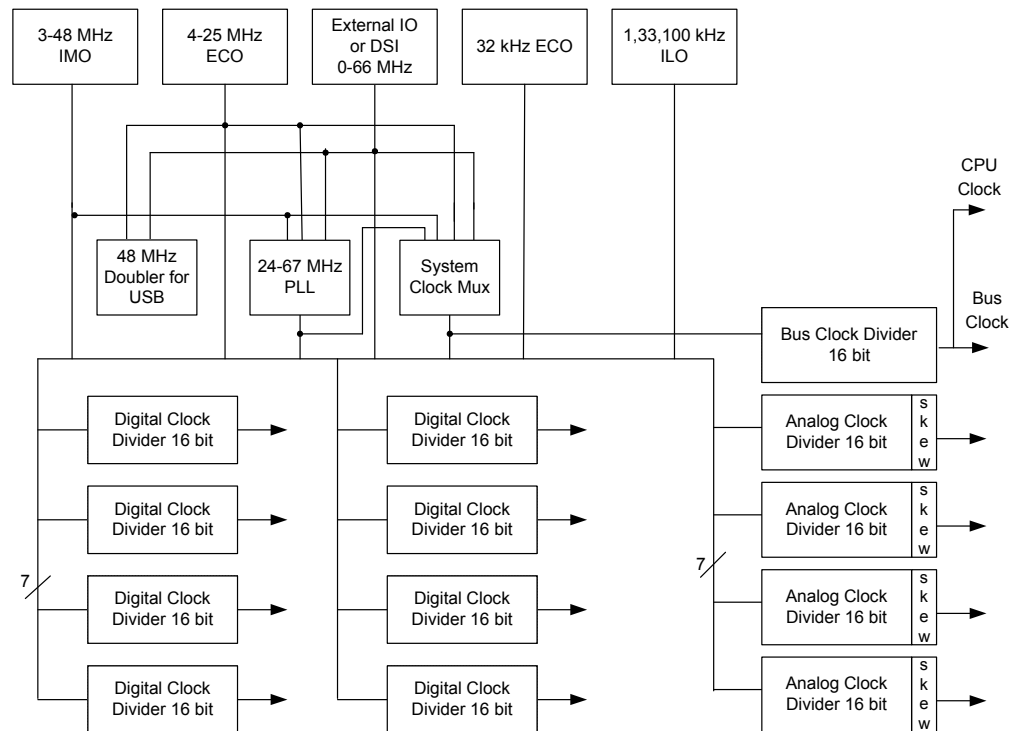
Bit 0 of each exception vector indicates whether the exception is executed using ARM or Thumb instructions. Because the Cortex-M3 only supports Thumb instructions, this bit must always be 1. The Cortex-M3 non maskable interrupt (NMI) input can be routed to any pin, via the DSI, or disconnected from all pins. See “[DSI Routing Interface Description](#)” section on page 38.

The Nested Vectored Interrupt Controller (NVIC) handles interrupts from the peripherals, and passes the interrupt vectors to the CPU. It is closely integrated with the CPU for low latency interrupt handling. Features include:

- 32 interrupts. Multiple sources for each interrupt.
- Configurable number of priority levels: from 3 to 8.
- Dynamic reprioritization of interrupts.
- Priority grouping. This allows selection of preempting and non preempting interrupt levels.

- Support for tail-chaining, and late arrival, of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. All interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Figure 6-1. Clocking Subsystem


6.1.1 Internal Oscillators

6.1.1.1 Internal Main Oscillator

The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from $\pm 5\%$ at 3 MHz, up to $\pm 10\%$ at 48 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency. The IMO provides clock outputs at 3, 6, 12, 24, and 48 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works at input frequency of 24 MHz, providing 48 MHz for the USB. It can be configured to use a clock from the MHzECO or the DSI (external pin). The doubler is typically used to clock the USB.

6.1.1.3 Phase-Locked Loop

The PLL allows low frequency, high accuracy clocks to be multiplied to higher frequencies. This is a tradeoff between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 67 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz,

where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 μ s (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO, or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low power modes.

6.1.1.4 Internal Low-Speed Oscillator

The ILO provides clock frequencies for low power consumption, including the sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz.

The 1 kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to long sleep intervals using the central timewheel (CTW). The central timewheel is a free running counter clocked by the ILO 1 kHz output. The central timewheel is always enabled except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low power mode. Firmware can reset the central timewheel.

The central timewheel can be programmed to wake the system periodically and optionally issue an interrupt. This enables flexible, periodic wakeups from low power modes or coarse timing applications. Systems that require accurate timing should use the RTC capability instead of the central timewheel. The 100 kHz clock (CLK100K) works as a low power system clock to run the CPU. It can also generate fast time intervals using the fast timewheel.

■ Features supported by both GPIO and SIO:

- Separate I/O supplies and voltages for up to four groups of I/O
- Digital peripherals use DSI to connect the pins
- Input or output or both for CPU and DMA
- Eight drive modes
- Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
- Dedicated port interrupt vector for each port
- Slew rate controlled digital output drive mode
- Access port control and configuration registers on either port basis or pin basis
- Separate port read (PS) and write (DR) data registers to avoid read modify write errors
- Special functionality on a pin by pin basis

■ Additional features only provided on the GPIO pins:

- LCD segment drive on LCD equipped devices
- CapSense on CapSense equipped devices^[11]
- Analog input and output capability
- Continuous 100 µA clamp current capability
- Standard drive strength down to 2.7 V

■ Additional features only provided on SIO pins:

- Higher drive strength than GPIO
- Hot swap capability (5 V tolerance at any operating VDD)
- Programmable and regulated high input and output drive levels down to 1.2 V
- No analog input or LCD capability
- Over voltage tolerance up to 5.5 V
- SIO can act as a general purpose analog comparator

■ USBIO features:

- Full speed USB 2.0 I/O
- Highest drive strength for general purpose use
- Input, output, or both for CPU and DMA
- Input, output, or both for digital peripherals
- Digital output (CMOS) drive mode
- Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

Figure 6-7. GPIO Block Diagram

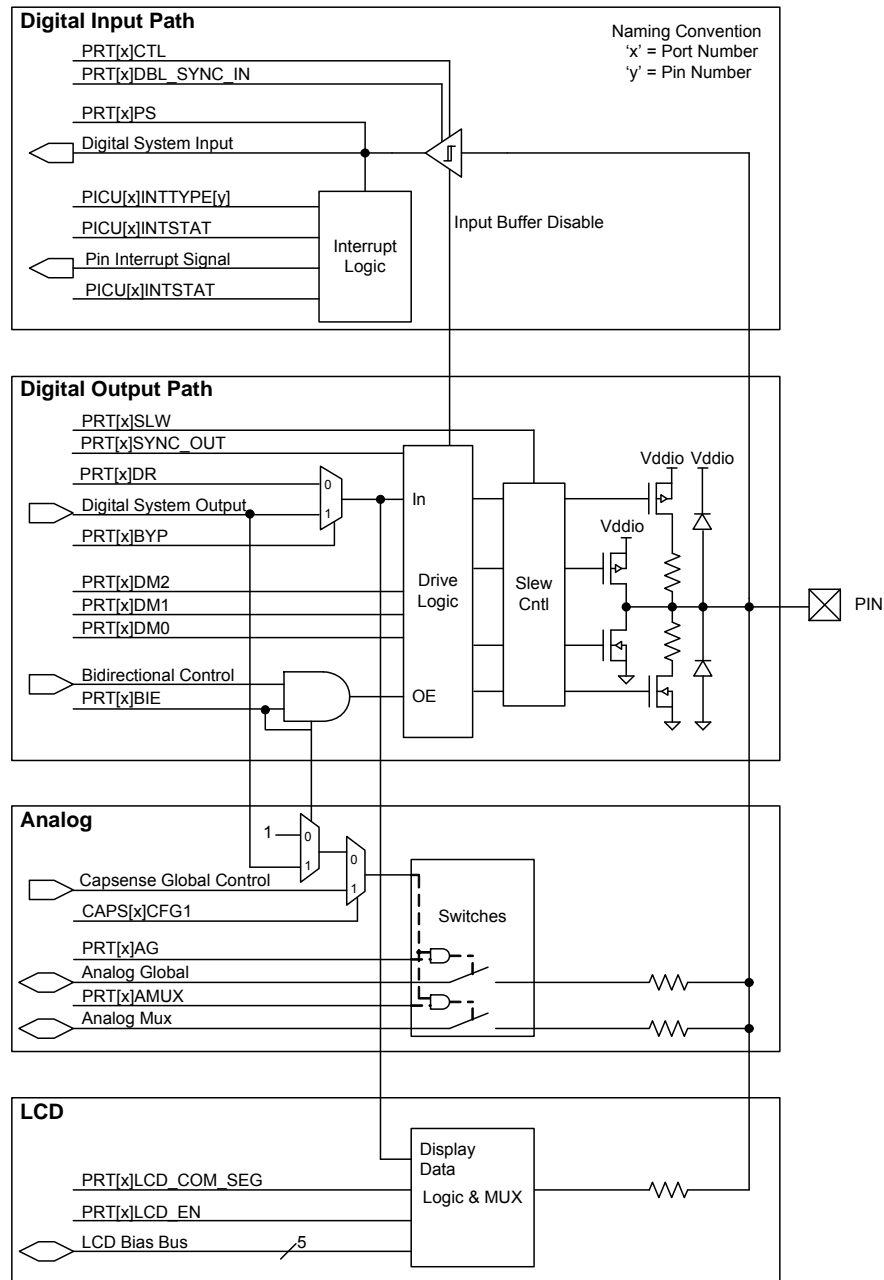
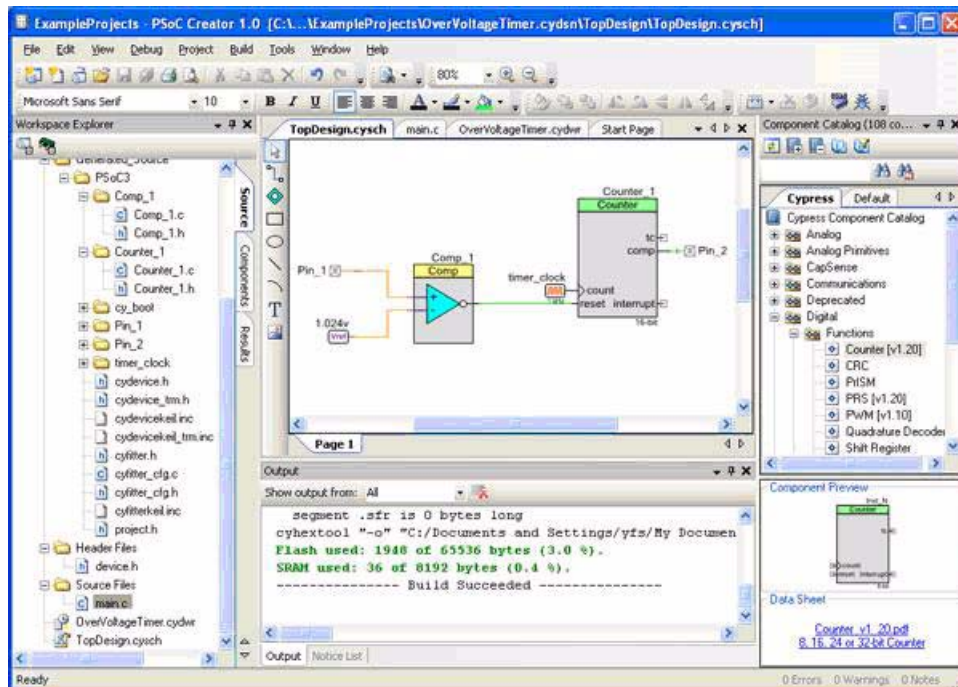
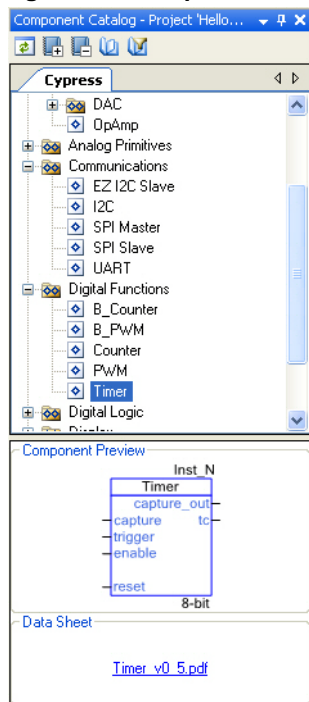


Figure 7-2. PSoC Creator Framework



7.1.4.2 Component Catalog

Figure 7-3. Component Catalog



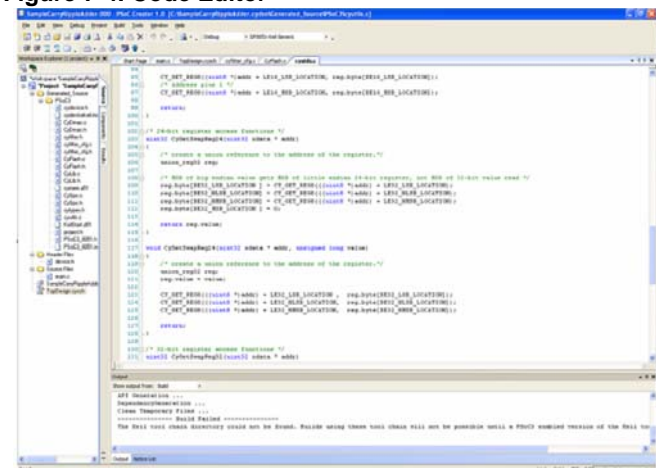
The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADCs, DACs, and filters, and communication protocols, such as I²C and USB. See “[Example Peripherals](#)” section on page 31 for more details about available peripherals. All content is fully characterized and carefully documented in datasheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

7.1.4.4 Software Development

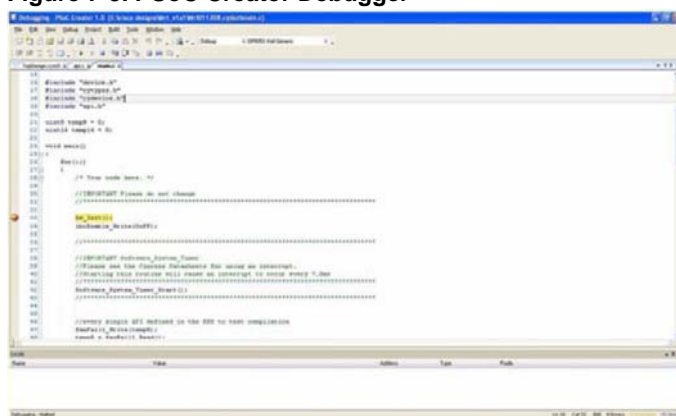
Figure 7-4. Code Editor



Anchoring the tool is a modern, highly customizable user interface. It includes project management and integrated editors for C and assembler source code, as well the design entry tools. Project build control leverages compiler technology from top commercial vendors such as ARM® Limited, Keil™, and CodeSourcery (GNU). Free versions of Keil C51 and GNU C Compiler (GCC) for ARM, with no restrictions on code size or end product distribution, are included with the tool distribution. Upgrading to more optimizing compilers is a snap with support for the professional Keil C51 product and ARM RealView™ compiler.

7.1.4.5 Nonintrusive Debugging

Figure 7-5. PSoC Creator Debugger



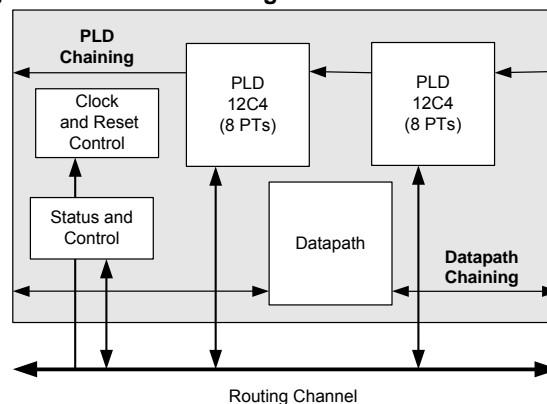
With SWD debug connectivity available on all devices, the PSoC Creator debugger offers full control over the target device with minimum intrusion. Breakpoints and code execution commands are all readily available from toolbar buttons and an impressive lineup of windows—register, locals, watch, call stack, memory and peripherals—make for an unparalleled level of visibility into the system. PSoC Creator contains all the tools necessary to complete a design, and then to maintain and extend that design for years to come. All steps of the design flow are carefully integrated and optimized for ease-of-use and to maximize productivity.

7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I²C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-6. UDB Block Diagram



The main component blocks of the UDB are:

- **PLD blocks** - There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- **Datapath Module** - This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- **Status and Control Module** - The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- **Clock and Reset Module** - This block provides the UDB clocks and reset selection and control.

7.5 USB

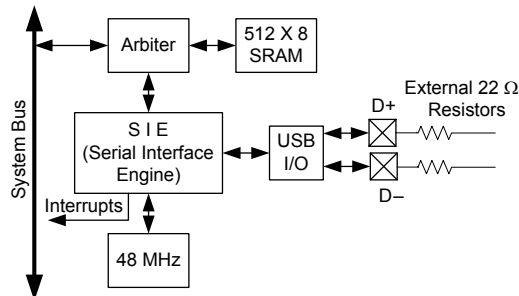
PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the “I/O System and Routing” section on page 24.

When using USB, either a crystal must be used (24 MHz with MHzECO) or a similar high-accuracy clock source must be provided externally through a pin and the DSI. Also, bus clock must be equal to 33 MHz. See Section 6.1 on page 18 for details.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Two memory modes
 - Manual Memory Management with No DMA Access
 - Manual Memory Management with Manual DMA Access
- Internal 3.3 V regulator for transceiver
- Interrupts on bus and each endpoint event
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

Figure 7-11. USB



7.6 Timers, Counters, and PWMs

The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows designers to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output and terminal count output (optional complementary compare output). The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit timer/counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One-shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-12. Timer/Counter/PWM

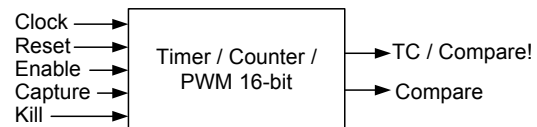
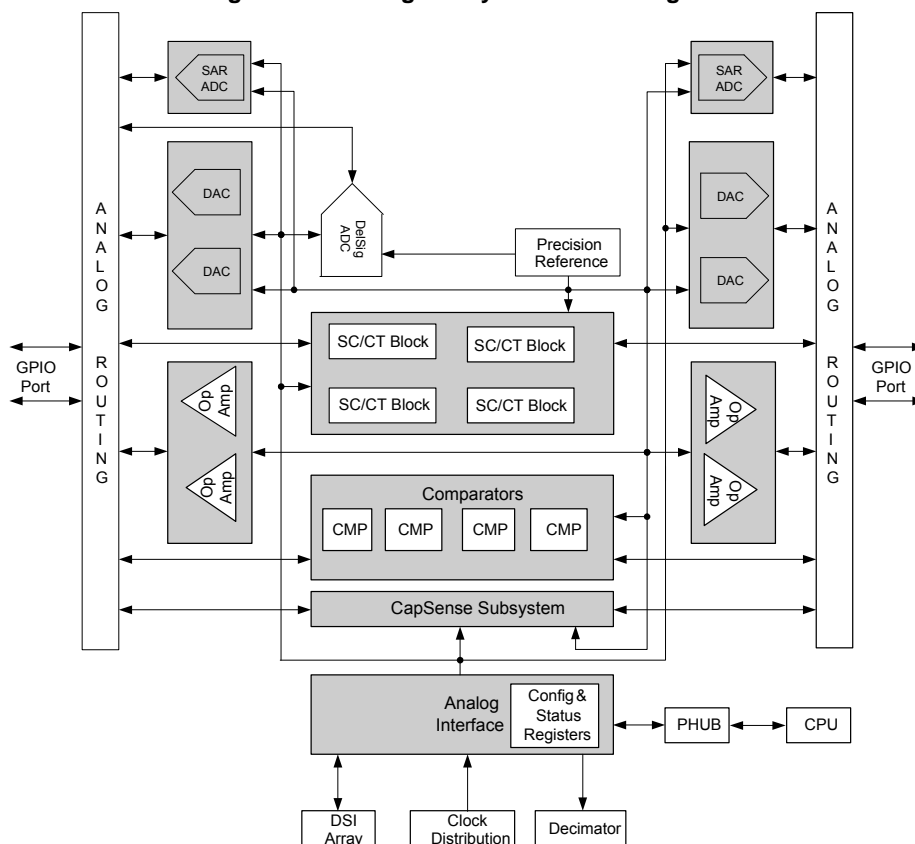
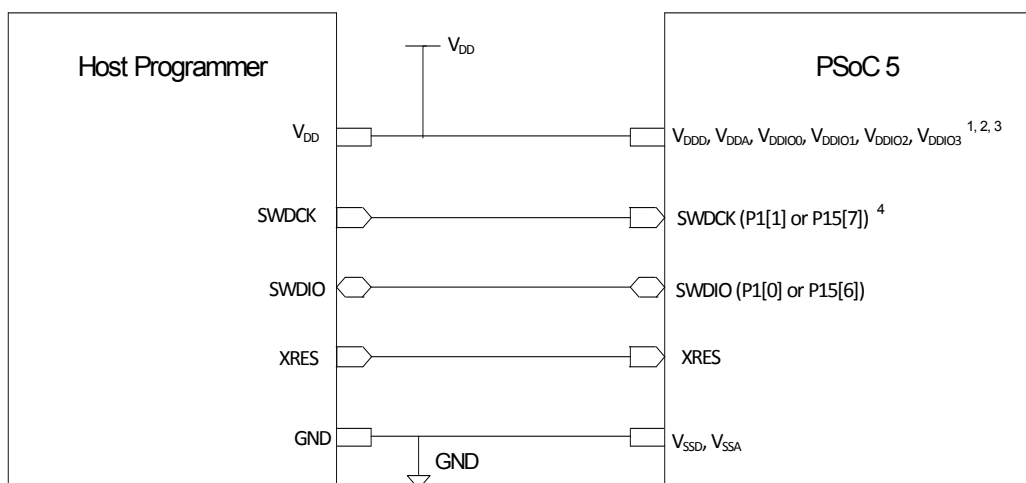


Figure 8-1. Analog Subsystem Block Diagram


The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and also connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions (PGA, transimpedance amplifier, voltage DAC, current DAC, and so on). The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

Figure 9-1. SWD Interface Connections between PSoC 5 and Programmer


¹ The voltage levels of the Host Programmer and the PSoC 5 voltage domains involved in programming should be the same. XRES pin is powered by V_{DDIO1}. The USB SWD pins are powered by V_{DD}. So for programming using the USB SWD pins with XRES pin, the V_{DD}, V_{DDIO1} of PSoC 5 should be at the same voltage level as Host V_{DD}. Rest of PSoC 5 voltage domains (V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by V_{DDIO1}. So V_{DDIO1} of PSoC 5 should be at same voltage level as host V_{DD} for Port 1 SWD programming. Rest of PSoC 5 voltage domains (V_{DD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

² V_{dda} must be greater than or equal to all other power supplies (V_{ddd}, V_{ddio}'s) in PSoC 5.

³ For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (V_{ddd}, V_{dda}, All V_{ddio}'s) to PSoC 5. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, V_{dda} must be greater than or equal to all other supplies.

⁴ When USB SWD pins are used for Programming, the P1[1] SWDCK pin must be externally connected to Ground using external pull-down resistor (around 100 K resistor). This is required for P15[7] SWDCK signal to be seen by PSoC 5's internal logic.

Table 11-3. AC Specifications^[22]

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{CPU}	CPU frequency		DC	–	67.01	MHz
F _{BUSCLK}	Bus frequency		DC	–	67.01	MHz
S _{VDD}	V _{DD} ramp rate		–	–	0.066	V/μs
T _{STARTUP}	Time from V _{DDD} /V _{DDA} /V _{CCD} /V _{CCA} ≥ min operating voltage to CPU executing code at reset vector	No PLL used, IMO boot mode 12 MHz typ.	–	45	80	μs
T _{SLEEP}	Wakeup from sleep – CTW timeout to beginning of execution of next CPU instruction		–	125	–	μs
T _{SLEEP_INT}	Sleep timer periodic wakeup interval		–	–	128	ms

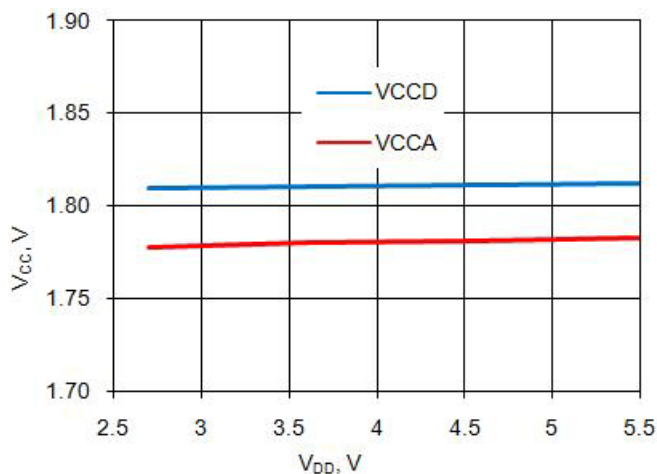
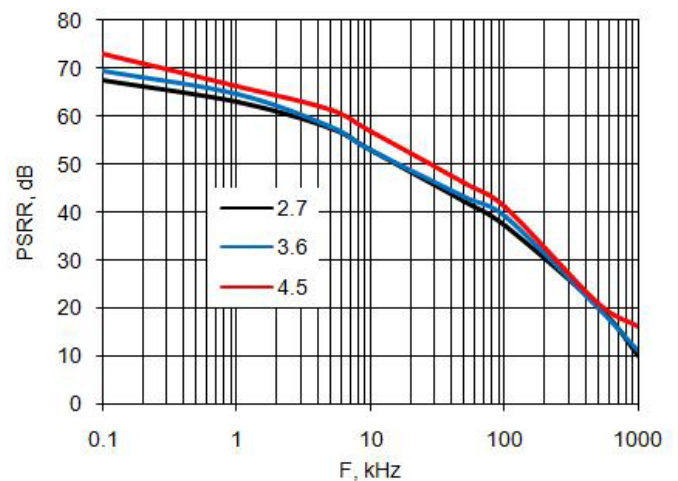
11.3 Power Regulators

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{DDD}	Input voltage		2.7	–	5.5	V
V _{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor ^[23]	±10%, X5R ceramic or better. The two V _{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 21	–	1	10	μF

Figure 11-2. Regulators V_{CC} vs V_{DD}

Figure 11-3. Digital Regulator PSRR vs Frequency and V_{DD}


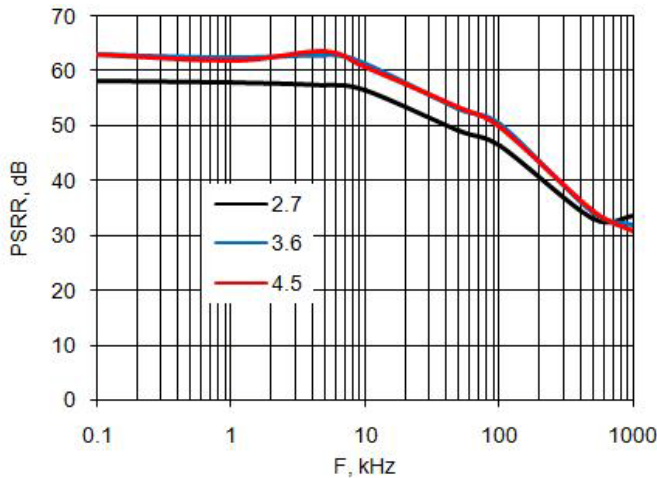
Notes

21. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.
22. Based on device characterization (Not production tested).
23. 10 μF is required for sleep mode. See [Table 11-3](#).

11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{DDA}	Input voltage		2.7	–	5.5	V
V _{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor ^[26]	±10%, X5R ceramic or better	–	1	10	μF

Figure 11-4. Analog Regulator PSRR vs Frequency and V_{DD}


11.4 Inputs and Outputs

Specifications are valid for $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ and $T_J \leq 100^{\circ}\text{C}$, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.4.1 GPIO

Table 11-6. GPIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{IH}	Input voltage high threshold	CMOS Input, PRT[x]CTL = 0	$0.7 \times V_{DDIO}$	–	–	V
V _{IL}	Input voltage low threshold	CMOS Input, PRT[x]CTL = 0	–	–	$0.3 \times V_{DDIO}$	V
V _{IH}	Input voltage high threshold	LVTTL Input, PRT[x]CTL = 1	2.0	–	–	V
V _{IL}	Input voltage low threshold	LVTTL Input, PRT[x]CTL = 1	–	–	0.8	V
V _{OH}	Output voltage high	I _{OH} = 4 mA at 3.3 V _{DDIO}	$V_{DDIO} - 0.6$	–	–	V
V _{OL}	Output voltage low	I _{OL} = 8 mA at 3.3 V _{DDIO}	–	–	0.6	V
R _{pullup}	Pull-up resistor		3.5	5.6	8.5	kΩ
R _{pulldown}	Pull-down resistor		3.5	5.6	8.5	kΩ
I _{IL}	Input leakage current (absolute value) ^[24]	25 °C, V _{DDIO} = 3.0 V	–	–	2	nA

Notes

24. Based on device characterization (Not production tested).

25. For information on designing with PSoC 3 oscillators, refer to the application note, [AN54439 - PSoC® 3 and PSoC 5 External Oscillator](#).

26. 10 μF is required for sleep mode. See [Table 11-3](#).

11.5.4 SAR ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- Fclk = 14 MHz
- Input range = $\pm V_{REF}$
- Bypass capacitor of 10 μ F

Table 11-25. SAR ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	–	12	bits
	Number of channels – single-ended		–	–	No of GPIO	
	Number of channels – differential	Differential pair is formed using a pair of neighboring GPIO.	–	–	No of GPIO/2	
	Monotonicity ^[39]		Yes	–	–	
Ge	Gain error	External reference	–	–	± 0.2	%
V _{OS}	Input offset voltage	V _{CM} = 0 V	–	–	± 2	mV
		V _{CM} = V _{DD} /2			± 6	
I _{DD}	Current consumption		–	–	1	mA
	Input voltage range – single-ended ^[39]		V _{SSA}	–	V _{DDA}	V
	Input voltage range – differential ^[39]		V _{SSA}	–	V _{DDA}	V
PSRR	Power supply rejection ratio ^[39]		70	–	–	dB
CMRR	Common mode rejection ratio		35	–	–	dB
INL	Integral non linearity ^[39]	Internal reference from V _{BG}	–	–	± 2	LSB
DNL	Differential non linearity ^[39]	Internal reference from V _{BG}	–	–	± 2	LSB

Figure 11-26. SAR ADC DNL vs Output Code, Bypassed Internal Reference Mode

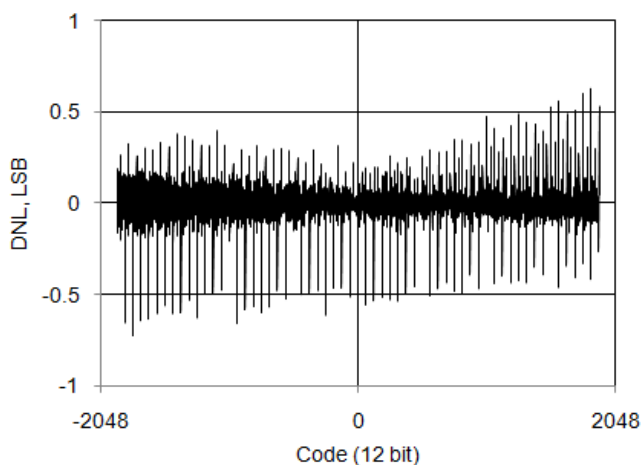
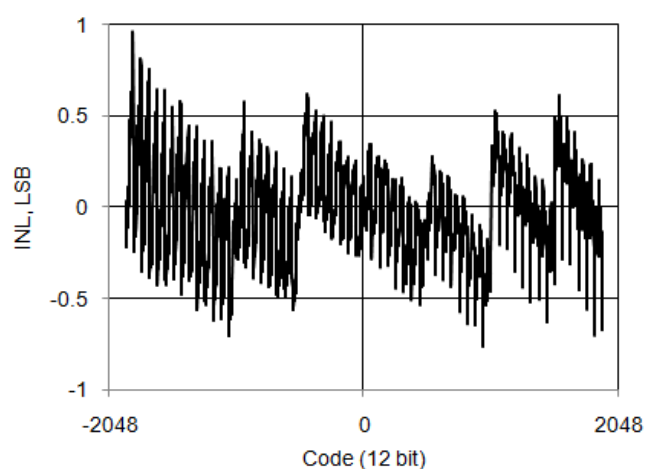


Figure 11-27. SAR ADC INL vs Output Code, Bypassed Internal Reference Mode



11.5.6 Comparator

Table 11-28. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V _{OS}	Input offset voltage in fast mode	Factory trim, V _{in} ≥ 0.5 V	–		15	mV
	Input offset voltage in slow mode	Factory trim, V _{in} ≥ 0.5 V	–		15	mV
V _{OS}	Input offset voltage in ultra low power mode		–	±12	–	mV
V _{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V _{ICM}	Input common mode voltage	High current / fast mode	V _{SSA}	–	V _{DDA} – 0.1	V
		Low current / slow mode	V _{SSA}	–	V _{DDA}	V
		Ultra low power mode	V _{SSA}	–	V _{DDA} – 0.9	
CMRR	Common mode rejection ratio		–	50	–	dB
I _{CMP}	High current mode/fast mode ^[40]		–	–	400	μA
	Low current mode/slow mode ^[40]		–	–	100	μA
	Ultra low power mode ^[40]		–	6	–	μA

Table 11-29. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T _{RESP}	Response time, high current mode ^[40]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode ^[40]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low power mode ^[40]	50 mV overdrive, measured pin-to-pin	–	55	–	μs

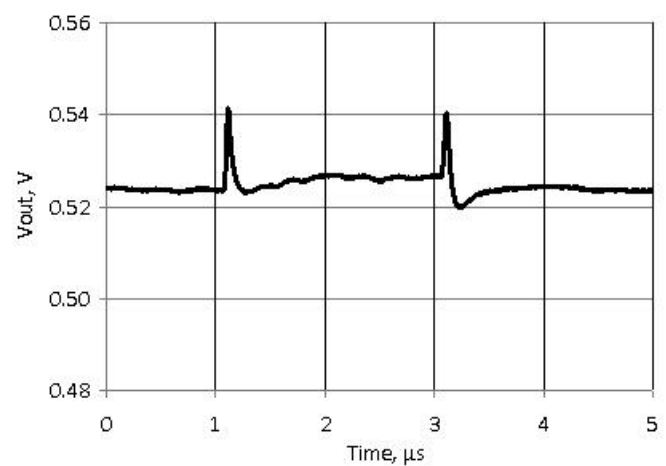
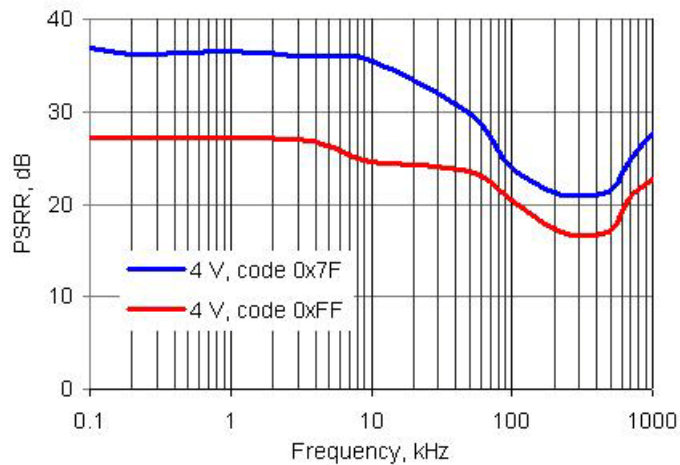
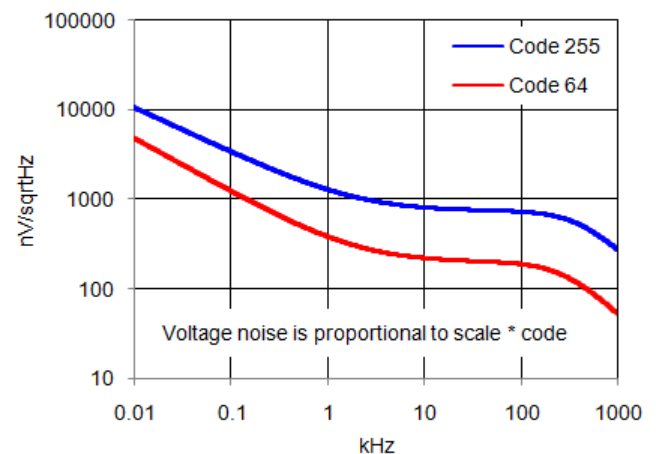
Note

40. Based on device characterization (Not production tested).

Table 11-33. VDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{DAC}	Update rate	1 V scale	–	–	1000	ksps
		4 V scale	–	–	250	ksps
T _{settleP}	Settling time to 0.1%, step 25% to 75%	1 V scale, Cload = 15 pF	–	0.45	1	μs
		4 V scale, Cload = 15 pF	–	0.8	4	μs
T _{settleN}	Settling time to 0.1%, step 75% to 25%	1 V scale, Cload = 15 pF	–	0.45	1	μs
		4 V scale, Cload = 15 pF	–	0.7	4	μs
	Voltage noise	Range = 1 V, fast mode, V _{DDA} = 5 V, 10 kHz	–	750	–	nV/sqrtHz

Figure 11-54. VDAC Step Response, Codes 0x40 - 0xC0, 1 V Mode, Fast Mode, V_{DDA} = 5 V

Figure 11-56. VDAC Glitch Response, Codes 0x7F - 0x80, 1 V Mode, Fast Mode, V_{DDA} = 5 V

Figure 11-55. VDAC PSRR vs Frequency

Figure 11-57. VDAC Voltage Noise, 1 V Mode, Fast Mode, V_{DDA} = 5 V


11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component data sheet in PSoC Creator.

Table 11-46. PWM DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	16-bit PWM block current consumption	Input clock frequency – 3 MHz	–	65	–	μA
		Input clock frequency – 12 MHz	–	170	–	μA
		Input clock frequency – 48 MHz	–	650	–	μA
		Input clock frequency – 67 MHz	–	900	–	μA

Table 11-47. PWM AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	67.01	MHz
	Pulse width		13	–	–	ns
	Pulse width (external)		30	–	–	ns
	Kill pulse width		13	–	–	ns
	Kill pulse width (external)		30	–	–	ns
	Enable pulse width		13	–	–	ns
	Enable pulse width (external)		30	–	–	ns
	Reset pulse width		13	–	–	ns
	Reset pulse width (external)		30	–	–	ns

11.6.4 I²C

Table 11-48. Fixed I²C DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	Enabled, configured for 100 kbps	–	90	250	μA
		Enabled, configured for 400 kbps	–	100	250	μA

Table 11-49. Fixed I²C AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate		–	–	400	Kbps

12. Ordering Information

In addition to the features listed in [Table 12-1](#), every CY8C55 device includes: up to 256 KB flash, 64 KB SRAM, 2 KB EEPROM, a precision on-chip voltage reference, precision oscillators, flash, DMA, a fixed function I²C, SWD programming and debug, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C55 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C55 Family with ARM Cortex-M3 CPU

Part Number	MCU Core				Analog								Digital			I/O ^[56]				Package	Device ID ^[57]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADCs	DAC	Comparators	SC/CT Analog Blocks ^[54]	Opamps	DFB	CapSense ^[55]	UDBs ^[55]	16-bit Timer/PWM	FS USB	Total I/O	GPIO	SIO	USBIO		
CY8C5568AXI-060	67	256	64	2	✓	1x 20-bit Del-Sig 2x 12-bit SAR	4	4	4	4	✓	✓	24	4	✓	70	60	8	2	100-pin TQFP	0x0E13C069
CY8C5568LTI-114	67	256	64	2	✓	1x 20-bit Del-Sig 2x 12-bit SAR	4	4	4	4	✓	✓	24	4	✓	46	36	8	2	68-pin QFN	0x0E172069
CY8C5567AXI-019	67	128	32	2	✓	1x 20-bit Del-Sig 1x 12-bit SAR	4	4	4	4	✓	✓	24	4	✓	70	60	8	2	100-pin TQFP	0x0E113069
CY8C5567LTI-079	67	128	32	2	✓	1x 20-bit Del-Sig 1x 12-bit SAR	4	4	4	4	✓	✓	24	4	✓	46	36	8	2	68-pin QFN	0x0E14F069
CY8C5566AXI-061	67	64	16	2	✓	1x 20-bit Del-Sig 1x 12-bit SAR	4	4	4	4	✓	✓	24	4	✓	70	60	8	2	100-pin TQFP	0x0E13D069
CY8C5566LTI-017	67	64	16	2	✓	1x20-bit Del-Sig 1x12-bit SAR	4	4	4	4	✓	✓	24	4	✓	46	36	8	2	68-pin QFN	0x0E111069

12.1 Part Numbering Conventions

PSoC 5 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, ..., 9, A, B, ..., Z) unless stated otherwise.

CY8Cabcdefg-xxx

■ a: Architecture

- 3: PSoC 3
- 5: PSoC 5

■ b: Family group within architecture

- 2: CY8C52 family
- 3: CY8C53 family
- 4: CY8C54 family
- 5: CY8C55 family

■ c: Speed grade

- 4: 40 MHz
- 6: 67 MHz

■ d: Flash capacity

- 5: 32 KB
- 6: 64 KB
- 7: 128 KB
- 8: 256 KB

■ ef: Package code

- Two character alphanumeric
- AX: TQFP
- LT: QFN

■ g: Temperature range

- C: commercial
- I: industrial
- A: automotive

■ xxx: Peripheral set

- Three character numeric
- No meaning is associated with these three characters

Notes

54. Analog blocks support a wide variety of functionality including TIA, PGA, and mixers. See [Example Peripherals on page 31](#) for more information on how analog blocks can be used.

55. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See [Example Peripherals on page 31](#) for more information on how UDBs can be used.

56. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See [I/O System and Routing on page 24](#) for details on the functionality of each of these types of I/O.

57. The device ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number, and a 3 nibble manufacturer ID.

Examples

		CY8C	5	5	6	8	AX/LT	I	-	x	x	x
	Cypress Prefix											
5: PSoC 5	Architecture											
5: CY8C55 Family	Family Group within Architecture											
6: 67 MHz	Speed Grade											
8: 256 KB	Flash Capacity											
AX: TQFP, LT: QFN	Package Code											
I: Industrial	Temperature Range											
	Peripheral Set											

All devices in the PSoC 5 CY8C55 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.