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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	67MHz
Connectivity	I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	60
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 1x20b, 2x12b; D/A 4x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c5568axi-060

Contents

PSoC's nonvolatile subsystem consists of flash and byte-writeable EEPROM. It provides up to 256 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling boot loaders. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Two KB of byte-writable EEPROM is available on-chip to store application data.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive, flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow V_{OH} to be set independently of VDDIO when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with FS USB, the USB physical interface is also provided (USBIO). When not using USB, these pins may also be used for limited digital functionality and device programming. All the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 24 of this datasheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The Internal Main Oscillator (IMO) is the master clock base for the system, and has 5% accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 48 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate system clock frequencies up to 67 MHz from the IMO, external crystal, or external reference clock. It also contains a separate, very low-power ILO for the sleep and watchdog timers. A 32.768 kHz external watch crystal is also supported for use in RTC applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C55 family supports a wide supply operating range from 2.7 to 5.5 V. This allows operation from regulated supplies such as 3.3 V ± 10% or 5.0 V ± 10%, or directly from a wide range of battery types.

PSoC supports a wide range of low power modes. These include a 300-nA hibernate mode with RAM retention and a 2-µA sleep mode.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 6 mA when the CPU is running at 6 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 21 of this data sheet.

PSoC uses a SWD interface for programming, debug, and test. Using this standard interface enables the designer to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. The Cortex-M3 debug and trace modules include FPB, DWT, and ITM. These modules have many features to help solve difficult debug and trace problems. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 53 of this data sheet.

2. Pinouts

The VDDIO pin that supplies a particular set of pins is indicated by the black lines drawn on the pinout diagrams in Figure 2-1 and Figure 2-2. Using the VDDIO pins, a single PSoC can support multiple interface voltage levels, eliminating the need for off-chip level shifters. Each VDDIO may sink up to 20 mA total to its associated I/O pins and opamps, and each set of VDDIO associated pins may sink up to 100 mA.

Figure 2-2. 100-pin TQFP Part Pinout

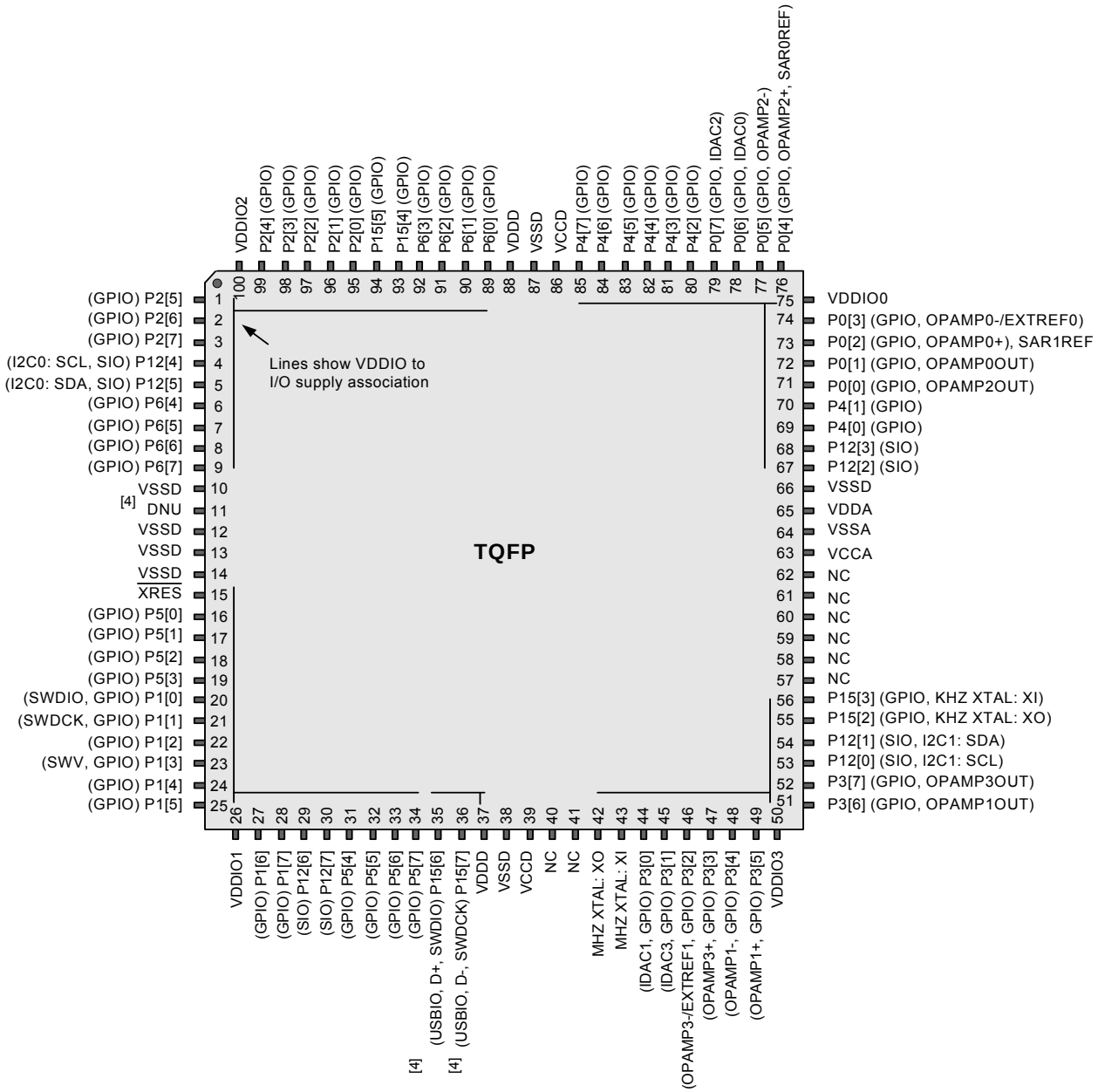


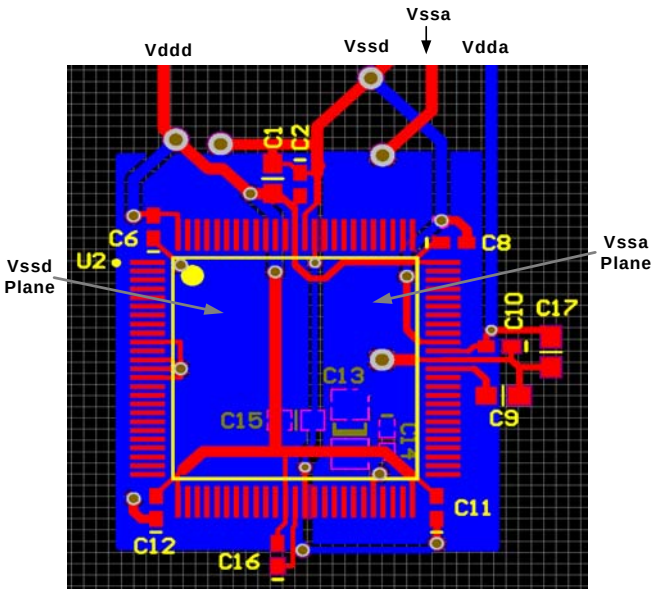
Figure 2-3 and Figure 2-4 on page 9 show an example schematic and an example PCB layout, for the 100-pin TQFP part, for optimal analog performance on a two-layer board.

- The two pins labeled VDDD must be connected together.
- The two pins labeled VCCD must be connected together, with capacitance added, as shown in Figure 2-3 and Power System on page 21. The trace between the two VCCD pins should be as short as possible.
- The two pins labeled VSSD must be connected together.

For information on circuit board layout issues for mixed signals, refer to the application note AN57821 - Mixed Signal Circuit Board Layout Considerations for PSoC® 3 and PSoC 5.

Note
4. Pins labeled Do Not Use (DNU) must be left floating. USB pins on devices without USB are DNU.

Figure 2-4. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0, IDAC1, IDAC2, IDAC3. Low-resistance output pin for high-current DACs (IDAC).

OpAmp0out, OpAmp1out, OpAmp2out, OpAmp3out. High current output of uncommitted opamp.[6]

Extref0, Extref1. External reference input to the analog system.

OpAmp0-, OpAmp1-, OpAmp2-, OpAmp3-. Inverting input to uncommitted opamp.

OpAmp0+, OpAmp1+, OpAmp2+, OpAmp3+. Noninverting input to uncommitted opamp.

SAR0ref, SAR1ref. External references for SAR ADCs.

GPIO. Provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense.[6]

kHz XTAL: Xo, kHz XTAL: Xi. 32.768 kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi. 4 to 25 MHz crystal oscillator pin. If a crystal is not used, then Xi must be shorted to ground and Xo must be left floating.

SIO. Provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK. SWD Clock programming and debug port connection. When programming and debugging using SWD is done over USBIOs, the SWDCK pin of port P1[1] is not available for use as a general purpose I/O and should be externally pulled down using a resistor of less than 100 KΩ.

SWDIO. SWD Input and Output programming and debug port connection.

SWV. SWV output.

USBIO, D+. Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from VDDD instead of from a VDDIO. Pins are Do Not Use (DNU) on devices without USB.

USBIO, D-. Provides D- connection directly to a USB 2.0 bus. May be used as a digital I/O pin; it is powered from VDDD instead of from a VDDIO. Pins are DNU on devices without USB.

VCCA. Output of analog core regulator and input to analog core. Requires a 1 µF capacitor to VSSA (10 µF is required for sleep mode. See Table 11-3). Regulator output not for external use.

VCCD. Output of digital core regulator and input to digital core. The two VCCD pins must be shorted together, with the trace between them as short as possible, and a 1 µF capacitor to VSSD (10 µF is required for sleep mode. See Table 11-3); see Power System on page 21. Regulator output not for external use.

VDDA. Supply for all analog peripherals and analog core regulator. **VDDA must be the highest voltage present on the device. All other supply pins must be less than or equal to VDDA.**[7]

VDDD. Supply for all digital peripherals and digital core regulator. VDDD must be less than or equal to VDDA.[7]

VSSA. Ground for all analog peripherals.

VSSD. Ground for all digital logic and I/O pins.

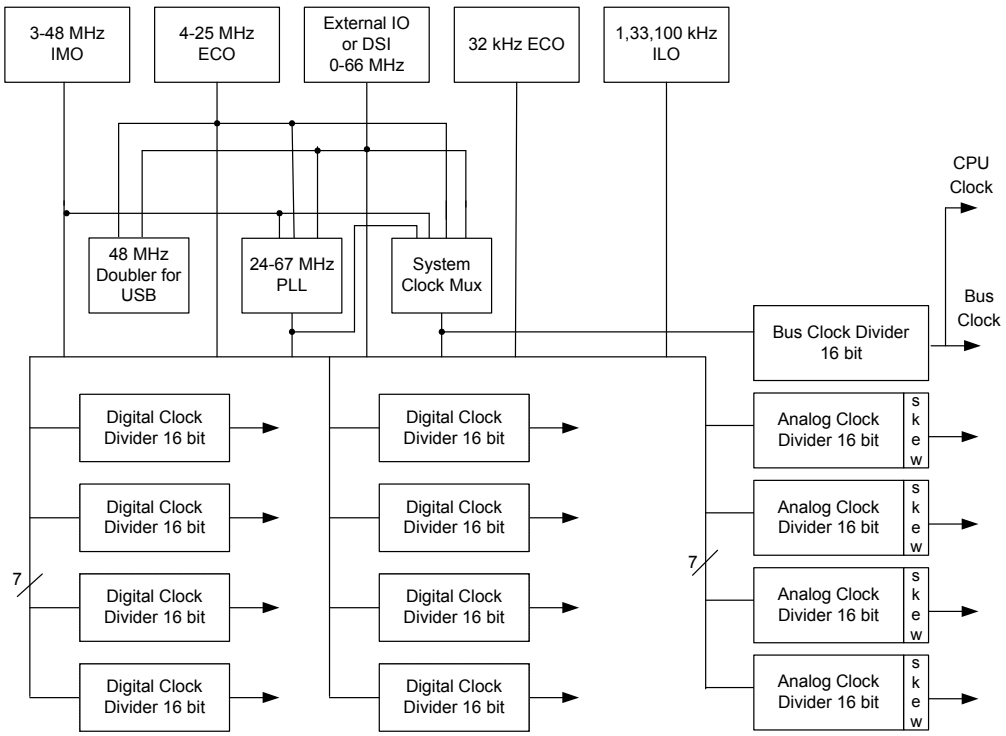
$VDDIO_0$, VDDIO1, VDDIO2, VDDIO3. Supply for I/O pins. Each VDDIO must be tied to a valid operating voltage (2.7 V to 5.5 V), and must be less than or equal to VDDA.

$\overline{XRES}$. External reset pin. Active low with internal pull-up.

RSVD. Reserved pins

Notes
6. GPIOs with opamp outputs are not recommended for use with CapSense.
7. VDDD and VDDA must be brought up in synchronization with each other, that is, at the same rates and levels. VDDA must be greater than or equal to all other supplies.

Figure 6-1. Clocking Subsystem



6.1.1 Internal Oscillators

6.1.1.1 Internal Main Oscillator

The IMO operates with no external components and outputs a stable clock. A factory trim for each frequency range is stored in the device. With the factory trim, tolerance varies from ±5% at 3 MHz, up to ±10% at 48 MHz. The IMO, in conjunction with the PLL, allows generation of CPU and system clocks up to the device's maximum frequency. The IMO provides clock outputs at 3, 6, 12, 24, and 48 MHz.

6.1.1.2 Clock Doubler

The clock doubler outputs a clock at twice the frequency of the input clock. The doubler works at input frequency of 24 MHz, providing 48 MHz for the USB. It can be configured to use a clock from the MHzECO or the DSI (external pin). The doubler is typically used to clock the USB.

6.1.1.3 Phase-Locked Loop

The PLL allows low frequency, high accuracy clocks to be multiplied to higher frequencies. This is a tradeoff between higher clock frequency and accuracy and, higher power consumption and increased startup time.

The PLL block provides a mechanism for generating clock frequencies based upon a variety of input sources. The PLL outputs clock frequencies in the range of 24 to 67 MHz. Its input and feedback dividers supply 4032 discrete ratios to create almost any desired system clock frequency. The accuracy of the PLL output depends on the accuracy of the PLL input source. The most common PLL use is to multiply the IMO clock at 3 MHz, where it is most accurate, to generate the CPU and system clocks up to the device's maximum frequency.

The PLL achieves phase lock within 250 µs (verified by bit setting). It can be configured to use a clock from the IMO, MHzECO, or DSI (external pin). The PLL clock source can be used until lock is complete and signaled with a lock bit. The lock signal can be routed through the DSI to generate an interrupt. Disable the PLL before entering low power modes.

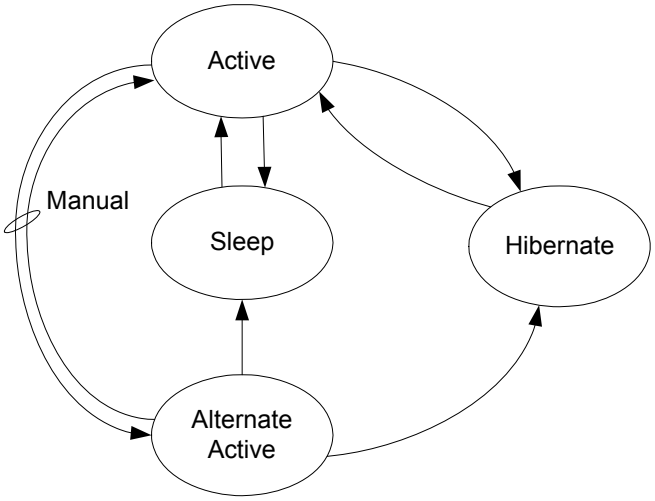
6.1.1.4 Internal Low-Speed Oscillator

The ILO provides clock frequencies for low power consumption, including the sleep timer. The ILO generates up to three different clocks: 1 kHz, 33 kHz, and 100 kHz.

The 1 kHz clock (CLK1K) is typically used for a background 'heartbeat' timer. This clock inherently lends itself to long sleep intervals using the central timewheel (CTW). The central timewheel is a free running counter clocked by the ILO 1 kHz output. The central timewheel is always enabled except in hibernate mode and when the CPU is stopped during debug on chip mode. It can be used to generate periodic interrupts for timing purposes or to wake the system from a low power mode. Firmware can reset the central timewheel.

The central timewheel can be programmed to wake the system periodically and optionally issue an interrupt. This enables flexible, periodic wakeups from low power modes or coarse timing applications. Systems that require accurate timing should use the RTC capability instead of the central timewheel. The 100 kHz clock (CLK100K) works as a low power system clock to run the CPU. It can also generate fast time intervals using the fast timewheel.

Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode powers down the CPU and other internal circuitry to reduce power consumption. However, supervisory services such as the central timewheel (CTW) remain available in this mode. The device can wake up using CTW or system reset. The wake up time from sleep mode is 125 µs (typical).

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external reset (XRES).

6.2.1.5 Wakeup Events

Wakeup events can come from the central timewheel or device reset. A wakeup event restores the system to active mode. The central timewheel allows the system to periodically wake up, poll peripherals, do voltage monitoring, or perform real-time functions. Reset event sources include the external reset pin (XRES).

6.3 Reset

CY8C55 has multiple internal and external reset sources available. The reset sources are:

- Power source monitoring - The analog and digital power voltages, VDDA, VDDD, VCCA, and VCCD are monitored in several different modes during power up and active mode. The monitors are programmable to generate an interrupt to the processor under certain conditions.
- External - The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to VDDIO1. VDDD, VDDA, and VDDIO1 must all have voltage applied before the part comes out of reset.
- Watchdog timer - A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset. The watchdog timer can be used only when the part remains in active mode.
- Software - The device can be reset under program control.

Figure 6-6. Resets

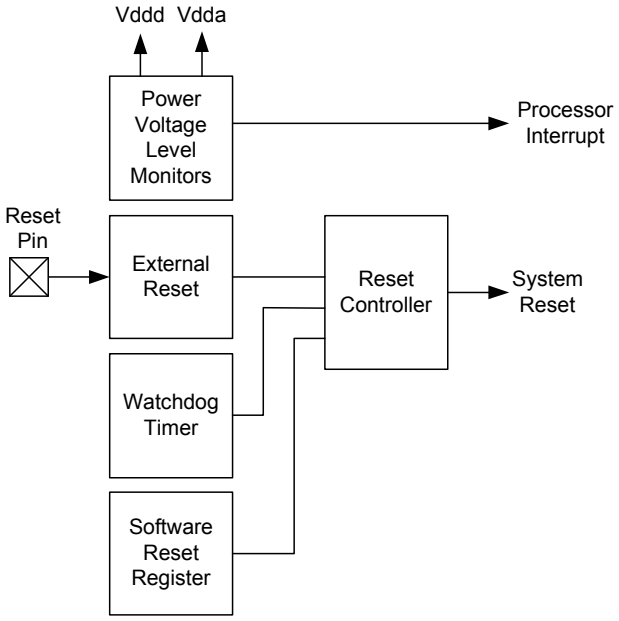
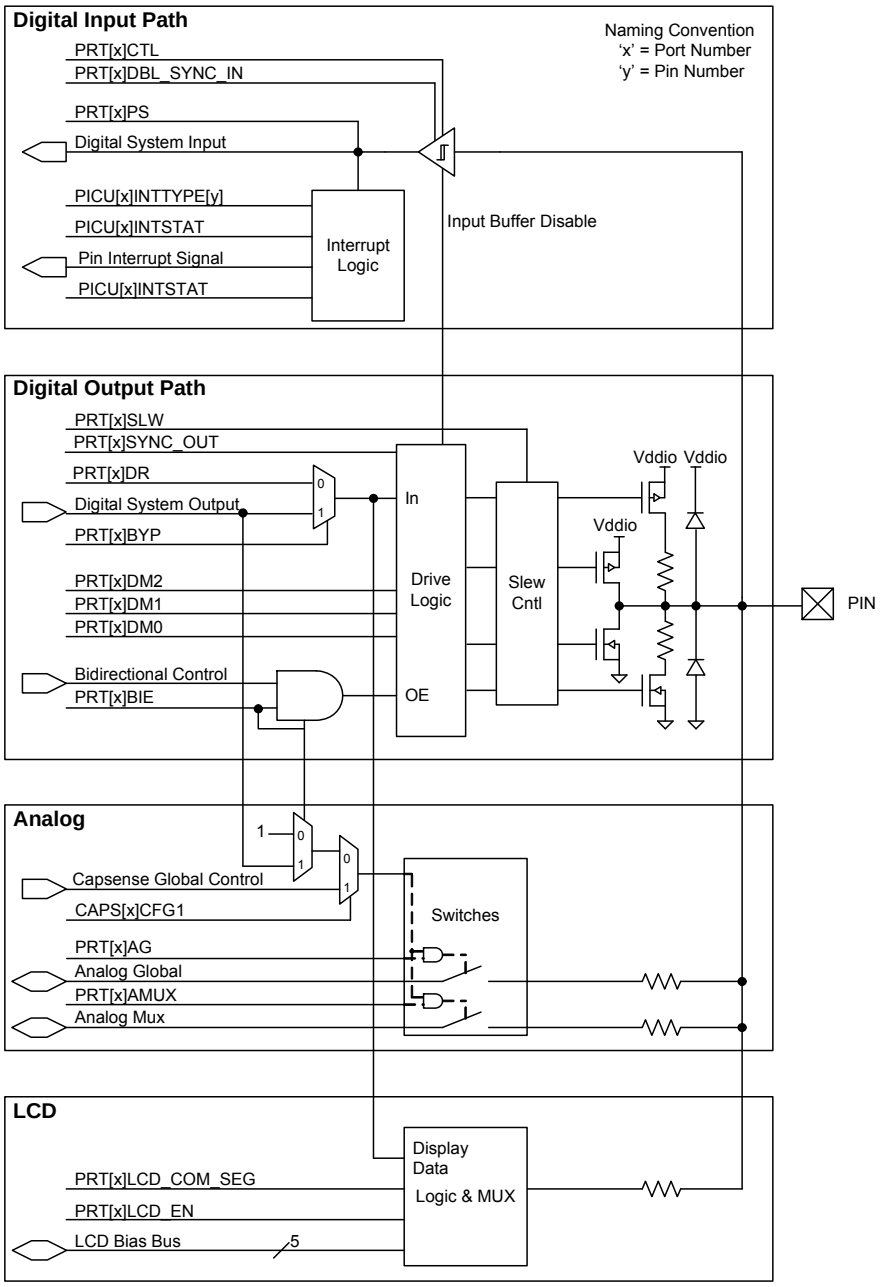


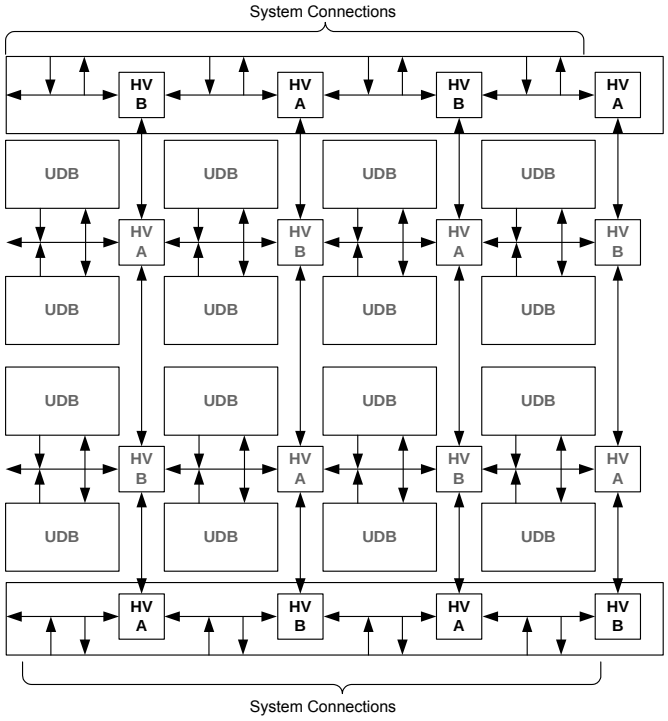
Figure 6-7. GPIO Block Diagram



7.3 UDB Array Description

Figure 7-4 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-4. Digital System Interface Structure

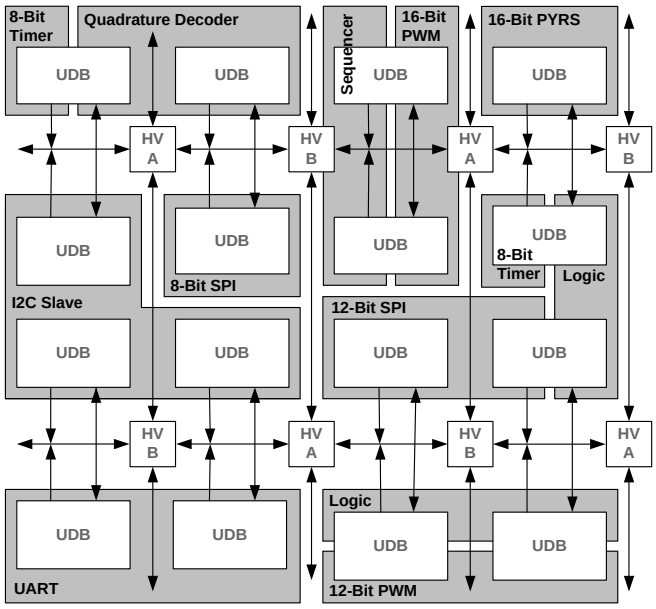


7.3.1 UDB Array Programmable Resources

Figure 7-5 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit Timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-5. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-6 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

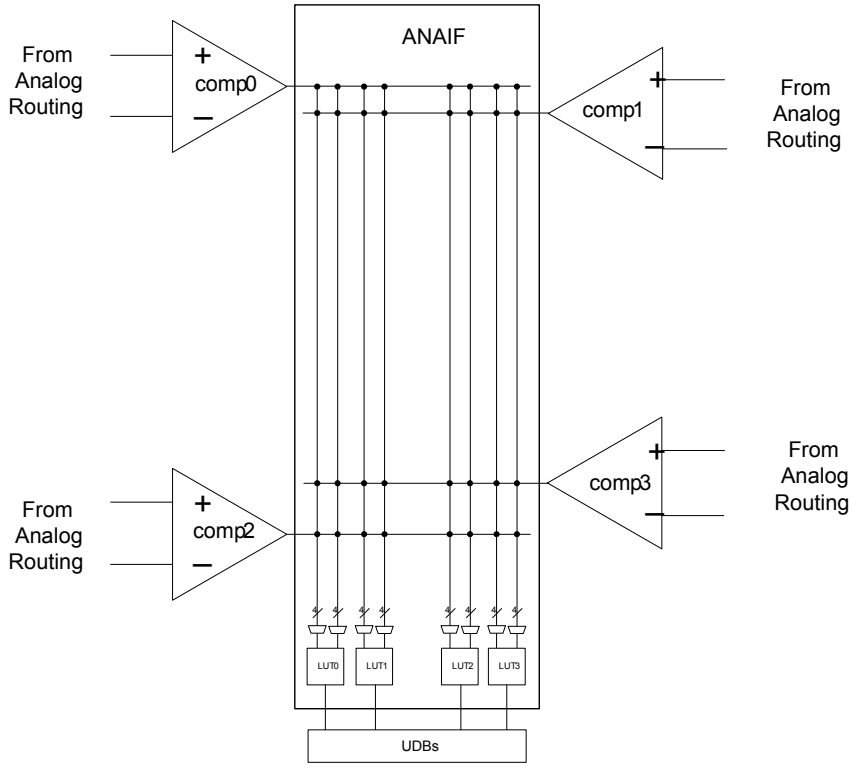
Signals in this category include:

- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

8.4.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB DSI.

Figure 8-6. Analog Comparator



8.4.2 LUT

The CY8C55 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	**FALSE** (‘0’)
0001b	**A** AND **B**
0010b	**A** AND (NOT **B**)
0011b	A
0100b	(NOT **A**) AND **B**
0101b	B
0110b	**A** XOR **B**
0111b	**A** OR **B**
1000b	**A** NOR **B**
1001b	**A** XNOR **B**
1010b	NOT **B**
1011b	**A** OR (NOT **B**)
1100b	NOT **A**
1101b	(NOT **A**) OR **B**
1110b	**A** NAND **B**
1111b	**TRUE** (‘1’)

11. Electrical Specifications

Specifications are valid for -40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component datasheets for full AC/DC specifications of individual functions. See the "Example Peripherals" section on page 31 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_J	Operating die temperature		–55	–	110	°C
T_{STG}	Storage temperature	Recommended storage temperature is +25 °C ±25 °C. Extended duration storage temperatures above 85 °C degrade reliability.	–55	25	100	°C
V_{DDA}	Analog supply voltage relative to V_{SSA}		–0.5	–	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{CCA}	Direct analog core voltage input		–0.5	–	1.95	V
V_{CCD}	Direct digital core voltage input		–0.5	–	1.95	V
V_{SSA}	Analog ground voltage		V_{SSD} – 0.5	–	V_{SSD} + 0.5	V
V_{GPIO}[15]	DC input voltage on GPIO	Includes signals sourced by V_{DDA} and routed internal to the pin.	V_{SSD} – 0.5	–	V_{DDIO} + 0.5	V
V_{SIO}	DC input voltage on SIO	Output disabled	V_{SSD} – 0.5	–	7	V
		Output enabled	V_{SSD} – 0.5	–	6	V
I_{VDDIO}	Current per V_{DDIO} supply pin	Source	–	–	20	mA
		Sink	–	–	100	
Vextref	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current[16]		–100	–	100	mA
ESD_{HBM}	Electrostatic discharge voltage	Human body model	500	–	–	V
ESD_{CDM}	ESD voltage	Charge device model	500	–	–	V

Note Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to maximum conditions for extended periods of time may affect device reliability. When used below maximum conditions but above normal operating conditions the device may not operate to specification.

Notes
15. The V_{DDIO} supply voltage must be greater than the maximum analog voltage on the associated GPIO pins. Maximum analog voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
16. Meets or exceeds JEDEC Spec EIA/JESD78 IC latch up test, at up to 85 °C.

Table 11-3. AC Specifications[22]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU frequency		DC	–	67.01	MHz
F_{BUSCLK}	Bus frequency		DC	–	67.01	MHz
S_{VDD}	V_{DD} ramp rate		–	–	0.066	V/µs
$T_{STARTUP}$	Time from $V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA}$ ≥ min operating voltage to CPU executing code at reset vector	No PLL used, IMO boot mode 12 MHz typ.	–	45	80	µs
T_{SLEEP}	Wakeup from sleep – CTW timeout to beginning of execution of next CPU instruction		–	125	–	µs
T_{SLEEP_INT}	Sleep timer periodic wakeup interval		–	–	128	ms

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		2.7	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor[23]	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 21	–	1	10	µF

Figure 11-2. Regulators V_{CC} vs V_{DD}

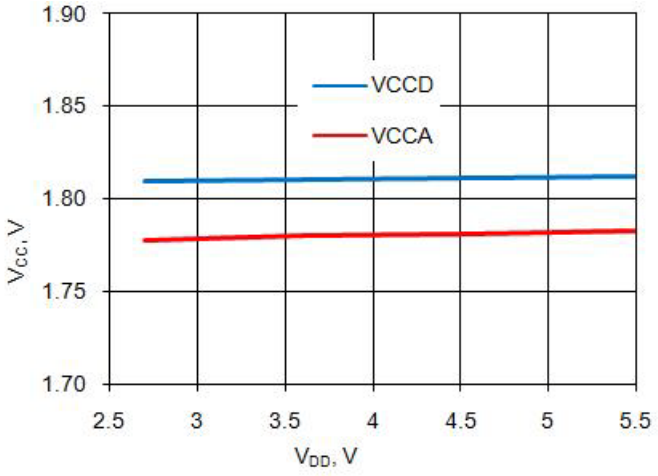
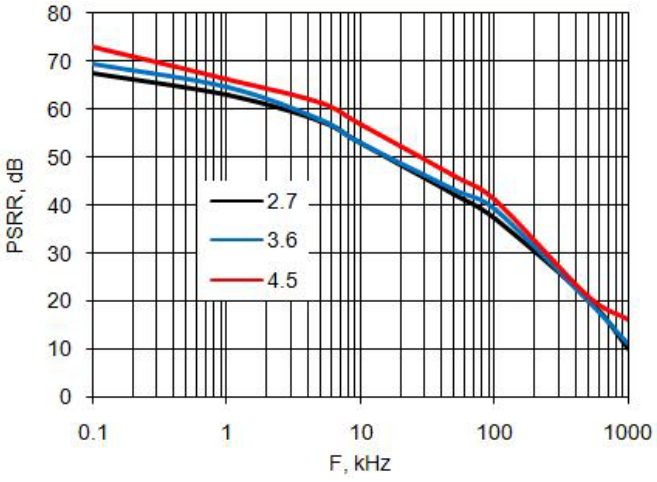


Figure 11-3. Digital Regulator PSRR vs Frequency and V_{DD}



Notes
21. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.
22. Based on device characterization (Not production tested).
23. 10 µF is required for sleep mode. See Table 11-3.

Figure 11-7. GPIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

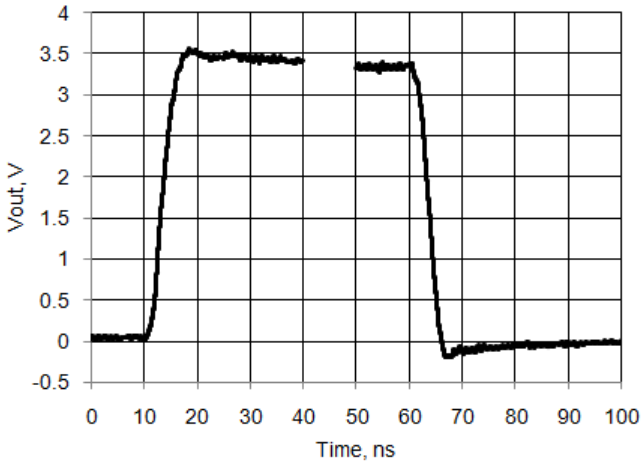
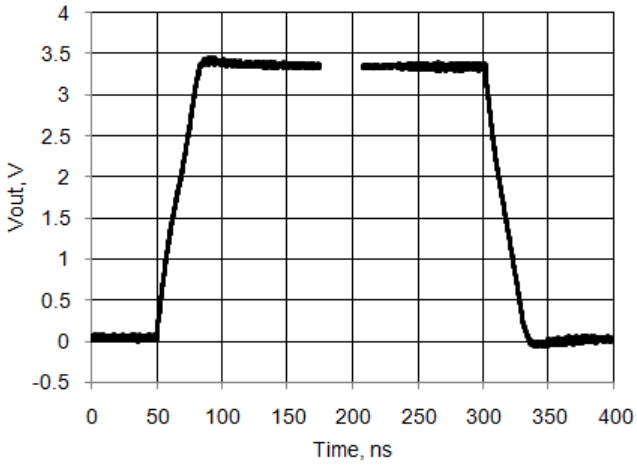


Figure 11-8. GPIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



11.4.2 SIO

Note that under certain conditions an SIO pin may cause up to 1 mA of additional current to be drawn from the related V_{DDIO} pin. If an SIO pin's voltage exceeds its V_{DDIO} supply by 0.5 V, the trigger condition is set. After the trigger condition is set, the SIO pin causes increased current when its voltage is between V_{SSD} + 0.5 V and V_{DDIO} – 0.5 V. The trigger condition is reset when the SIO pin is brought within the range of V_{SSD} to V_{SSD} + 0.5 V. The trigger condition may unknowningly be met during device powerup due to differences in supply ramps.

Table 11-8. SIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vinmax	Maximum input voltage	All allowed values of V_{DDIO} and V_{DDD}, see *Section 11.2.1*	–	–	5.5	V
Vinref	Input voltage reference (differential input mode)		0.5	–	0.52 × V_{DDIO}	V
Voutref	Output voltage reference (regulated output mode)					
		V_{DDIO} > 3.7	1	–	V_{DDIO} – 1	V
		V_{DDIO} < 3.7	1	–	V_{DDIO} – 0.5	V
V_{IH}	Input voltage high threshold					
	GPIO mode	CMOS input	0.7 × V_{DDIO}	–	–	V
	Differential input mode[28]	Hysteresis disabled	SIO_ref + 0.2	–	–	V
V_{IL}	Input voltage low threshold					
	GPIO mode	CMOS input	–	–	0.3 × V_{DDIO}	V
	Differential input mode[28]	Hysteresis disabled	–	–	SIO_ref – 0.2	V
V_{OH}	Output voltage high					
	Unregulated mode	I_{OH} = 4 mA, V_{DDIO} = 3.3 V	V_{DDIO} – 0.4	–	–	V
	Regulated mode[28]	I_{OH} = 1 mA	SIO_ref – 0.65	–	SIO_ref + 0.2	V
	Regulated mode[28]	I_{OH} = 0.1 mA	SIO_ref – 0.3	–	SIO_ref + 0.2	V
V_{OL}	Output voltage low	V_{DDIO} = 3.30 V, I_{OL} = 25 mA	–	–	0.8	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I_{IL}	Input leakage current (absolute value)[29]					
	$V_{IH} \le V_{DDSIO}$	25 °C, V_{DDSIO} = 3.0 V, V_{IH} = 3.0 V	–	–	14	nA
	$V_{IH} > V_{DDSIO}$	25 °C, V_{DDSIO} = 0 V, V_{IH} = 3.0 V	–	–	10	µA

Notes
28. See Figure 6-8 on page 27 and Figure 6-11 on page 30 for more information on SIO reference.
29. Based on device characterization (Not production tested).

11.4.4 XRES

Table 11-13. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold		0.7 × V_{DDIO}	–	–	V
V_{IL}	Input voltage low threshold		–	–	0.3 × V_{DDIO}	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
C_{IN}	Input capacitance[33]		–	3		pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[33]		–	100	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA

Table 11-14. XRES AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESET}	Reset pulse width		1	–	–	µs

11.5 Analog Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted.

11.5.1 Opamp

Table 11-15. Opamp DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_I	Input voltage range		V_{SSA}	–	V_{DDA}	V
V_{OS}	Input offset voltage	Operating temperature > 70 °C	–	–	3	mV
		Operating temperature –40 °C to 70 °C	–	–	2	mV
TCV_{OS}	Input offset voltage drift with temperature		–	–	±30	µV / °C
Ge1	Gain error, unity gain buffer mode	Rload = 1 kΩ	–	–	±0.1	%
C_{IN}	Input capacitance	Routing from pin	–	–	18	pF
Vo	Output voltage range	1 mA, source or sink	V_{SSA} + 0.05	–	V_{DDA} – 0.05	V
I_{OUT}	Output current, source or sink	V_{SSA} + 500 mV ≤ Vout ≤ V_{DDA} –500 mV	10	–	–	mA
I_{DD}	Quiescent current	V_{SSA} + 50 mV < V_{IN} < V_{DDA}-50 mV	–	1	2.5	mA
CMRR	Common mode rejection ratio		80	–	–	dB
PSRR	Power supply rejection ratio		75	–	–	dB

Note
33. Based on device characterization (Not production tested).

11.5.2 Delta-Sigma ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- Fclk = 3.072 MHz for resolution = 16 to 20 bits; Fclk = 6.144 MHz for resolution = 8 to 15 bits
- Reference = 1.024 V internal reference bypassed on P3.2 or P0.3
- Unless otherwise specified, all charts and graphs show typical values

Table 11-17. Delta-sigma ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		8	–	20	bits
	Number of channels, single-ended		–	–	No. of GPIOs	
	Number of channels, differential	Differential pair is formed using a pair of GPIOs	–	–	No. of GPIOs/2	
	Monotonic	Yes	–	–	–	
Ge	Gain error	Level shift buffered, Buffer gain = 1, Differential range ±1.024 V, 25 °C, 16-bit	–0.6	–	0.6	%
		Unbuffered, Differential range ±1.024 V, 25 °C, 16-bit	–0.3	–	0.3	%
Gd	Gain Drift	Level shift buffered, Buffer Gain = 1, Range = ±1.024 V, 16-bit	–	–	60	ppm/°C
		Unbuffered, Range = ±1.024 V, 16-bit	–	–	70	ppm/°C
Vos	Input offset voltage	Level shift buffered, 16-bit mode, V_{DDA} = 2.7 V, 25 °C	–650	–	650	uV
		Unbuffered, 16-bit mode, V_{DDA} = 2.7 V, 25 °C	–200	–	200	uV
TCVos	Temperature coefficient, input offset voltage	Level shift buffered, Buffer Gain = 1, 16-bit, Range = ±1.024 V, V_{DDA} < 3.6 V	–	10	–	uV/°C
		Unbuffered, 16-bit, Range=±1.024 V	–	–	0.45	uV/°C
	Input voltage range[34]	Single-ended, Unbuffered	V_{SSA}	–	V_{DDA}	V
		Differential, Unbuffered	V_{SSA}	–	V_{DDA}	V
		Differential, Level shift buffered	V_{SSA}	–	V_{DDA} – 1	V
PSRRb	Power supply rejection ratio - 16-bit[34]	Level shift buffered, Buffer Gain = 1, Range=±1.024 V, V_{DDA} < 3.6 V	–	80	–	dB
		Unbuffered, Range = ±1.024 V	90	–	–	dB
CMRRb	Common mode rejection ratio, 16-bit[34]	Level shift buffered, Buffer Gain=1, Range=±1.024 V, V_{DDA} < 3.6 V	–	85	–	dB
		Unbuffered, Range = ±1.024 V	85	–	–	dB
INL20	INL for 20-bit[35]	Differential range ±1.024 V	–	–	32	LSB
DNL20	DNL for 20-bit[35]	Differential range ±1.024 V	–	–	1	LSB
INL16	Integral non linearity - 16-bit[35]	Differential range ±1.024 V	–	–	2	LSB

Note
34. Based on device characterization (not production tested).

Table 11-17. Delta-sigma ADC DC Specifications (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
DNL16	Differential non linearity - 16-bit[35]	Differential range ±1.024 V	–	–	1	LSB
INL12	INL for 12-bit[35]	Differential range ±1.024 V	–	–	1	LSB
DNL12	DNL for 12-bit[35]	Differential range ±1.024 V	–	–	1	LSB
INL8	INL for 8-bit[35]	Differential range ±1.024 V	–	–	1	LSB
DNL8	DNL for 8-bit[35]	Differential range ±1.024 V	–	–	1	LSB
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	MΩ
Rin_ADC_16	ADC input resistance	Input buffer bypassed, 16-bit, Range = ±1.024 V	–	74[36]	–	kΩ
Rin_ADC_12	ADC input resistance	Input buffer bypassed, 12-bit, Range = ±1.024 V	–	148[36]	–	kΩ
Vextref	ADC external reference input voltage, see also internal reference in Voltage Reference on page 75	Pins P0[3], P3[2]	0.9	–	1.3	V
Current consumption						
IDD_20	Current consumption, 20-bit, 187 sps[35]	Unbuffered	–	–	4	mA
IDD_16	Current consumption, 16-bit, 48 ksps[35]	Unbuffered	–	–	4	mA
IDD_12	Current consumption, 12-bit, 192 ksps[35]	Unbuffered	–	–	4.5	mA
IDD_8	Current consumption, 8-bit, 384 ksps[35]	Unbuffered	–	–	4.5	mA
IBUFF	Current consumption, 16-bit, 48 ksps[35]	Buffer alone	–	–	3.5	mA

Figure 11-24. Delta-Sigma ADC DNL vs Output Code, 16-bit, 48 ksps, 25 °C, V_{DDA} = 3.3 V

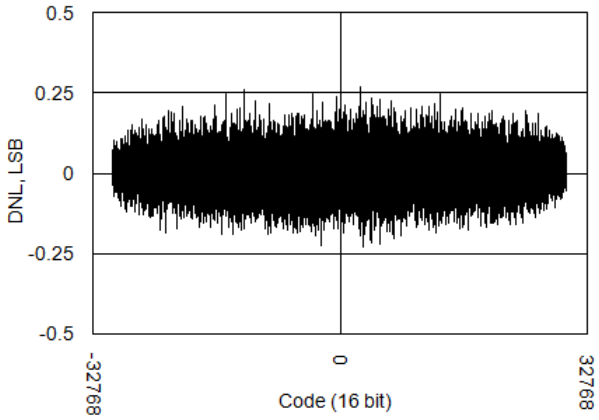
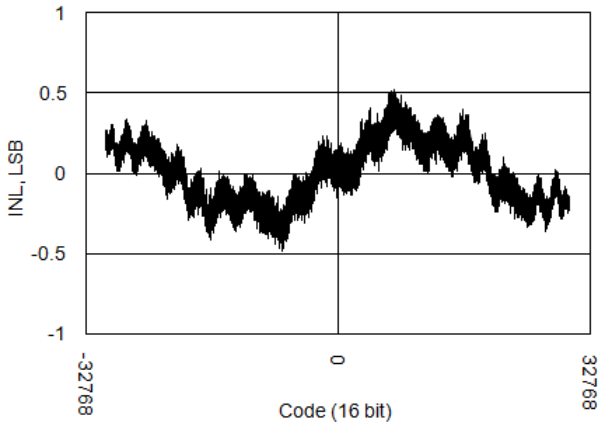


Figure 11-25. Delta-Sigma ADC INL vs Output Code, 16-bit, 48 ksps, 25 °C, V_{DDA} = 3.3 V



Notes
35. Based on device characterization (not production tested).
36. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.

Table 11-31. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	5.5	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, fast mode, 600 Ω 15-pF load	–	–	180	ns
	Current noise	Range = 255 µA, source mode, fast mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-42. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V

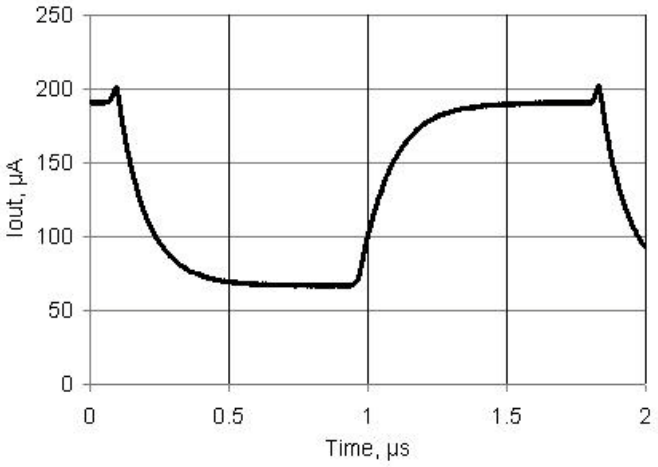


Figure 11-43. IDAC PSRR vs Frequency

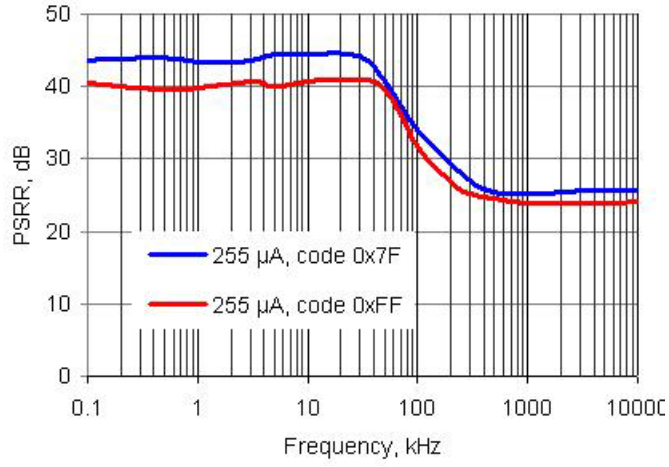


Figure 11-44. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V

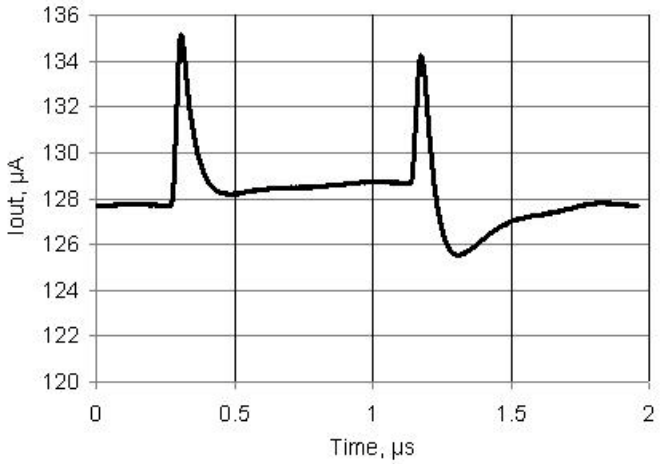
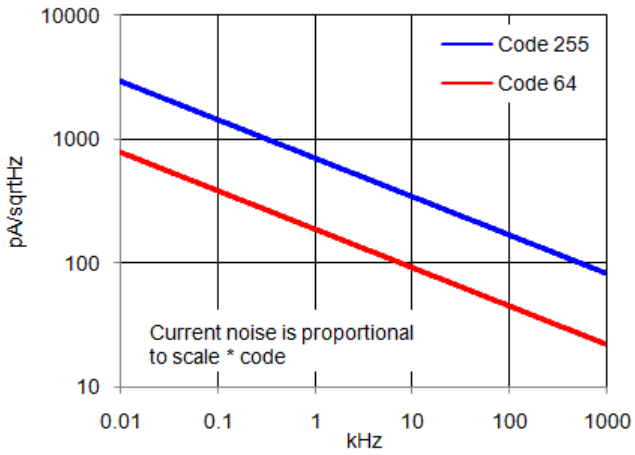


Figure 11-45. IDAC Current Noise, 255 µA Mode, Source Mode, Fast Mode, V_{DDA} = 5 V



11.5.9 Mixer

The mixer is created using a SC/CT analog block; see the Mixer component data sheet in PSoC Creator for full electrical specifications and APIs.

Table 11-34. Mixer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage		–	–	26	mV
	Quiescent current		–	0.9	2	mA
G	Gain		–	0	–	dB

Table 11-35. Mixer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
f_{LO}	Local oscillator frequency	Down mixer mode	–	–	4	MHz
f_{in}	Input signal frequency	Down mixer mode	–	–	14	MHz
f_{LO}	Local oscillator frequency	Up mixer mode	–	–	1	MHz
f_{in}	Input signal frequency	Up mixer mode	–	–	1	MHz
SR	Slew rate		3	–	–	V/µs

11.5.10 Transimpedance Amplifier

The TIA is created using a SC/CT analog block; see the TIA component data sheet in PSoC Creator for full electrical specifications and APIs.

Table 11-36. Transimpedance Amplifier (TIA) DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IOFF}	Input offset voltage		–	–	20	mV
Rconv	Conversion resistance[41]	R = 20K; 40 pF load	–25	–	+35	%
		R = 30K; 40 pF load	–25	–	+35	%
		R = 40K; 40 pF load	–25	–	+35	%
		R = 80K; 40 pF load	–25	–	+35	%
		R = 120K; 40 pF load	–25	–	+35	%
		R = 250K; 40 pF load	–25	–	+35	%
		R= 500K; 40 pF load	–25	–	+35	%
		R = 1M; 40 pF load	–25	–	+35	%
	Quiescent current		–	1.1	2	mA

Table 11-37. Transimpedance Amplifier (TIA) AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW	Input bandwidth (–3 dB)	R = 20K; 40 pF load	1000	–	–	kHz
		R = 120K; 40 pF load	230	–	–	kHz
		R = 1M; 40 pF load	23	–	–	kHz

Note
41. Conversion resistance values are not calibrated. Calibrated values and details about calibration are provided in PSoC Creator component datasheets. External precision resistors can also be used.

11.5.11 Programmable Gain Amplifier

The PGA is created using a SC/CT analog block; see the PGA component data sheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, operating conditions are:

- Operating temperature = 25 °C for typical values
- Unless otherwise specified, all charts and graphs show typical values

Table 11-38. PGA DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Vin	Input voltage range	Power mode = minimum	V_{SSA}	–	V_{DDA}	V
Vos	Input offset voltage	Power mode = high, gain = 1	–	–	20	mV
TCVos	Input offset voltage drift with temperature	Power mode = high, gain = 1	–	–	±30	µV/°C
Ge1	Gain error, gain = 1		–	–	±2	%
Ge16	Gain error, gain = 16		–	–	±8	%
Ge50	Gain error, gain = 50		–	–	±10	%
Vonl	DC output nonlinearity	Gain = 1	–	–	±0.1	% of FSR
Cin	Input capacitance		–	–	7	pF
Voh	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	V_{DDA} – 0.15	–	–	V
Vol	Output voltage swing	Power mode = high, gain = 1, Rload = 100 kΩ to V_{DDA} / 2	–	–	V_{SSA} + 0.15	V
Vsrc	Output voltage under load	Iload = 250 µA, power mode = high	–	–	300	mV
Idd	Operating current	Power mode = high	–	1.5	1.65	mA
PSRR	Power supply rejection ratio		48	–	–	dB

Table 11-39. PGA AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
BW1	–3 dB bandwidth	Power mode = high, gain = 1, noninverting mode, 300 mV ≤ VIN ≤ V_{DDA} – 1.2 V, CI ≤ 25 pF	6	8	–	MHz
SR1	Slew rate	Power mode = high, gain = 1, 20% to 80%	3	–	–	V/µs
e_n	Input noise density	Power mode = high, V_{DDA} = 5 V, at 100 kHz	–	43	–	nV/sqrtHz

11.9 Clocking

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 2.7 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

11.9.1 kHz External Crystal Oscillator (kHzECO)

For more information on crystal selection for the kHzECO, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators.

Table 11-66. kHz ECO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Oscillator operating current	Low power mode; CL = 6 pF	–	0.25	–	µA
C_{IN}	Capacitance at Pins kHz-XTAL:Xi and kHz-XTAL:Xo[48]		–	5	7	pF

Table 11-67. kHz ECO Crystal Specifications

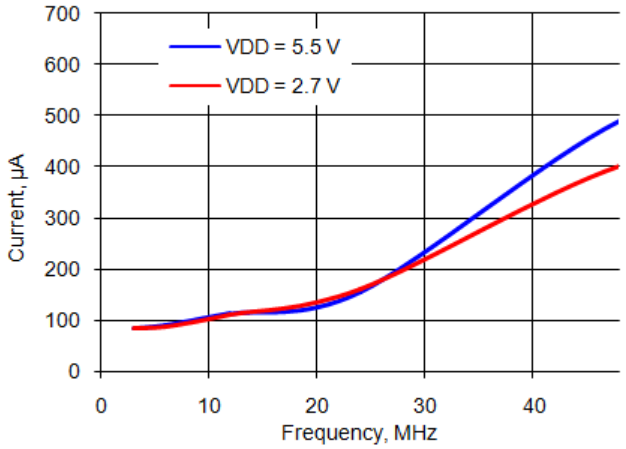
Parameter	Description	Conditions	Min	Typ	Max	Units
F	Crystal frequency		–	32.768	–	kHz
C_L	Crystal load capacitance	Recommended values	–	6 or 12.5	–	pF
D_L	Crystal drive level tolerance		1	–	–	µW

11.9.2 Internal Main Oscillator

Table 11-68. IMO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	48 MHz		–	465	850	µA
	24 MHz		–	195	500	µA
	12 MHz		–	150	450	µA
	6 MHz		–	120	400	µA
	3 MHz		–	105	300	µA

Figure 11-62. IMO Current vs. Frequency



Note
48. Based on device characterization (Not production tested).

16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibels
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohours
kHz	kilohertz
kΩ	kilohms
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	megaohms
Msps	megasamples per second
µA	microamperes
µF	microfarads
µH	microhenrys
µs	microseconds
µV	microvolts
µW	microwatts
mA	milliamperes
ms	milliseconds
mV	millivolts
nA	nanoamperes
ns	nanoseconds
nV	nanovolts
Ω	ohms
pF	picofarads
ppm	parts per million
ps	picoseconds
s	seconds
sps	samples per second
sqrtHz	square root of hertz
V	volts