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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f042c4u6

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F042x4/x6 microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website *www.st.com*.

For information on the ARM® Cortex®-M0 core, please refer to the Cortex®-M0 Technical Reference Manual, available from the www.arm.com website.

2 Description

The STM32F042x4/x6 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash memory and 6 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one I^2C, two SPIs/one I^2S, one HDMI CEC and two USARTs), one USB Full-speed device (crystal-less), one CAN, one 12-bit ADC, four 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F042x4/x6 microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F042x4/x6 microcontrollers include devices in seven different packages ranging from 20 pins to 48 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F042x4/x6 microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = V_{DDIO1} = 2.0 to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- V_{DDIO2} = 1.65 to 3.6 V: external power supply for marked I/Os. V_{DDIO2} is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}, but it must not be provided without a valid supply on V_{DD}. The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt. Refer to the pinout diagrams or tables for concerned I/Os list.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 13: Power supply scheme*.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD}

4 Pinouts and pin descriptions

Figure 3. LQFP48 package pinout

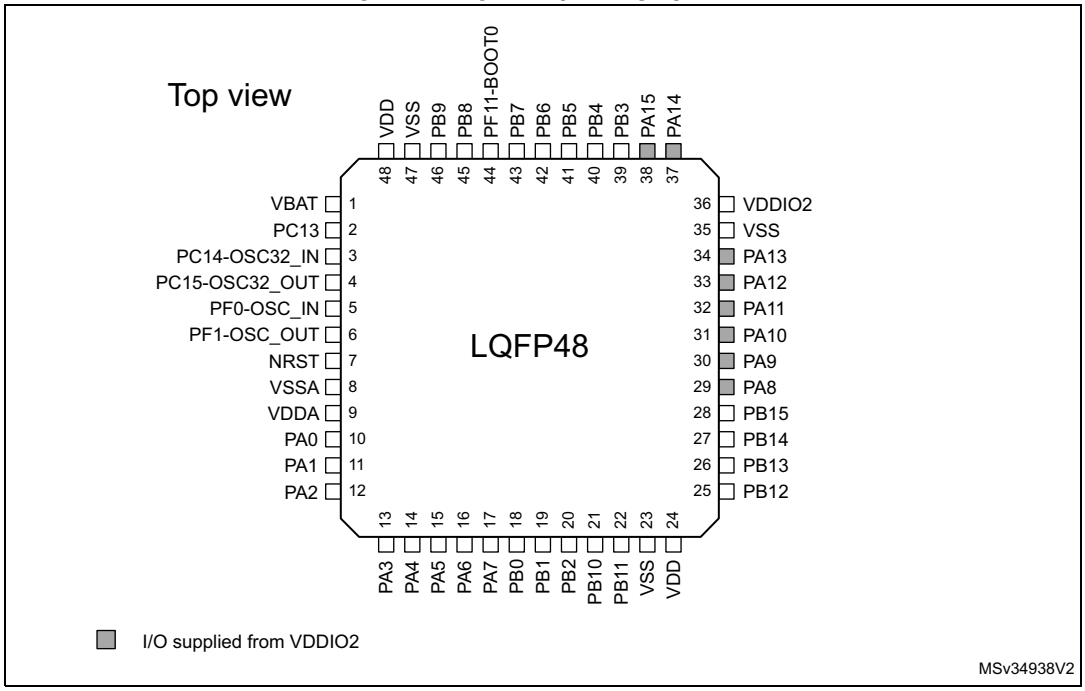


Figure 4. UFQFPN48 package pinout

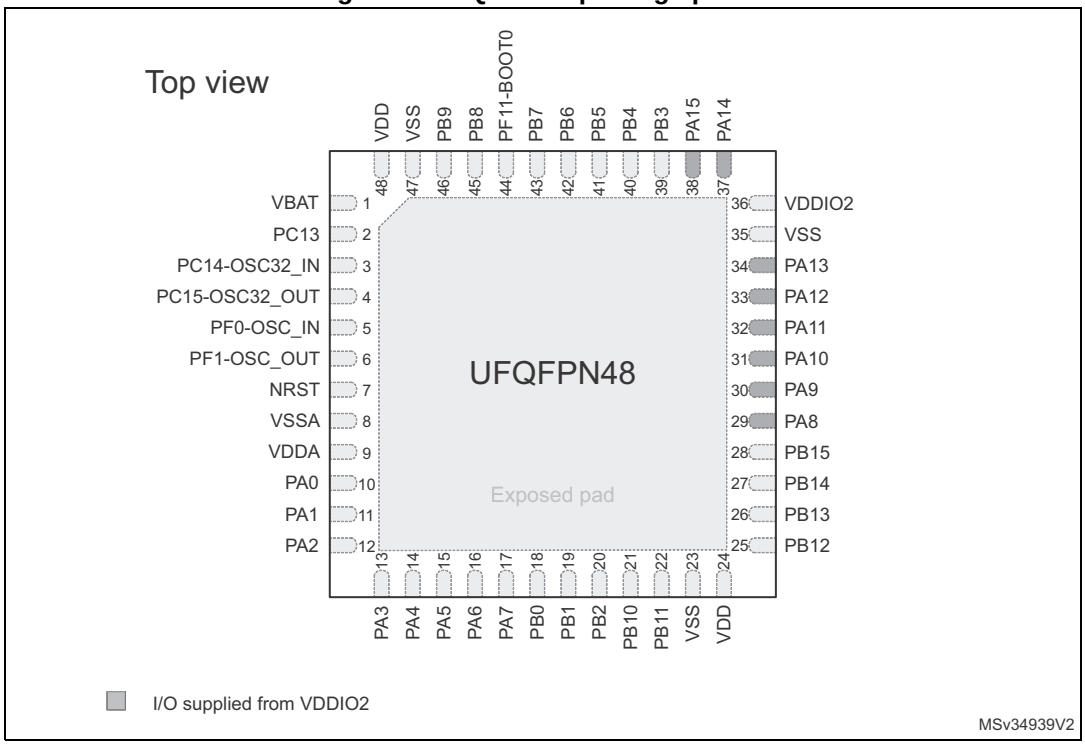


Table 13. STM32F042x pin definitions

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
1	-	-	-	-	-	VBAT	S	-	-	Backup power supply	
2	A6	-	-	-	-	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
3	B6	-	-	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1) (2)	-	OSC32_IN
4	C6	-	-	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1) (2)	-	OSC32_OUT
5	B5	2	2	2	2	PF0-OSC_IN (PF0)	I/O	FTf	-	CRS_ SYNC I2C1_SDA	OSC_IN
6	C5	3	3	3	3	PF1-OSC_OUT (PF1)	I/O	FTf	-	I2C1_SCL	OSC_OUT
7	D5	4	4	4	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	D6	32	0	16	15	VSSA	S		(3)	Analog ground	
9	E5	5	5	5	5	VDDA	S		-	Analog power supply	
10	F6	6	6	6	6	PA0	I/O	TTa	-	USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1	RTC_ TAMP2, WKUP1, ADC_IN0,
11	D4	7	7	7	7	PA1	I/O	TTa	-	USART2_RTS, TIM2_CH2, TSC_G1_IO2, EVENTOUT	ADC_IN1
12	E4	8	8	8	8	PA2	I/O	TTa	-	USART2_TX, TIM2_CH3, TSC_G1_IO3	ADC_IN2, WKUP4
13	F5	9	9	9	9	PA3	I/O	TTa	-	USART2_RX, TIM2_CH4, TSC_G1_IO4	ADC_IN3

Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
26	-	-	-	-	-	PB13	I/O	FTf	-	SPI2_SCK, TIM1_CH1N, I2C1_SCL	-
27	-	-	-	-	-	PB14	I/O	FTf	-	SPI2_MISO, TIM1_CH2N, I2C1_SDA	-
28	-	-	-	-	-	PB15	I/O	FT	-	SPI2_MOSI, TIM1_CH3N	WKUP7, RTC_REFIN
29	E2	18	18	-	-	PA8	I/O	FT	(4)	USART1_CK, TIM1_CH1, EVENTOUT, MCO, CRS_SYNC	-
30	D1	19	19	19	17	PA9	I/O	FTf	(4)	USART1_TX, TIM1_CH2, TSC_G4_IO1, I2C1_SCL	-
31	C1	20	20	20	18	PA10	I/O	FTf	(4)	USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2, I2C1_SDA	-
32	C2	21	21	19(5)	17(5)	PA11	I/O	FTf	(4)	CAN_RX, USART1_CTS, TIM1_CH4, TSC_G4_IO3, EVENTOUT, I2C1_SCL	USB_DM
33	A1	22	22	20(5)	18(5)	PA12	I/O	FTf	(4)	CAN_TX,USART1_RTS, TIM1_ETR, TSC_G4_IO4, EVENTOUT, I2C1_SDA	USB_DP
34	B1	23	23	21	19	PA13	I/O	FT	(4) (6)	IR_OUT, SWDIO USB_NOE	-
35	-	-	-	-	-	VSS	S	-	-	Ground	
36	E1	17	17	18	16	VDDIO2	S	-	-	Digital power supply	
37	B2	24	24	22	20	PA14	I/O	FT	(4) (6)	USART2_TX, SWCLK	-

Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
38	A2	25	25	23	-	PA15	I/O	FT	(4)	SPI1_NSS, I2S1_WS, USART2_RX, TIM2_CH1_ETR, EVENTOUT, USB_NOE	-
39	B3	26	26	24	-	PB3	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	-
40	A3	27	27	25	-	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
41	E6	28	28	26	-	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6
42	C4	29	29	27	-	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_I03	-
43	A4	30	30	28	-	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4	-
44	-	-	31	-	-	PF11-BOOT0	I/O	FT	-	-	Boot memory selection
-	B4	31	-	1	1	PB8-BOOT0	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	Boot memory selection
45	-	-	32	-	-	PB8	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	-

Table 15. Alternate functions selected through GPIOB_AFR registers for port B

Pin name	AF0	AF1	AF2	AF3	AF4	AF5
PB0	EVENTOUT	TIM3_CH3	TIM1_CH2N	TSC_G3_IO2	-	-
PB1	TIM14_CH1	TIM3_CH4	TIM1_CH3N	TSC_G3_IO3	-	-
PB2	-	-	-	TSC_G3_IO4	-	-
PB3	SPI1_SCK, I2S1_CK	EVENTOUT	TIM2_CH2	TSC_G5_IO1	-	-
PB4	SPI1_MISO, I2S1_MCK	TIM3_CH1	EVENTOUT	TSC_G5_IO2	-	TIM17_BKIN
PB5	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM16_BKIN	I2C1_SMBA	-	-
PB6	USART1_TX	I2C1_SCL	TIM16_CH1N	TSC_G5_IO3	-	-
PB7	USART1_RX	I2C1_SDA	TIM17_CH1N	TSC_G5_IO4	-	-
PB8	CEC	I2C1_SCL	TIM16_CH1	TSC_SYNC	CAN_RX	-
PB9	IR_OUT	I2C1_SDA	TIM17_CH1	EVENTOUT	CAN_TX	SPI2_NSS
PB10	CEC	I2C1_SCL	TIM2_CH3	TSC_SYNC	-	SPI2_SCK
PB11	EVENTOUT	I2C1_SDA	TIM2_CH4	-	-	-
PB12	SPI2_NSS	EVENTOUT	TIM1_BKIN	-	-	-
PB13	SPI2_SCK	-	TIM1_CH1N	-	-	I2C1_SCL
PB14	SPI2_MISO	-	TIM1_CH2N	-	-	I2C1_SDA
PB15	SPI2_MOSI	-	TIM1_CH3N	-	-	-

Table 16. Alternate functions selected through GPIOF_AFR registers for port F

Pin name	AF0	AF1
PF0	CRS_SYNC	I2C1_SDA
PF1	-	I2C1_SCL

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

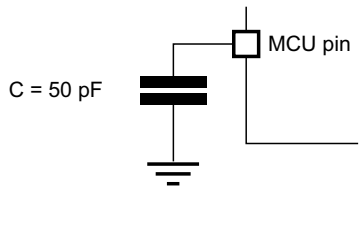


Figure 12. Pin input voltage

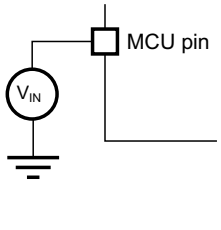


Table 24. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$I_{DD(PVD)}$	PVD current consumption	-	-	0.15	0.26(1)	µA

1. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 25. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10(1)	µs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4(1)	-	-	µs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V	-	-	10(1)	mV
T_{Coeff}	Temperature coefficient	-	- 100(1)	-	100(1)	ppm/°C

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 27. Typical and maximum current consumption from the V_{DDA} supply

Symbol	Para-meter	Conditions (1)	f_{HCLK}	V_{DDA} = 2.4 V				V_{DDA} = 3.6 V				Unit
				Typ	Max @ T_A (2)			Typ	Max @ T_A (2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DDA}	Supply current in Run or Sleep mode, code executing from Flash memory or RAM	HSI48	48 MHz	309	325	332	342	317	334	338	344	µA
		HSE bypass, PLL on	48 MHz	148	167(3)	176	179(3)	161	181(3)	193	197(3)	
			32 MHz	102	119	124	126	111	128	135	137	
			24 MHz	80	95	99	100	88	102	106	108	
		HSE bypass, PLL off	8 MHz	2.7	3.7	4.2	4.5	3.5	4.7	5.2	5.5	
			1 MHz	2.7	3.7	4.2	4.2	3.6	4.7	5.2	5.5	
		HSI clock, PLL on	48 MHz	220	242	251	254	242	264	275	279	
			32 MHz	173	193	200	202	191	211	219	221	
			24 MHz	151	169	175	177	167	184	191	193	
		HSI clock, PLL off	8 MHz	72	82	85	85	82	92	95	95	

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash memory or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 30. Typical current consumption, code executing from Flash memory, running from HSE 8 MHz crystal

Symbol	Parameter	f_{HCLK}	Typical consumption in Run mode		Typical consumption in Sleep mode		Unit
			Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	
I_{DD}	Current consumption from V_{DD} supply	48 MHz	20.7	12.8	12.3	3.4	mA
		36 MHz	15.9	9.9	9.5	2.7	
		32 MHz	14.3	9.0	8.5	2.5	
		24 MHz	11.0	7.1	6.6	2.1	
		16 MHz	7.7	5.0	4.7	1.6	
		8 MHz	4.3	3.0	2.7	1.2	
		4 MHz	2.6	2.0	1.7	0.9	
		2 MHz	1.8	1.5	1.2	0.8	
		1 MHz	1.4	1.2	1.0	0.8	
		500 kHz	1.2	1.1	0.8	0.7	
I_{DDA}	Current consumption from V_{DDA} supply	48 MHz	163.3				µA
		36 MHz	124.3				
		32 MHz	111.9				
		24 MHz	87.1				
		16 MHz	62.5				
		8 MHz	2.5				
		4 MHz	2.5				
		2 MHz	2.5				
		1 MHz	2.5				
		500 kHz	2.5				

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 50: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt

Table 32. Peripheral current consumption (continued)

Peripheral		Typical consumption at 25 °C	Unit
APB	APB-Bridge(2)	2.9	µA/MHz
	ADC(3)	3.9	
	CAN	12.9	
	CEC	1.5	
	CRS	1.0	
	DBG (MCU Debug Support)	0.2	
	I2C1	3.6	
	PWR	1.4	
	SPI1	8.5	
	SPI2	6.1	
	SYSCFG	1.8	
	TIM1	15.1	
	TIM2	16.8	
	TIM3	11.7	
	TIM14	5.5	
	TIM16	7.0	
	TIM17	6.9	
	USART1	17.8	
	USART2	5.6	
	USB	4.9	
	WWDG	1.4	
	All APB peripherals	**136.7**	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The APB Bridge is automatically active when at least one peripheral is ON on the Bus.
3. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC is not included. Refer to the tables of characteristics in the subsequent sections.

6.3.6 Wakeup time from low-power mode

The wakeup times given in *Table 33* are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop or Standby mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode. The wakeup source from Standby mode is the WKUP1 pin (PA0).

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*..

Table 33. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @V_{DD} = V_{DDA}					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t_{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	3.2	3.1	2.9	2.9	2.8	5	µs
		Regulator in low power mode	7.0	5.8	5.2	4.9	4.6	9	
$t_{WUSTANDBY}$	Wakeup from Standby mode	-	60.4	55.6	53.5	52	51	-	
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	4 SYSCLK cycles					-	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

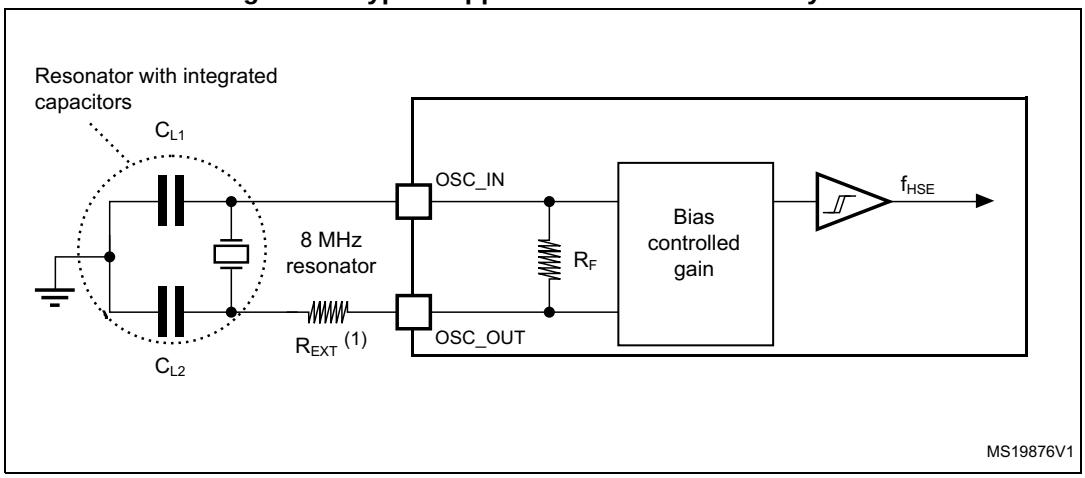
In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

The external clock signal has to respect the I/O characteristics in *Section 6.3.14*. However, the recommended clock input waveform is shown in *Figure 15: High-speed external clock source AC timing diagram*.

Table 34. High-speed external user clock characteristics

Symbol	Parameter(1)	Min	Typ	Max	Unit
f_{HSE_ext}	User external clock source frequency	-	8	32	MHz
V_{HSEH}	OSC_IN input pin high level voltage	0.7 V_{DDIOx}	-	V_{DDIOx}	V
V_{HSEL}	OSC_IN input pin low level voltage	V_{SS}	-	0.3 V_{DDIOx}	
$t_{w(HSEH)}$ $t_{w(HSEL)}$	OSC_IN high or low time	15	-	-	ns
$t_{r(HSE)}$ $t_{f(HSE)}$	OSC_IN rise or fall time	-	-	20	

Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

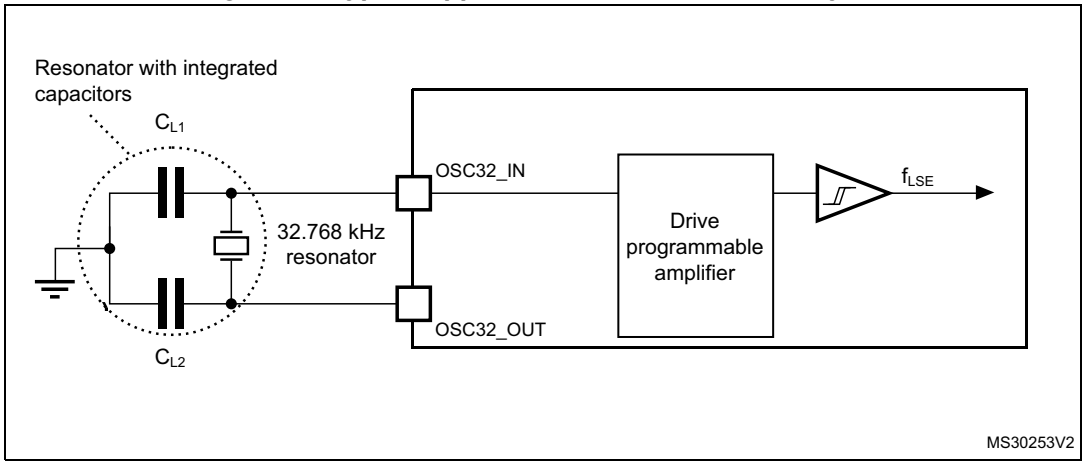
Table 37. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	low drive capability	-	0.5	0.9	µA
		medium-low drive capability	-	-	1	
		medium-high drive capability	-	-	1.3	
		high drive capability	-	-	1.6	
g_m	Oscillator transconductance	low drive capability	5	-	-	µA/V
		medium-low drive capability	8	-	-	
		medium-high drive capability	15	-	-	
		high drive capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DDIOx} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in *Table 38* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*. The provided curves are characterization results, not tested in production.

High-speed internal (HSI) RC oscillator

Table 38. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator	T_A = -40 to 105°C	-2.8(3)	-	3.8(3)	%
		T_A = -10 to 85°C	-1.9(3)	-	2.3(3)	
		T_A = 0 to 85°C	-1.9(3)	-	2(3)	
		T_A = 0 to 70°C	-1.3(3)	-	2(3)	
		T_A = 0 to 55°C	-1(3)	-	2(3)	
		T_A = 25°C(4)	-1	-	1	
$t_{su(HSI)}$	HSI oscillator startup time	-	1(2)	-	2(2)	µs
$I_{DDA(HSI)}$	HSI oscillator power consumption	-	-	80	100(2)	µA

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 19. HSI oscillator accuracy characterization results for soldered parts

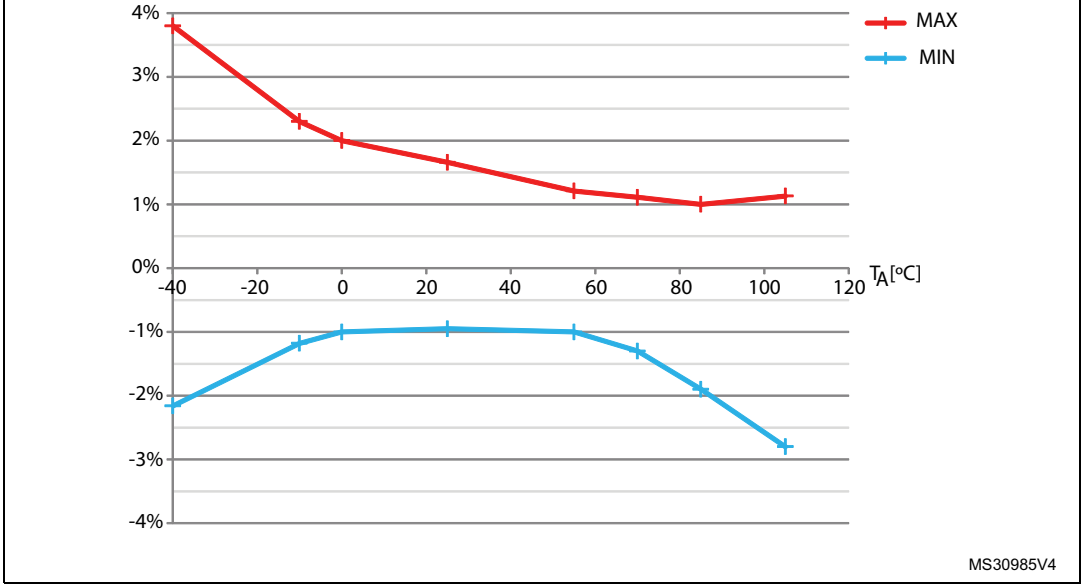


Figure 22. TC and TTa I/O input characteristics

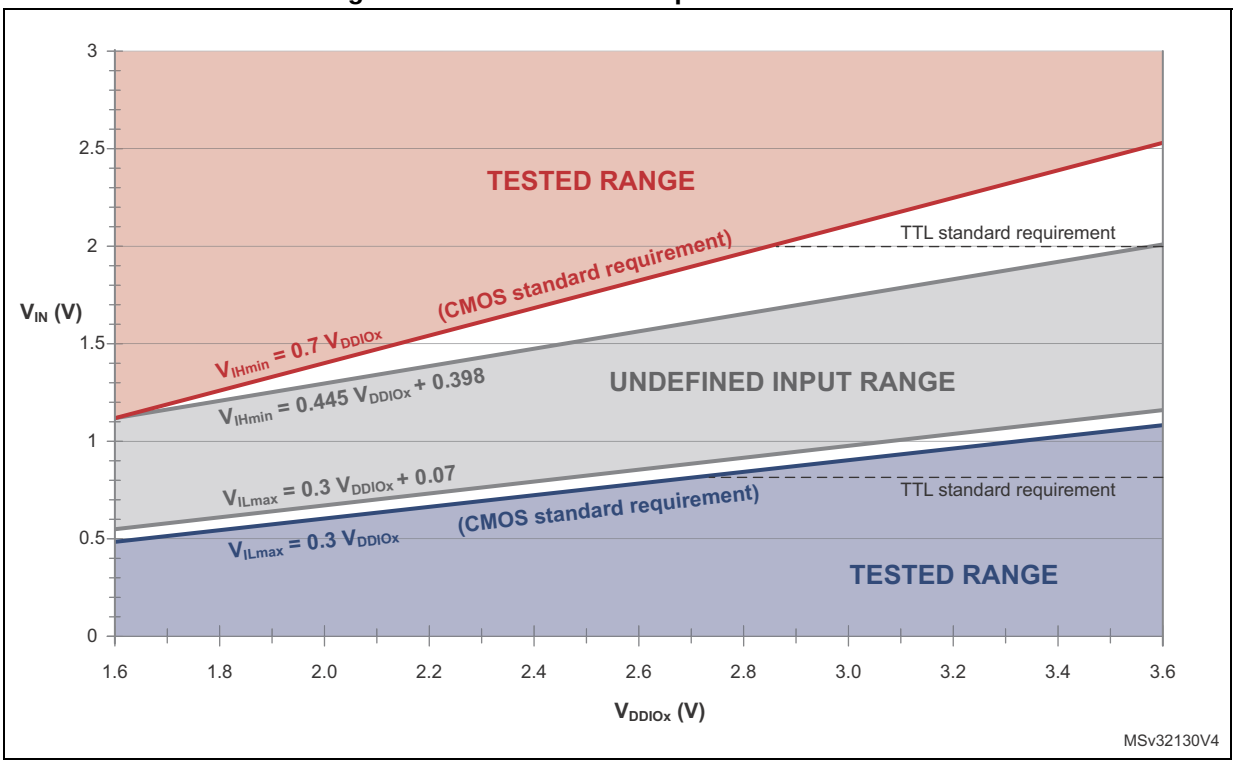


Figure 23. Five volt tolerant (FT and FTf) I/O input characteristics

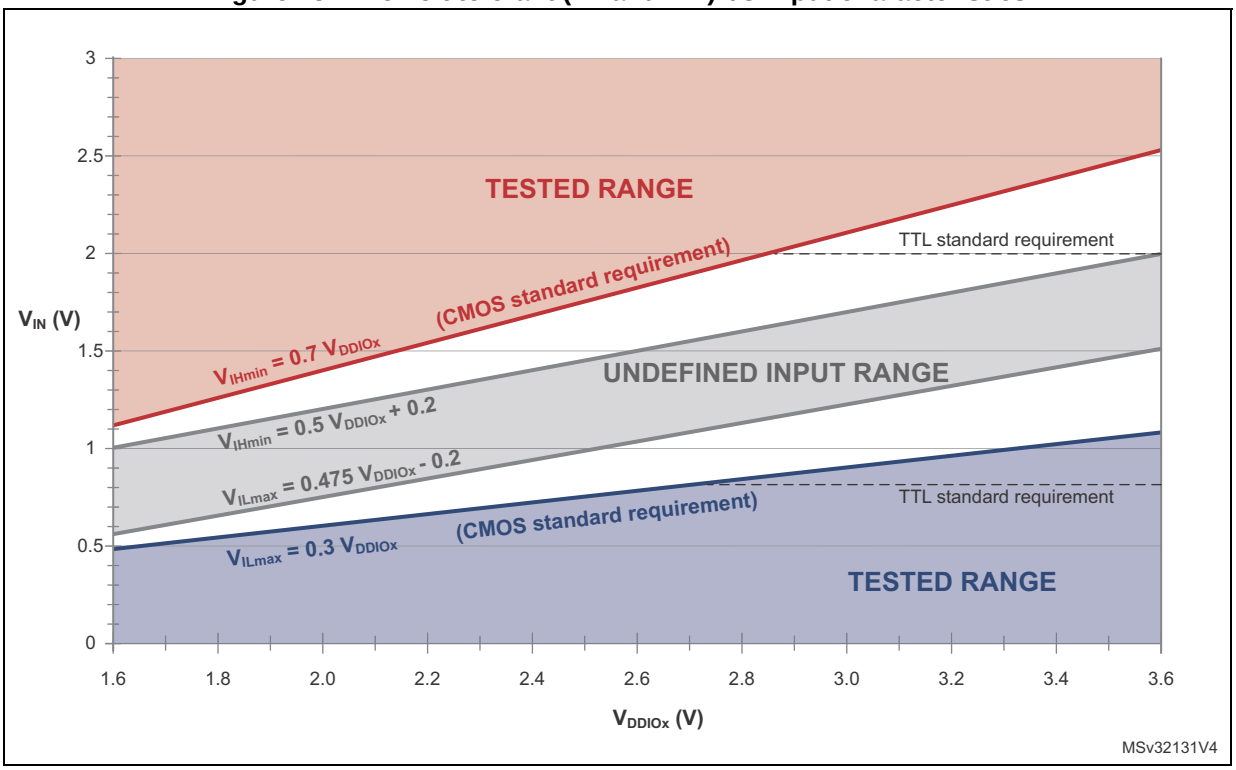


Table 76. Document revision history (continued)

Date	Revision	Changes
16-Dec-2015	4	***Section 3: Functional overview***: – *Figure 2: Clock tree* modified ***Section 4: Pinouts and pin descriptions***: – Package pinout figures updated (look and feel) – *Figure 5: WLCSP36 package pinout*- **now presented in top view** – *Table 13: STM32F042x pin definitions* - note 3 added; CIMP1_OUT and USART4_CTS removed – *Table 15: Alternate functions selected through GPIOB_AFR registers for port B* - change of I2C2_SDA and I2C2_SCL to I2C1_SDA and I2C1_SCL ***Section 5: Memory mapping***: – *Table 17: STM32F042x4/x6 peripheral register boundary addresses* - change of “SYSCFG + COMP” to “SYSCFG” ***Section 6: Electrical characteristics***: – *Table 50: I/O static characteristics*- removed note – *Section 6.3.16: 12-bit ADC characteristics* - changed introductory sentence ***Section 7: Package information***: – *Figure 49: Recommended footprint for UFQFPN28 package* distance between corner pads added
10-Jan-2017	5	***Section 6: Electrical characteristics***: – *Table 37: LSE oscillator characteristics (fLSE = 32.768 kHz)* - information on configuring different drive capabilities removed. See the corresponding reference manual. – *Table 25: Embedded internal reference voltage* - V_{REFINT} values – *Figure 28: SPI timing diagram - slave mode and CPHA = 0* and *Figure 29: SPI timing diagram - slave mode and CPHA = 1* enhanced and corrected ***Section 8: Ordering information***: – The name of the section changed from the previous “Part numbering”