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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f042c6t6

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- V_{DD} = V_{DDIO1} = 2.0 to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- V_{DDIO2} = 1.65 to 3.6 V: external power supply for marked I/Os. V_{DDIO2} is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA}, but it must not be provided without a valid supply on V_{DD}. The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt. Refer to the pinout diagrams or tables for concerned I/Os list.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 13: Power supply scheme*.

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD}.
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD}.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD}

threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F042x4/x6 microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

  The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1 USART1, USB or the CEC.

  The CEC, USART1 and I2C1 peripherals can be configured to enable the HSI RC oscillator so as to get clock for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.14 Inter-integrated circuit interface (I^2C)

The I^2C interface (I2C1) can operate in multimaster or slave modes. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). It also includes programmable analog and digital noise filters.

Table 8. Comparison of I^2C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs. standard requirements –Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent

Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
14	C3	10	10	10	10	PA4	I/O	TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK USB_NOE	ADC_IN4
15	D3	11	11	11	11	PA5	I/O	TTa	-	SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2	ADC_IN5
16	E3	12	12	12	12	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, TSC_G2_IO3, EVENTOUT	ADC_IN6
17	F4	13	13	13	13	PA7	I/O	TTa	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, TSC_G2_IO4, EVENTOUT	ADC_IN7
18	F3	14	14	14	-	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	ADC_IN8
19	F2	15	15	15	14	PB1	I/O	TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
20	D2	-	16	-	-	PB2	I/O	FT	-	TSC_G3_IO4	-
21	-	-	-	-	-	PB10	I/O	FTf	-	SPI2_SCK, CEC, TSC_SYNC, TIM2_CH3, I2C1_SCL	-
22	-	-	-	-	-	PB11	I/O	FTf	-	TIM2_CH4, EVENTOUT, I2C1_SDA	-
23	F1	16	0	16	15	VSS	S	-	-	Ground	
24	-	-	-	17	16	VDD	S	-	-	Digital power supply	
25	-	-	-	-	-	PB12	I/O	FT	-	TIM1_BKIN, SPI2_NSS, EVENTOUT	-

Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
46	-	-	-	-	-	PB9	I/O	FTf	-	SPI2_NSS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT, CAN_TX	-
47	-	32	0	-	-	VSS	S	-	-	Ground	
48	A5	1	1	-	-	VDD	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. Distinct VSSA pin is only available on 48-pin packages. On all other packages, the pin number corresponds to the VSS pin to which VSSA pad of the silicon die is connected.
4. PA8, PA9, PA10, PA11, PA12, PA13, PA14 and PA15 I/Os are supplied by VDDIO2.
5. Pin pair PA11/12 can be remapped in place of pin pair PA9/10 using SYSCFG_CFGR1 register.
6. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Table 17. STM32F042x4/x6 peripheral register boundary addresses

Bus	Boundary address	Size	Peripheral
	0x4800 1800 - 0x5FFF FFFF	~384 MB	Reserved
AHB2	0x4800 1400 - 0x4800 17FF	1 KB	GPIOF
	0x4800 0C00 - 0x4800 13FF	2 KB	Reserved
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
	0x4002 4400 - 0x47FF FFFF	~128 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	3 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	Flash memory interface
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0400 - 0x4002 0FFF	3 KB	Reserved
	0x4002 0000 - 0x4002 03FF	1 KB	DMA
	0x4001 8000 - 0x4001 FFFF	32 KB	Reserved
APB	0x4001 5C00 - 0x4001 7FFF	9 KB	Reserved
	0x4001 5800 - 0x4001 5BFF	1 KB	DBGMCU
	0x4001 4C00 - 0x4001 57FF	3 KB	Reserved
	0x4001 4800 - 0x4001 4BFF	1 KB	TIM17
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 3C00 - 0x4001 43FF	2 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1/I2S1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1
	0x4001 2800 - 0x4001 2BFF	1 KB	Reserved
	0x4001 2400 - 0x4001 27FF	1 KB	ADC
	0x4001 0800 - 0x4001 23FF	7 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0000 - 0x4001 03FF	1 KB	SYSCFG
	0x4000 8000 - 0x4000 FFFF	32 KB	Reserved

Table 24. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}$(1)	PVD hysteresis	-	-	100	-	mV
$I_{DD(PVD)}$	PVD current consumption	-	-	0.15	0.26(1)	µA

1. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in *Table 25* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 25. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +105 °C	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10(1)	µs
$t_{S\_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4(1)	-	-	µs
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DDA} = 3 V	-	-	10(1)	mV
T_{Coeff}	Temperature coefficient	-	- 100(1)	-	100(1)	ppm/°C

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 14: Current consumption measurement scheme*.

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Table 50. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PD}	Weak pull-down equivalent resistor(3)	V_{IN} = - V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 49: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

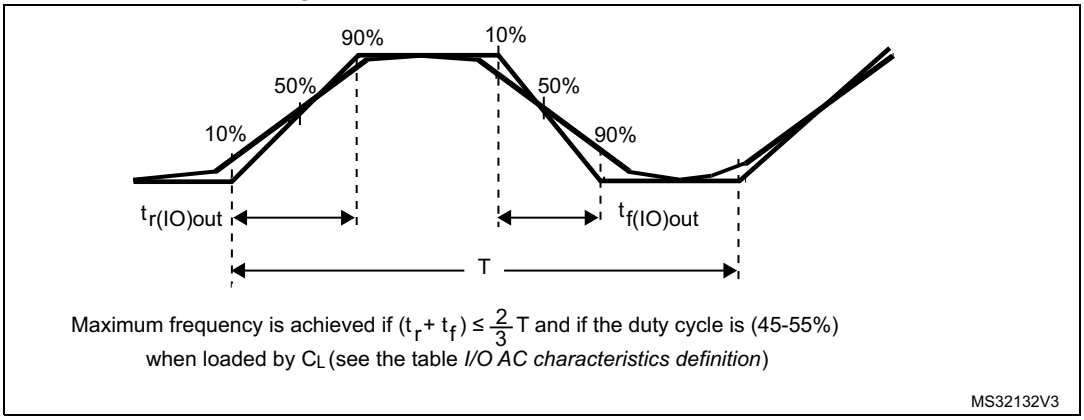
All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Table 52. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
Fm+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	12	ns
	$t_{r(IO)out}$	Output rise time		-	34	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	0.5	MHz
	$t_{f(IO)out}$	Output fall time		-	16	ns
	$t_{r(IO)out}$	Output rise time		-	44	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 24*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

Figure 24. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 53. NRST pin characteristics

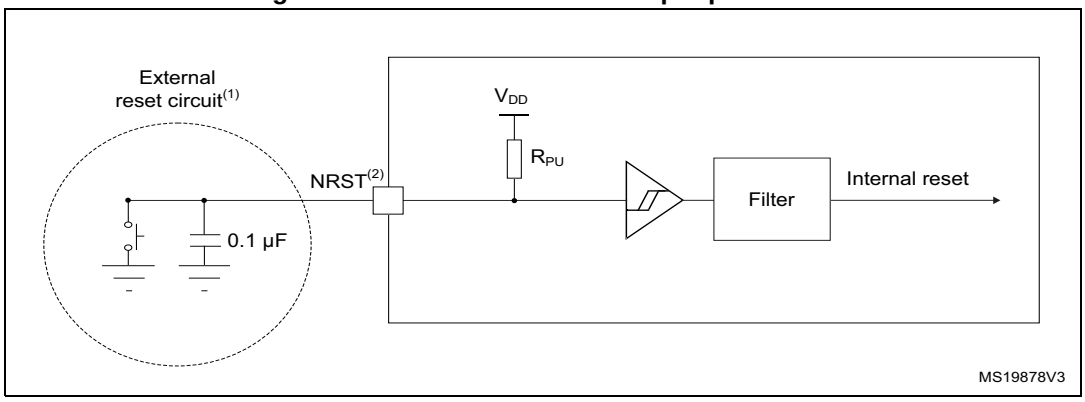
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3\ V_{DD}+0.07$(1)	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.445\ V_{DD}+0.398$(1)	-	-	

Table 53. NRST pin characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$2.7 < V_{DD} < 3.6$	300(3)	-	-	ns
		$2.0 < V_{DD} < 3.6$	500(3)	-	-	

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).
3. Data based on design simulation only. Not tested in production.

Figure 25. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under the conditions summarized in *Table 21: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
$I_{DDA\ (ADC)}$	Current consumption of the ADC(1)	$V_{DDA} = 3.3$ V	-	0.9	-	mA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	12-bit resolution	0.043	-	1	MHz

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 55. R_{AIN} max for f_{ADC} = 14 MHz

T_S (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 56. ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 3 V to 3.6 V T_A = 25 °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.7 V to 3.6 V T_A = - 40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.4 V to 3.6 V T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

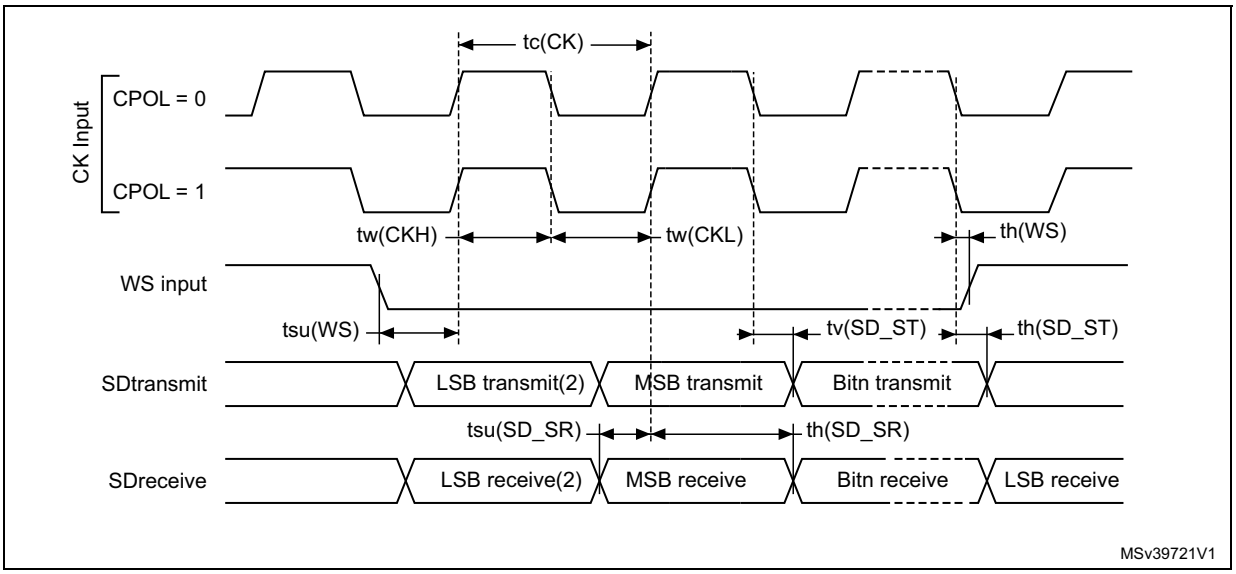
1. ADC DC accuracy values are measured after internal calibration.

Table 64. I²S characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	ns
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$(2)	Data input hold time	Master receiver	4	-	
$t_{h(SD\_SR)}$(2)		Slave receiver	0.5	-	
$t_{v(SD\_MT)}$(2)	Data output valid time	Master transmitter	-	4	
$t_{v(SD\_ST)}$(2)		Slave transmitter	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter	0	-	
$t_{h(SD\_ST)}$		Slave transmitter	13	-	

1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then T_{PCLK} = 1/f_{PLCLK} = 125 ns.

Figure 31. I²S slave timing diagram (Philips protocol)



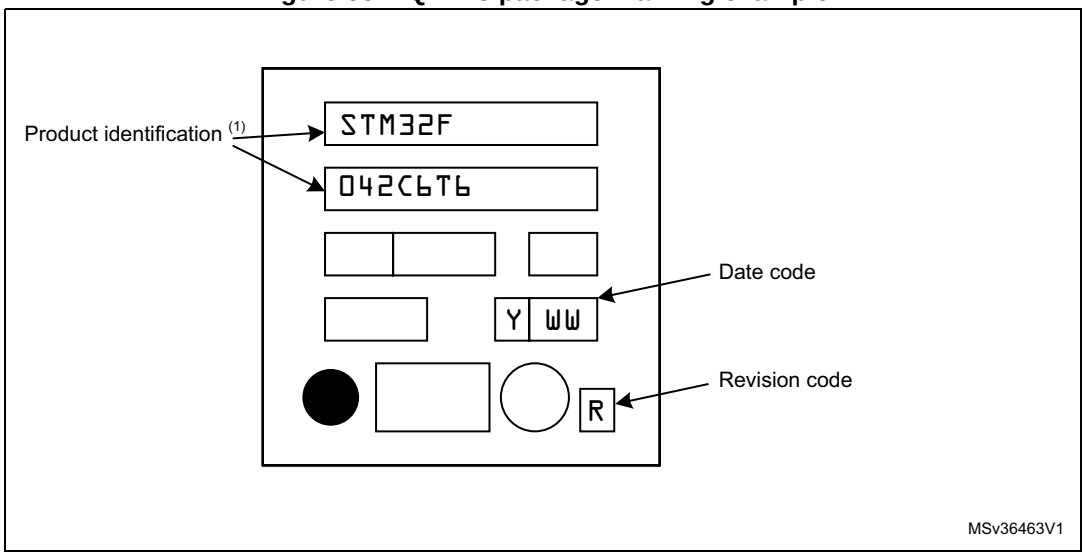
1. Measurement points are done at CMOS levels: 0.3 × V_{DDIOx} and 0.7 × V_{DDIOx}.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 35. LQFP48 package marking example



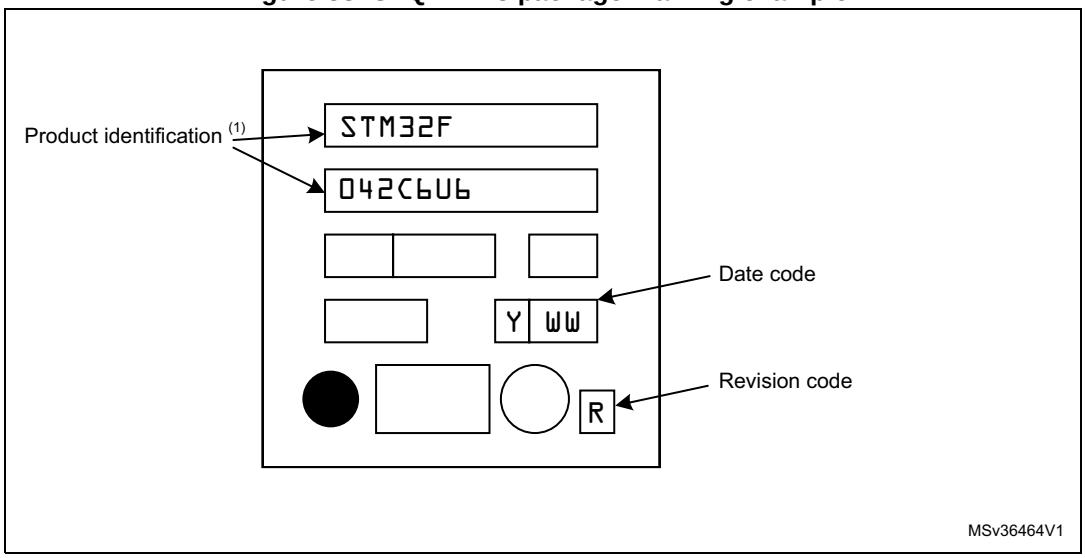
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 38. UFQFPN48 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 68. WLCSP36 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	-	0.3025	-	-	0.0119	-
G	-	0.3515	-	-	0.0138	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 40. Recommended pad footprint for WLCSP36 package

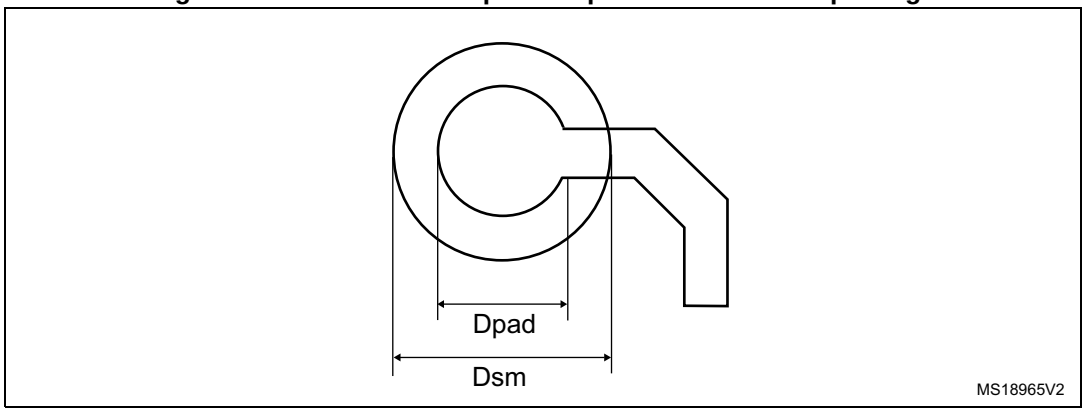


Table 69. WLCSP36 recommended PCB design rules

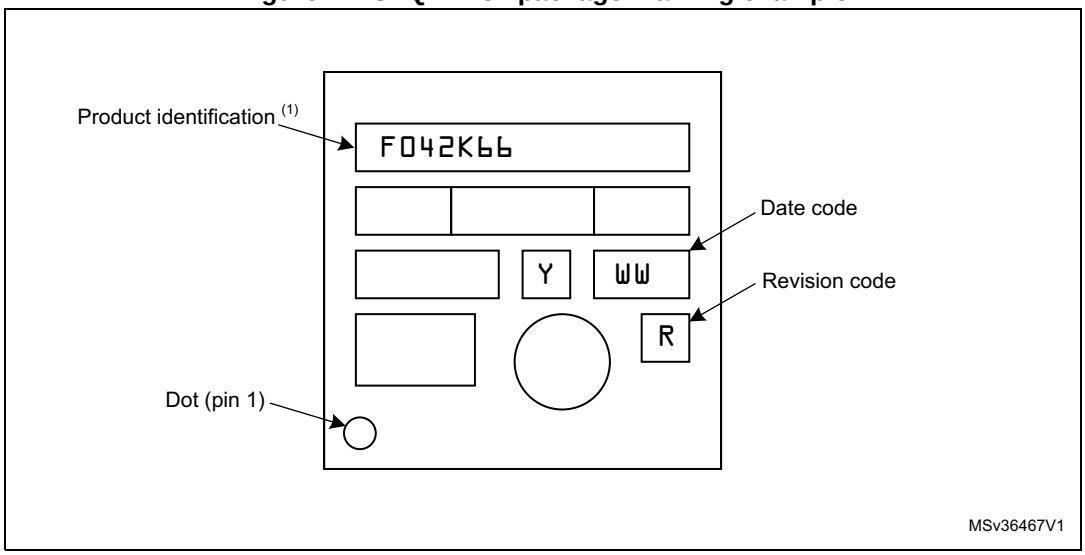
Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 47. UFQFPN32 package marking example



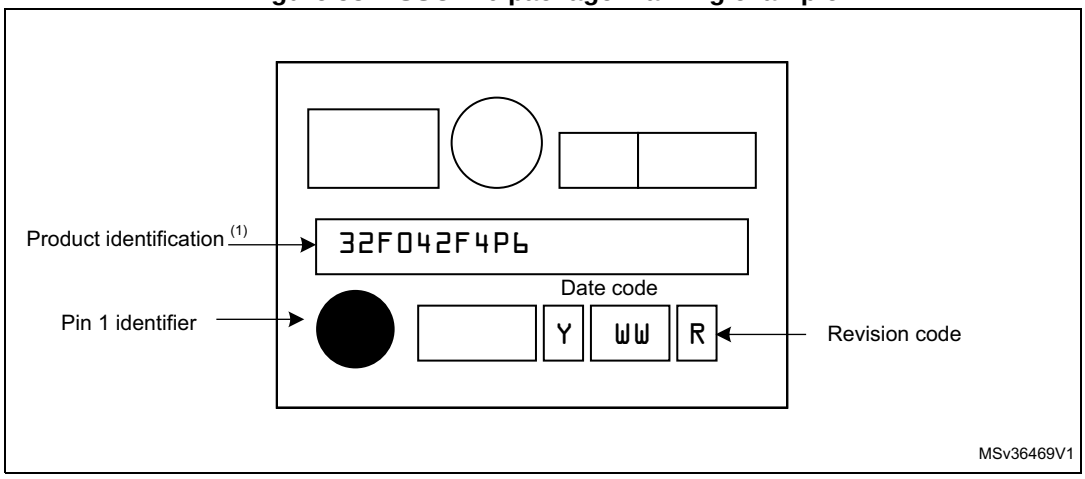
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 53. TSSOP20 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 76. Document revision history (continued)

Date	Revision	Changes
26-Oct-2015	3	– *Table 9: STM32F042x4/x6 I^2C implementation* - adding 20 mA **Updates in *Section 4: Pinouts and pin descriptions*** – *Table 12: Legend/abbreviations used in the pinout table* - removing “I” pin type **Updates in *Section 5: Memory mapping*:** – *Figure 10: STM32F042x6 memory map*, x4 difference described in text **Updates in *Section 6: Electrical characteristics*:** – the condition “Regulator in run mode, all oscillators OFF” in *Table 28: Typical and maximum consumption in Stop and Standby modes*, – footnote for V_{IN} max value in *Table 18: Voltage characteristics,* – footnote for max V_{IN} in *Table 21: General operating conditions*, – t_{START} parameter definition in *Table 25: Embedded internal reference voltage* – addition of t_{START} parameter in *Table 25: Embedded internal reference voltage,* removal of -40°C to 85°C condition and the associated footnote – *Table 26: Typical and maximum current consumption from VDD supply at VDD = 3.6 V:* removing “code executing from Flash or RAM” – removal of the min value for t_{START} parameter in *Table 57: TS characteristics* – the typical value for R parameter in *Table 58: VBAT monitoring characteristics* – removal of Res_{TM} parameter line from *Table 59: TIMx characteristics* and putting all values in new Typ column, substitution of $t_{COUNTER}$ with $t_{MAX\_COUNT,}$ values defined as powers of two – $V_{ESD(CDM)}$ class in *Table 47: ESD absolute maximum ratings* – reorganization of *Table 64: I^2S characteristics* and filling max value of $t_{v(SD\_ST)}$ – adding definition of levels in *Figure 32: I^2S master timing diagram (Philips protocol)* **Updates in *Section 7: Package information***: – heading and display of columns in *Table 68: WLCSP36 package mechanical data*., – *Figure 38: UFQFPN48 package marking example* – *Figure 41: WLCSP36 package marking example* – *Figure 50: UFQFPN28 package marking example* – *Figure 41: WLCSP36 package marking example* – *Figure 51: TSSOP20 package outline* - correcting GAGE to GAUGE – removing “die 445” from *Table 74: Package thermal characteristics* **Updates in *Section 8: Part numbering*:** – adding tray packing to options