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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f042c6u7

Table 10. STM32F042x4/x6 USART implementation (continued)

USART modes/features ⁽¹⁾	USART1	USART2
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X = supported.

3.16 Serial peripheral interface (SPI) / Inter-integrated sound interface (I²S)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I²S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F042x4/x6 SPI/I²S implementation

SPI features ⁽¹⁾	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I ² S mode	X	-
TI mode	X	X

1. X = supported.

3.17 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.18 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames

with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.19 Universal serial bus (USB)

The STM32F042x4/x6 embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB (the last 256 byte are used for CAN peripheral if enabled) and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.20 Clock recovery system (CRS)

The STM32F042x4/x6 embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.21 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 13. STM32F042x pin definitions

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSOP20					Alternate function	Additional functions
1	-	-	-	-	-	VBAT	S	-	-	Backup power supply	
2	A6	-	-	-	-	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
3	B6	-	-	-	-	PC14- OSC32_IN (PC14)	I/O	TC	(1) (2)	-	OSC32_IN
4	C6	-	-	-	-	PC15- OSC32_OUT (PC15)	I/O	TC	(1) (2)	-	OSC32_OUT
5	B5	2	2	2	2	PF0-OSC_IN (PF0)	I/O	FTf	-	CRS_SYNC I2C1_SDA	OSC_IN
6	C5	3	3	3	3	PF1-OSC_OUT (PF1)	I/O	FTf	-	I2C1_SCL	OSC_OUT
7	D5	4	4	4	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	D6	32	0	16	15	VSSA	S		(3)	Analog ground	
9	E5	5	5	5	5	VDDA	S		-	Analog power supply	
10	F6	6	6	6	6	PA0	I/O	TTa	-	USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1	RTC_ TAMP2, WKUP1, ADC_IN0,
11	D4	7	7	7	7	PA1	I/O	TTa	-	USART2_RTS, TIM2_CH2, TSC_G1_IO2, EVENTOUT	ADC_IN1
12	E4	8	8	8	8	PA2	I/O	TTa	-	USART2_TX, TIM2_CH3, TSC_G1_IO3	ADC_IN2, WKUP4
13	F5	9	9	9	9	PA3	I/O	TTa	-	USART2_RX, TIM2_CH4, TSC_G1_IO4	ADC_IN3

Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
38	A2	25	25	23	-	PA15	I/O	FT	(4)	SPI1_NSS, I2S1_WS, USART2_RX, TIM2_CH1_ETR, EVENTOUT, USB_NOE	-
39	B3	26	26	24	-	PB3	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	-
40	A3	27	27	25	-	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
41	E6	28	28	26	-	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6
42	C4	29	29	27	-	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_IO3	-
43	A4	30	30	28	-	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4	-
44	-	-	31	-	-	PF11-BOOT0	I/O	FT	-	-	Boot memory selection
-	B4	31	-	1	1	PB8-BOOT0	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	Boot memory selection
45	-	-	32	-	-	PB8	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	-

6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme

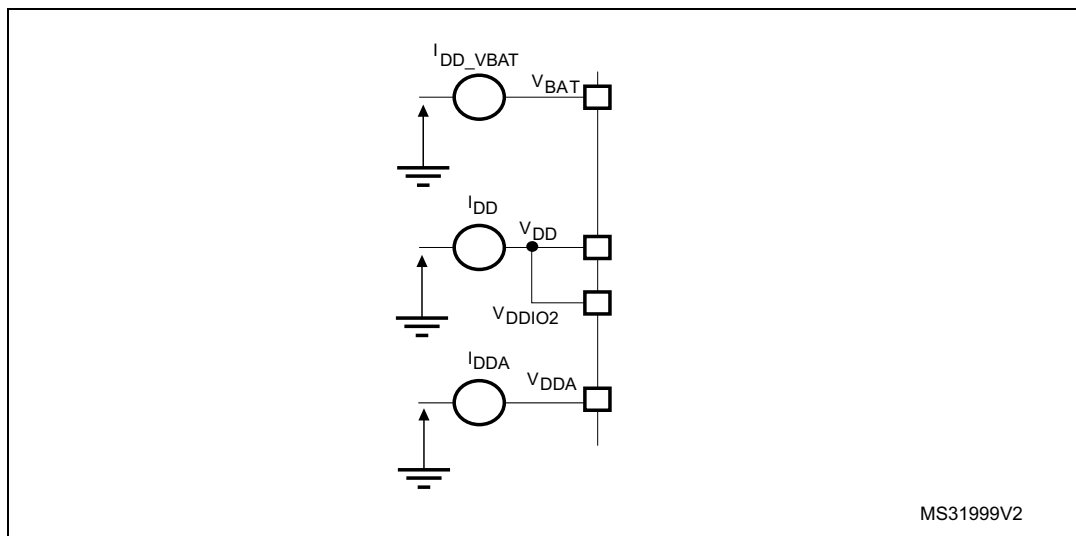


Table 19. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source) ⁽¹⁾	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink) ⁽¹⁾	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source) ⁽¹⁾	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink) ⁽¹⁾	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins ⁽²⁾	80	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	-80	
	Total output current sourced by sum of all I/Os supplied by VDDIO2	-40	
$I_{INJ(PIN)}^{(3)}$	Injected current on FT and FTf pins	-5/+0 ⁽⁴⁾	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins ⁽⁵⁾	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	± 25	

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 18: Voltage characteristics](#) for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note ⁽²⁾ below [Table 56: ADC accuracy](#).
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 20. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	150	°C

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	$\mu\text{s/V}$
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 23](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}^{(1)}$	Power on/power down reset threshold	Falling edge ⁽²⁾	1.80	1.88	1.96 ⁽³⁾	V
		Rising edge	1.84 ⁽³⁾	1.92	2.00	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}^{(4)}$	Reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD} .
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

Table 24. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V

Table 24. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}^{(1)}$	PVD hysteresis	-	-	100	-	mV
$I_{DD(PVD)}$	PVD current consumption	-	-	0.15	0.26 ⁽¹⁾	μ A

1. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in [Table 25](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 25. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10 ⁽¹⁾	μ s
$t_{S_vrefint}$	ADC sampling time when reading the internal reference voltage	-	4 ⁽¹⁾	-	-	μ s
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DDA} = 3\text{ V}$	-	-	10 ⁽¹⁾	mV
T_{Coff}	Temperature coefficient	-	- 100 ⁽¹⁾	-	100 ⁽¹⁾	ppm/ $^{\circ}\text{C}$

1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 14: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

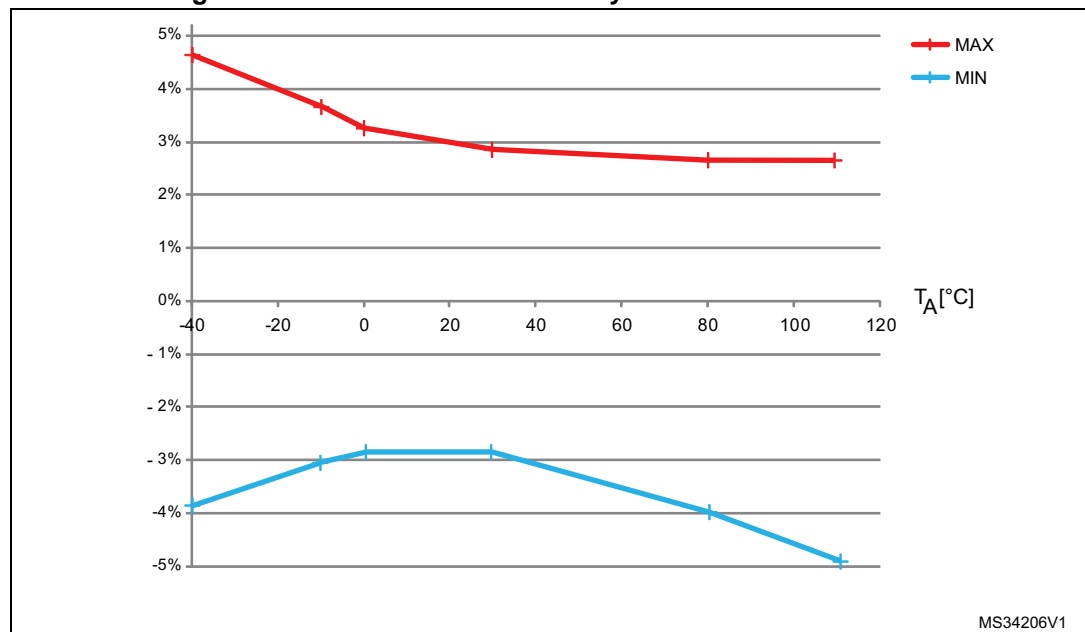
High-speed internal 48 MHz (HSI48) RC oscillator

Table 40. HSI48 oscillator characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	Frequency	-	-	48	-	MHz
TRIM	HSI48 user-trimming step	-	0.09 ⁽²⁾	0.14	0.2 ⁽²⁾	%
DuCy _(HSI48)	Duty cycle	-	45 ⁽²⁾	-	55 ⁽²⁾	%
$\text{ACC}_{\text{HSI48}}$	Accuracy of the HSI48 oscillator (factory calibrated)	$T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$	-4.9 ⁽³⁾	-	4.7 ⁽³⁾	%
		$T_A = -10 \text{ to } 85 \text{ }^\circ\text{C}$	-4.1 ⁽³⁾	-	3.7 ⁽³⁾	%
		$T_A = 0 \text{ to } 70 \text{ }^\circ\text{C}$	-3.8 ⁽³⁾	-	3.4 ⁽³⁾	%
		$T_A = 25 \text{ }^\circ\text{C}$	-2.8	-	2.9	%
$t_{\text{su(HSI48)}}$	HSI48 oscillator startup time	-	-	-	6 ⁽²⁾	μs
$I_{\text{DDA(HSI48)}}$	HSI48 oscillator power consumption	-	-	312	350 ⁽²⁾	μA

1. $V_{\text{DDA}} = 3.3 \text{ V}$, $T_A = -40 \text{ to } 105 \text{ }^\circ\text{C}$ unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 21. HSI48 oscillator accuracy characterization results



Low-speed internal (LSI) RC oscillator

Table 41. LSI oscillator characteristics⁽¹⁾

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}	Frequency	30	40	50	kHz
$t_{su(LSI)}^{(2)}$	LSI oscillator startup time	-	-	85	μ s
$I_{DDA(LSI)}^{(2)}$	LSI oscillator power consumption	-	0.75	1.2	μ A

1. $V_{DDA} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in [Table 42](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 42. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
f_{PLL_IN}	PLL input clock ⁽¹⁾	1 ⁽²⁾	8.0	24 ⁽²⁾	MHz
	PLL input clock duty cycle	40 ⁽²⁾	-	60 ⁽²⁾	%
f_{PLL_OUT}	PLL multiplier output clock	16 ⁽²⁾	-	48	MHz
t_{LOCK}	PLL lock time	-	-	200 ⁽²⁾	μ s
Jitter _{PLL}	Cycle-to-cycle jitter	-	-	300 ⁽²⁾	ps

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT} .

2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

Table 43. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max ⁽¹⁾	Unit
t_{prog}	16-bit programming time	$T_A = -40$ to $+105$ °C	40	53.5	60	μ s
t_{ERASE}	Page (1 KB) erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
t_{ME}	Mass erase time	$T_A = -40$ to $+105$ °C	20	-	40	ms
I_{DD}	Supply current	Write mode	-	-	10	mA
		Erase mode	-	-	12	mA

1. Guaranteed by design, not tested in production.

Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DDIOx} , plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 18: Voltage characteristics](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 18: Voltage characteristics](#)).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#). All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 51. Output voltage characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	1.3	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 1.3$	-	
$V_{OL}^{(3)}$	Output low level voltage for an I/O pin	$ I_{IO} = 6 \text{ mA}$ $V_{DDIOx} \geq 2 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	
$V_{OL}^{(4)}$	Output low level voltage for an I/O pin	$ I_{IO} = 4 \text{ mA}$	-	0.4	V
$V_{OH}^{(4)}$	Output high level voltage for an I/O pin		$V_{DDIOx} - 0.4$	-	V
$V_{OLFm+}^{(3)}$	Output low level voltage for an FTf I/O pin in Fm+ mode	$ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$	-	0.4	V
		$ I_{IO} = 10 \text{ mA}$	-	0.4	V

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 18: Voltage characteristics](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.
4. Data based on characterization results. Not tested in production.

Table 54. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{\text{TRIG}}^{(2)}$	External trigger frequency	$f_{\text{ADC}} = 14 \text{ MHz}$, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{\text{ADC}}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
$R_{\text{AIN}}^{(2)}$	External input impedance	See Equation 1 and Table 55 for details	-	-	50	k Ω
$R_{\text{ADC}}^{(2)}$	Sampling switch resistance	-	-	-	1	k Ω
$C_{\text{ADC}}^{(2)}$	Internal sample and hold capacitor	-	-	-	8	pF
$t_{\text{CAL}}^{(2)(3)}$	Calibration time	$f_{\text{ADC}} = 14 \text{ MHz}$	5.9			μs
		-	83			$1/f_{\text{ADC}}$
$W_{\text{LATENCY}}^{(2)(4)}$	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
$t_{\text{latr}}^{(2)}$	Trigger conversion latency	$f_{\text{ADC}} = f_{\text{PCLK}}/2 = 14 \text{ MHz}$	0.196			μs
		$f_{\text{ADC}} = f_{\text{PCLK}}/2$	5.5			$1/f_{\text{PCLK}}$
		$f_{\text{ADC}} = f_{\text{PCLK}}/4 = 12 \text{ MHz}$	0.219			μs
		$f_{\text{ADC}} = f_{\text{PCLK}}/4$	10.5			$1/f_{\text{PCLK}}$
		$f_{\text{ADC}} = f_{\text{HSI14}} = 14 \text{ MHz}$	0.179	-	0.250	μs
$\text{Jitter}_{\text{ADC}}$	ADC jitter on trigger conversion	$f_{\text{ADC}} = f_{\text{HSI14}}$	-	1	-	$1/f_{\text{HSI14}}$
$t_{\text{S}}^{(2)}$	Sampling time	$f_{\text{ADC}} = 14 \text{ MHz}$	0.107	-	17.1	μs
		-	1.5	-	239.5	$1/f_{\text{ADC}}$
$t_{\text{STAB}}^{(2)}$	Stabilization time	-	14			$1/f_{\text{ADC}}$
$t_{\text{CONV}}^{(2)}$	Total conversion time (including sampling time)	$f_{\text{ADC}} = 14 \text{ MHz}$, 12-bit resolution	1	-	18	μs
		12-bit resolution	14 to 252 (t_{S} for sampling + 12.5 for successive approximation)			$1/f_{\text{ADC}}$

1. During conversion of the sampled value ($12.5 \times \text{ADC clock period}$), an additional consumption of $100 \mu\text{A}$ on I_{DDA} and $60 \mu\text{A}$ on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above ([Equation 1](#)) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 55. R_{AIN} max for $f_{ADC} = 14$ MHz

T_s (cycles)	t_s (μs)	R_{AIN} max (kΩ) ⁽¹⁾
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

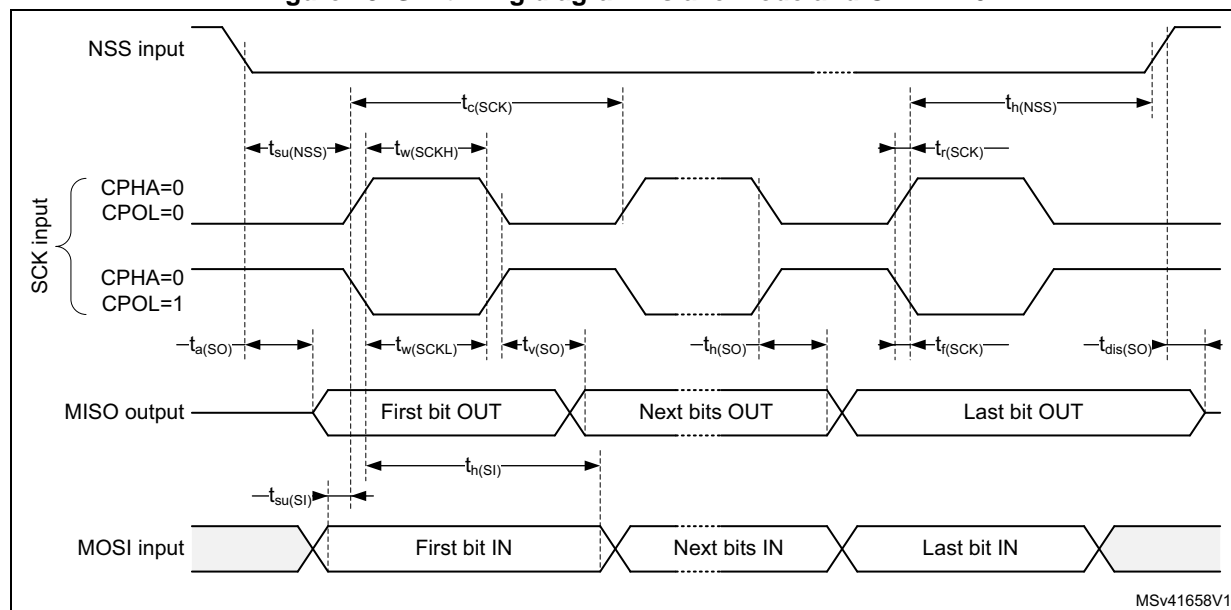
1. Guaranteed by design, not tested in production.

Table 56. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

Symbol	Parameter	Test conditions	Typ	Max ⁽⁴⁾	Unit
ET	Total unadjusted error	$f_{PCLK} = 48$ MHz, $f_{ADC} = 14$ MHz, $R_{AIN} < 10$ kΩ $V_{DDA} = 3$ V to 3.6 V $T_A = 25$ °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	$f_{PCLK} = 48$ MHz, $f_{ADC} = 14$ MHz, $R_{AIN} < 10$ kΩ $V_{DDA} = 2.7$ V to 3.6 V $T_A = -40$ to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	$f_{PCLK} = 48$ MHz, $f_{ADC} = 14$ MHz, $R_{AIN} < 10$ kΩ $V_{DDA} = 2.4$ V to 3.6 V $T_A = 25$ °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

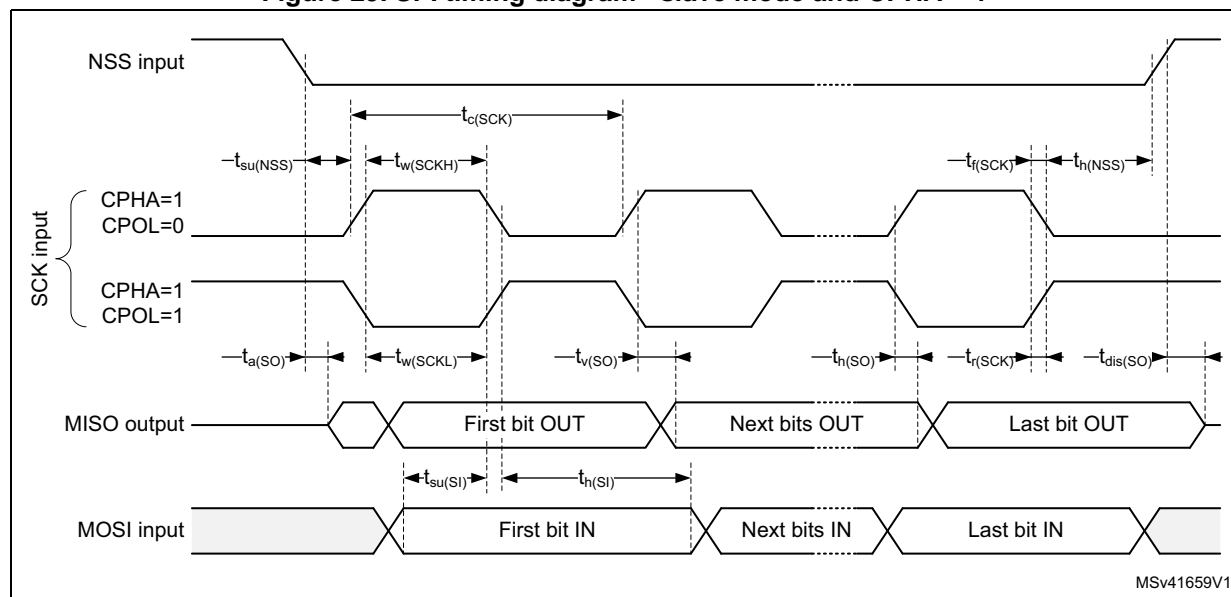
1. ADC DC accuracy values are measured after internal calibration.

Figure 28. SPI timing diagram - slave mode and CPHA = 0



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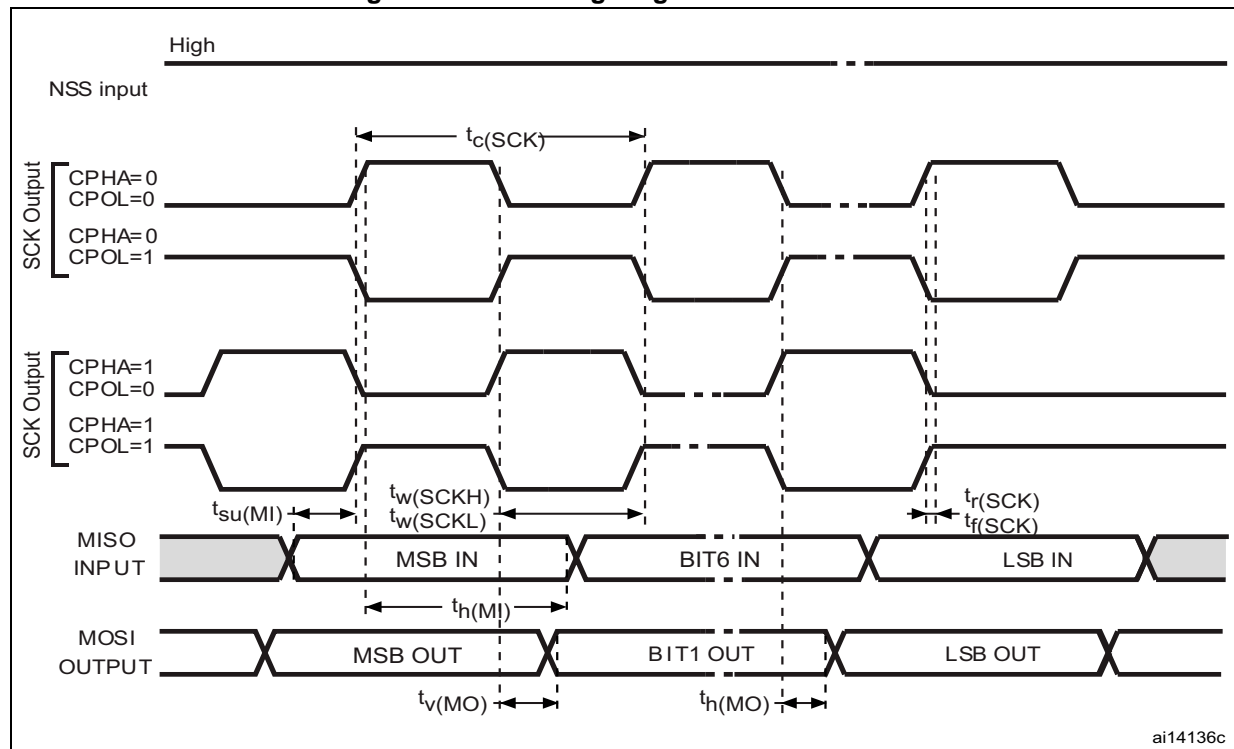
Figure 29. SPI timing diagram - slave mode and CPHA = 1



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1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

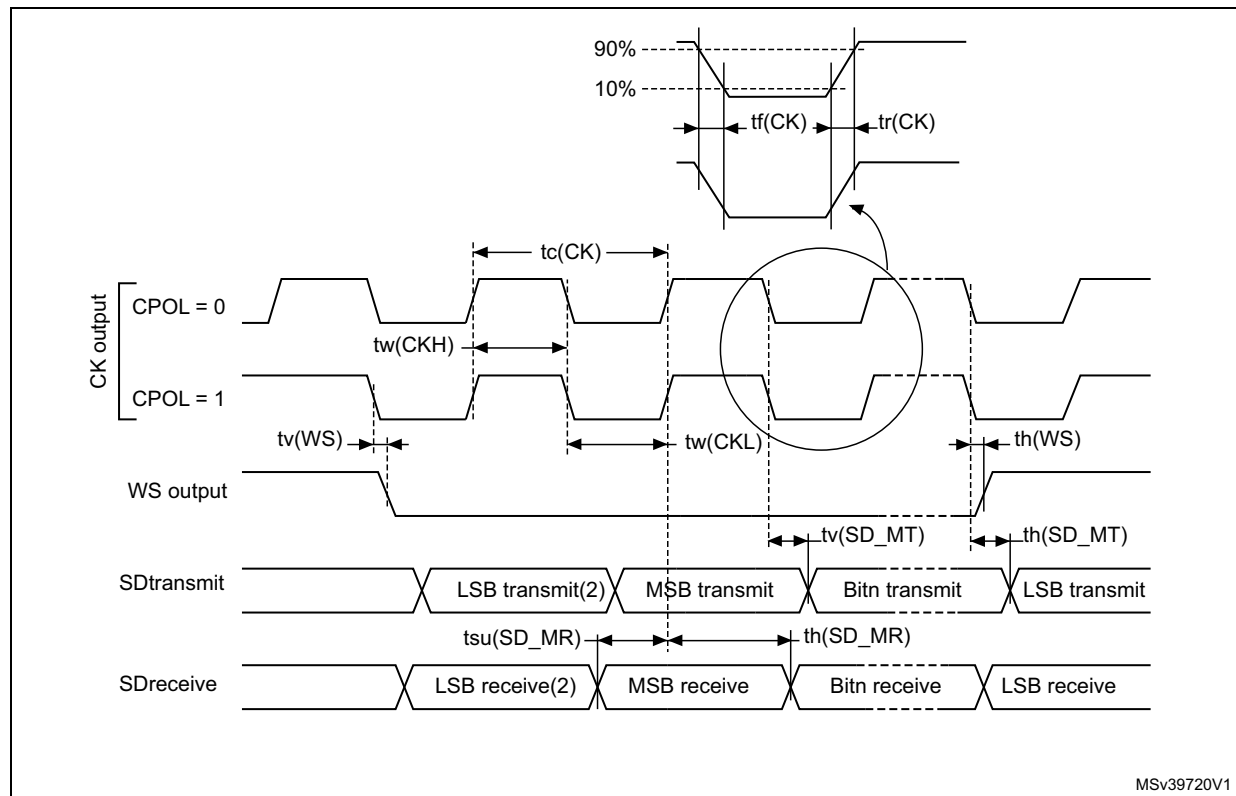
Figure 30. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

Table 64. I²S characteristics⁽¹⁾

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I ² S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)	1.597	1.601	MHz
		Slave mode	0	6.5	
$t_{r(CK)}$	I ² S clock rise time	Capacitive load $C_L = 15$ pF	-	10	ns
$t_{f(CK)}$	I ² S clock fall time		-	12	
$t_{w(CKH)}$	I ² S clock high time	Master $f_{PCLK} = 16$ MHz, audio frequency = 48 kHz	306	-	
$t_{w(CKL)}$	I ² S clock low time		312	-	
$t_{v(WS)}$	WS valid time	Master mode	2	-	
$t_{h(WS)}$	WS hold time	Master mode	2	-	
$t_{su(WS)}$	WS setup time	Slave mode	7	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
DuCy(SCK)	I ² S slave input clock duty cycle	Slave mode	25	75	%

Figure 32. I²S master timing diagram (Philips protocol)

1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

USB characteristics

The STM32F042x4/x6 USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 65. USB electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
V_{DDIO2}	USB transceiver operating voltage	-	3.0 ⁽¹⁾	-	3.6	V
$t_{STARTUP}^{(2)}$	USB transceiver startup time	-	-	-	1.0	μs
R_{PUI}	Embedded USB_DP pull-up value during idle	-	1.1	1.26	1.5	kΩ
R_{PUR}	Embedded USB_DP pull-up value during reception	-	2.0	2.26	2.6	
$Z_{DRV}^{(2)}$	Output driver impedance ⁽³⁾	Driving high and low	28	40	44	Ω

1. The STM32F042x4/x6 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V voltage range.
2. Guaranteed by design, not tested in production.
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

CAN (controller area network) interface

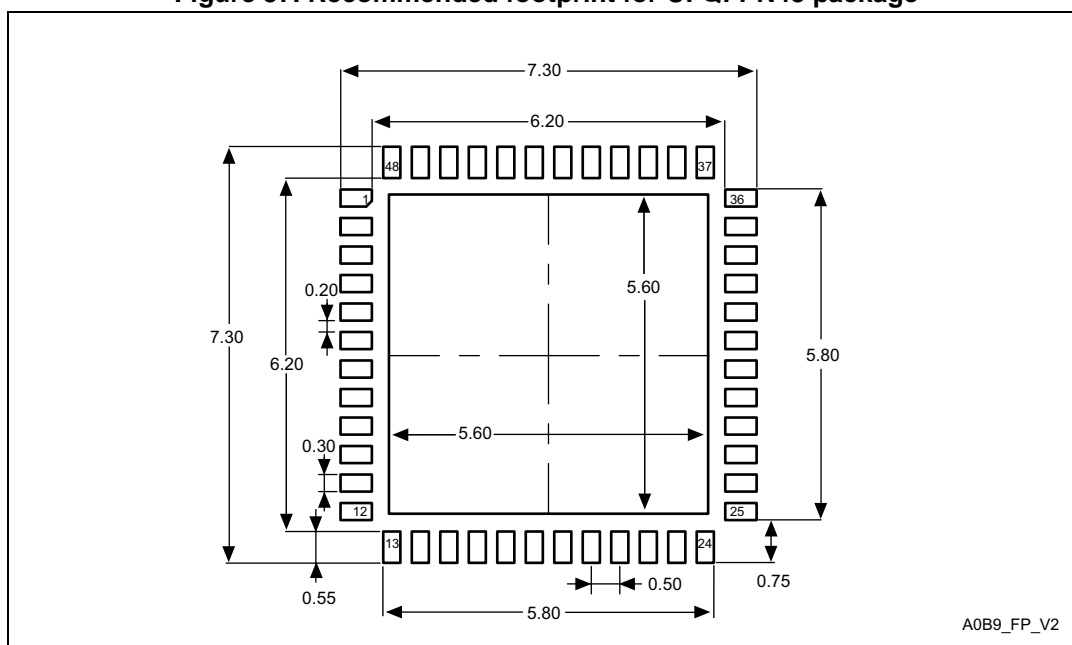
Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

Table 67. UFQFPN48 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. Recommended footprint for UFQFPN48 package



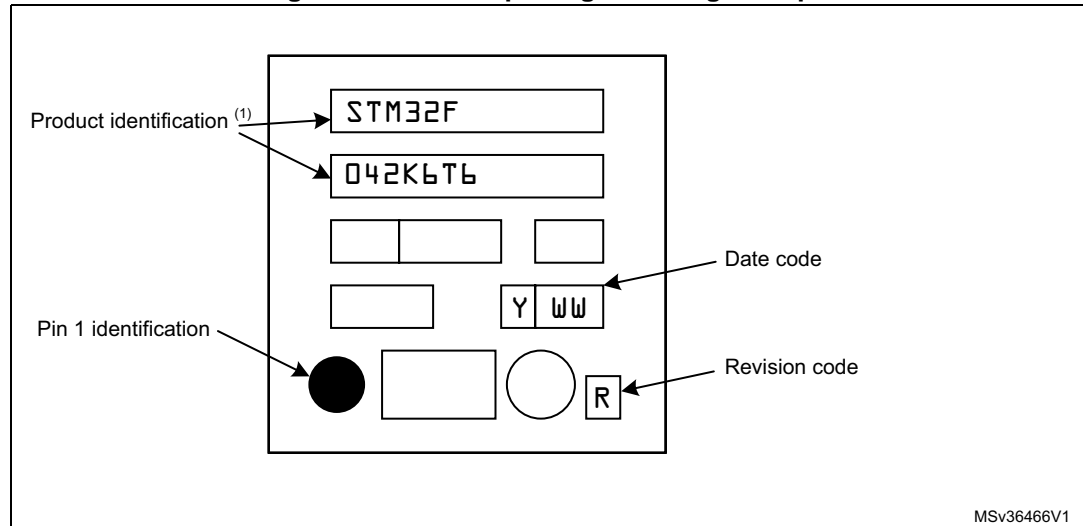
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 44. LQFP32 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.5 UFQFPN32 package information

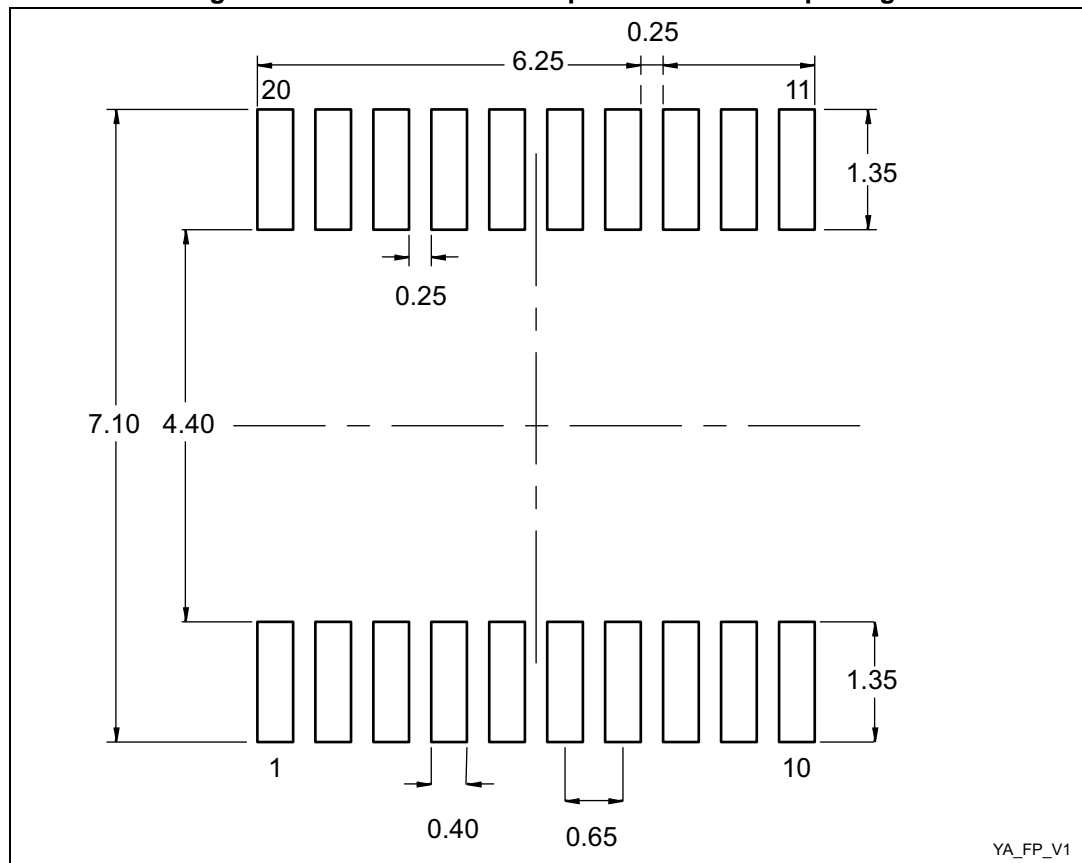
UFQFPN32 is a 32-pin, 5x5 mm, 0.5 mm pitch ultra-thin fine-pitch quad flat package.

Table 73. TSSOP20 package mechanical data (continued)

Symbol	millimeters			inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension "E1" does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 52. Recommended footprint for TSSOP20 package



1. Dimensions are expressed in millimeters.