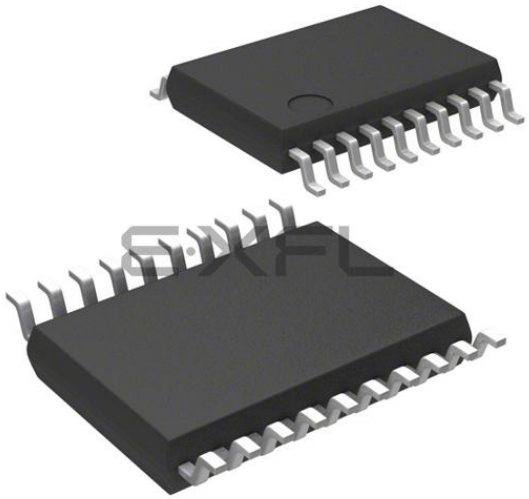

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	16
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f042f4p6tr

2 Description

The STM32F042x4/x6 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash memory and 6 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one I^2C, two SPIs/one I^2S, one HDMI CEC and two USARTs), one USB Full-speed device (crystal-less), one CAN, one 12-bit ADC, four 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F042x4/x6 microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F042x4/x6 microcontrollers include devices in seven different packages ranging from 20 pins to 48 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F042x4/x6 microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

Figure 1. Block diagram

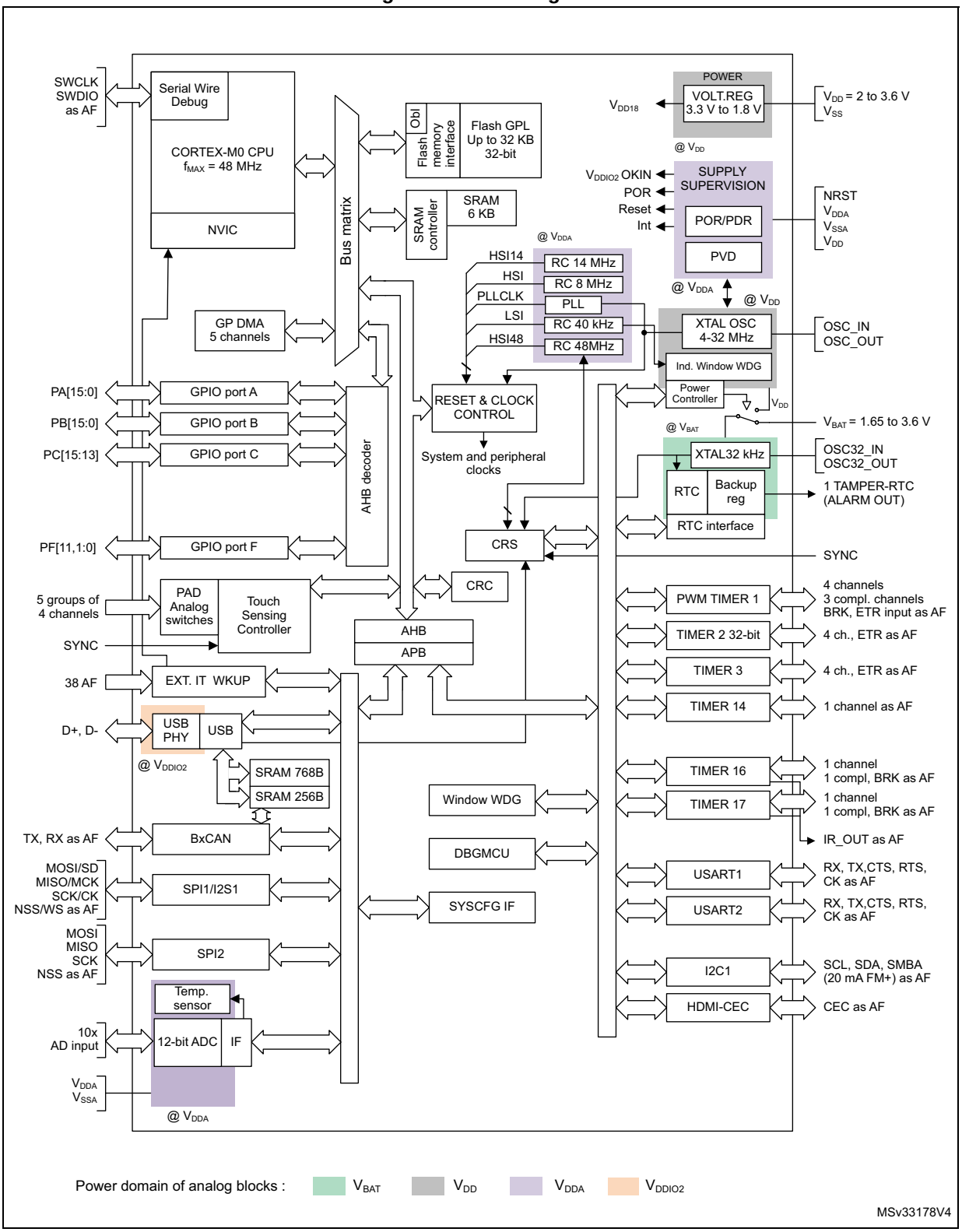
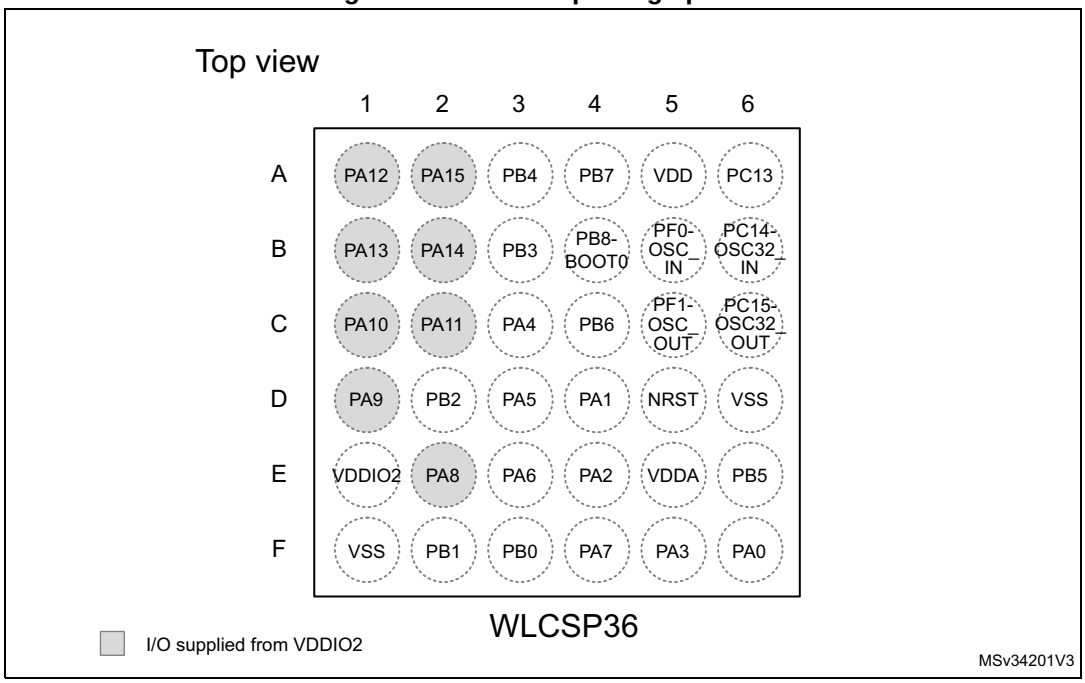


Figure 5. WLCSP36 package pinout



1. The above figure shows the package in top view, changing from bottom view in the previous document versions.

Figure 6. LQFP32 package pinout

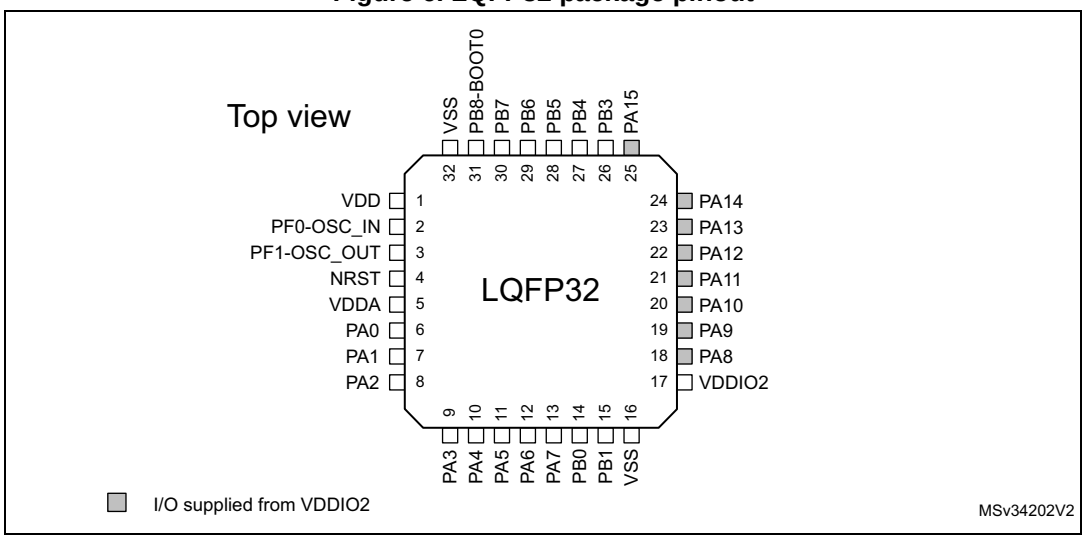


Table 13. STM32F042x pin definitions

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
1	-	-	-	-	-	VBAT	S	-	-	Backup power supply	
2	A6	-	-	-	-	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
3	B6	-	-	-	-	PC14-OSC32_IN (PC14)	I/O	TC	(1) (2)	-	OSC32_IN
4	C6	-	-	-	-	PC15-OSC32_OUT (PC15)	I/O	TC	(1) (2)	-	OSC32_OUT
5	B5	2	2	2	2	PF0-OSC_IN (PF0)	I/O	FTf	-	CRS_ SYNC I2C1_SDA	OSC_IN
6	C5	3	3	3	3	PF1-OSC_OUT (PF1)	I/O	FTf	-	I2C1_SCL	OSC_OUT
7	D5	4	4	4	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	D6	32	0	16	15	VSSA	S		(3)	Analog ground	
9	E5	5	5	5	5	VDDA	S		-	Analog power supply	
10	F6	6	6	6	6	PA0	I/O	TTa	-	USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1	RTC_ TAMP2, WKUP1, ADC_IN0,
11	D4	7	7	7	7	PA1	I/O	TTa	-	USART2_RTS, TIM2_CH2, TSC_G1_IO2, EVENTOUT	ADC_IN1
12	E4	8	8	8	8	PA2	I/O	TTa	-	USART2_TX, TIM2_CH3, TSC_G1_IO3	ADC_IN2, WKUP4
13	F5	9	9	9	9	PA3	I/O	TTa	-	USART2_RX, TIM2_CH4, TSC_G1_IO4	ADC_IN3

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3.3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 11*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 12*.

Figure 11. Pin loading conditions

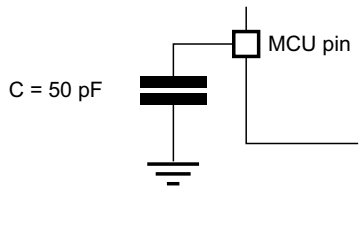
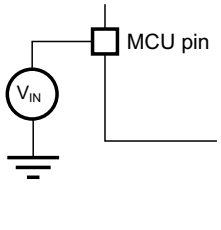


Figure 12. Pin input voltage



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in *Table 18: Voltage characteristics*, *Table 19: Current characteristics* and *Table 20: Thermal characteristics* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 18. Voltage characteristics(1)

Symbol	Ratings	Min	Max	Unit
V_{DD}–V_{SS}	External main supply voltage	- 0.3	4.0	V
V_{DDIO2}–V_{SS}	External I/O supply voltage	- 0.3	4.0	V
V_{DDA}–V_{SS}	External analog supply voltage	- 0.3	4.0	V
V_{DD}–V_{DDA}	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
V_{BAT}–V_{SS}	External backup supply voltage	- 0.3	4.0	V
V_{IN}(2)	Input voltage on FT and FTf pins	V_{SS} - 0.3	V_{DDIOx} + 4.0 (3)	V
	Input voltage on TTa pins	V_{SS} - 0.3	4.0	V
	Input voltage on any other pin	V_{SS} - 0.3	4.0	V
$\lvert\Delta V_{DDx}\rvert$	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{SSx} - V_{SS}\rvert$	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see *Section 6.3.12: Electrical sensitivity characteristics*		-

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to *Table 19: Current characteristics* for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 31. Switching output I/O current consumption

Symbol	Parameter	Conditions[1]	I/O toggling frequency (f_{SW})	Typ	Unit
I_{SW}	I/O current consumption	V_{DDIOx} = 3.3 V C =C_{INT}	4 MHz	0.07	mA
			8 MHz	0.15	
			16 MHz	0.31	
			24 MHz	0.53	
			48 MHz	0.92	
		V_{DDIOx} = 3.3 V C_{EXT} = 0 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.18	
			8 MHz	0.37	
			16 MHz	0.76	
			24 MHz	1.39	
			48 MHz	2.188	
		V_{DDIOx} = 3.3 V C_{EXT} = 10 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.32	
			8 MHz	0.64	
			16 MHz	1.25	
			24 MHz	2.23	
			48 MHz	4.442	
		V_{DDIOx} = 3.3 V C_{EXT} = 22 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.49	
			8 MHz	0.94	
			16 MHz	2.38	
			24 MHz	3.99	
		V_{DDIOx} = 3.3 V C_{EXT} = 33 pF C = C_{INT} + C_{EXT}+ C_S	4 MHz	0.64	
			8 MHz	1.25	
			16 MHz	3.24	
			24 MHz	5.02	
		V_{DDIOx} = 3.3 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.81	
			8 MHz	1.7	
			16 MHz	3.67	
		V_{DDIOx} = 2.4 V C_{EXT} = 47 pF C = C_{INT} + C_{EXT}+ C_S C = C_{int}	4 MHz	0.66	
			8 MHz	1.43	
			16 MHz	2.45	
			24 MHz	4.97	

1. C_S = 7 pF (estimated value).

Table 50. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PD}	Weak pull-down equivalent resistor(3)	V_{IN} = - V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 49: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

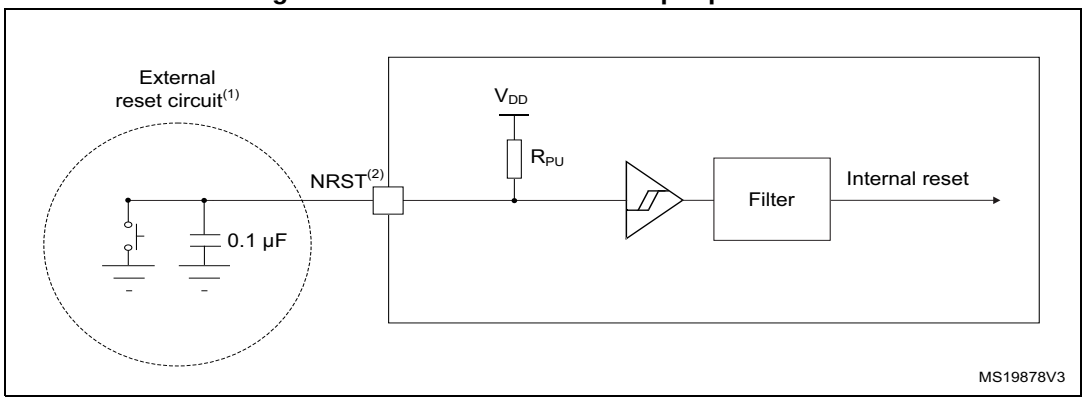
All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Table 53. NRST pin characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	25	40	55	kΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	-	-	100(1)	ns
$V_{NF(NRST)}$	NRST input not filtered pulse	$2.7 < V_{DD} < 3.6$	300(3)	-	-	ns
		$2.0 < V_{DD} < 3.6$	500(3)	-	-	

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).
3. Data based on design simulation only. Not tested in production.

Figure 25. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 53: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 54* are derived from tests performed under the conditions summarized in *Table 21: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
$I_{DDA\ (ADC)}$	Current consumption of the ADC(1)	$V_{DDA} = 3.3$ V	-	0.9	-	mA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	12-bit resolution	0.043	-	1	MHz

Table 54. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG} (2)	External trigger frequency	f_{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (2)	External input impedance	See *Equation 1* and *Table 55* for details	-	-	50	kΩ
R_{ADC} (2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC} (2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL} (2)(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$ (2)(4)	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr} (2)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 14$ MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 12$ MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.179	-	0.250	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S (2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB} (2)	Stabilization time	-	14			$1/f_{ADC}$
t_{CONV} (2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz, 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 6.3.14* does not affect the ADC accuracy.
3. Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
4. Data based on characterization results, not tested in production.

Figure 26. ADC accuracy characteristics

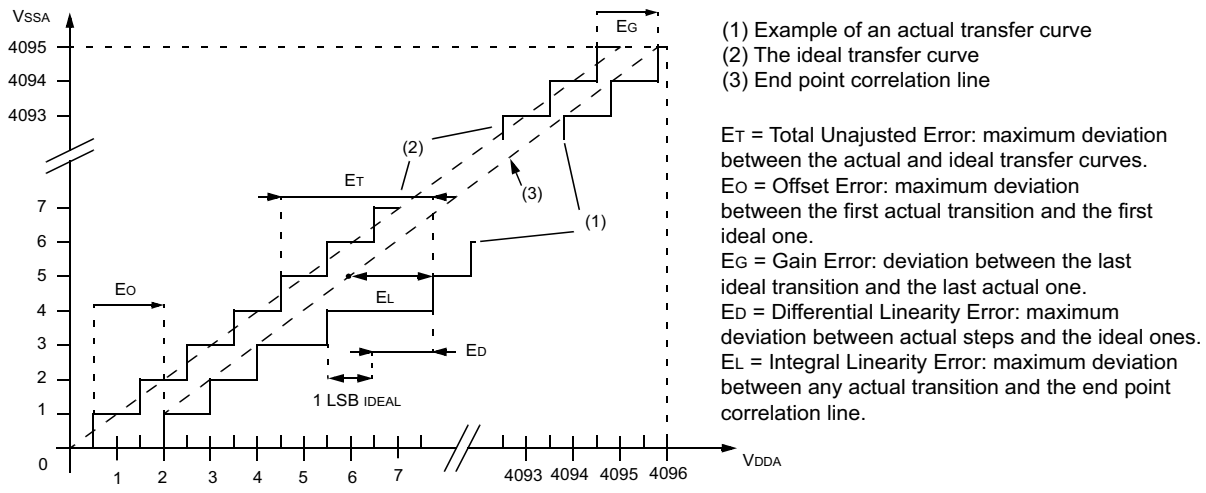
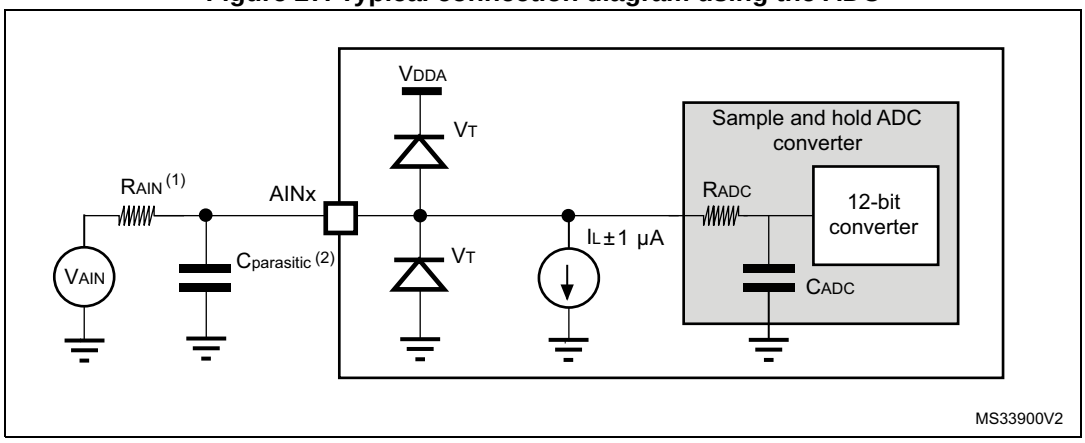


Figure 27. Typical connection diagram using the ADC



1. Refer to *Table 54: ADC characteristics* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 13: Power supply scheme*. The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

Table 60. IWDG min/max timeout period at 40 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 61. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.20 Communication interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I^2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Figure 28. SPI timing diagram - slave mode and CPHA = 0

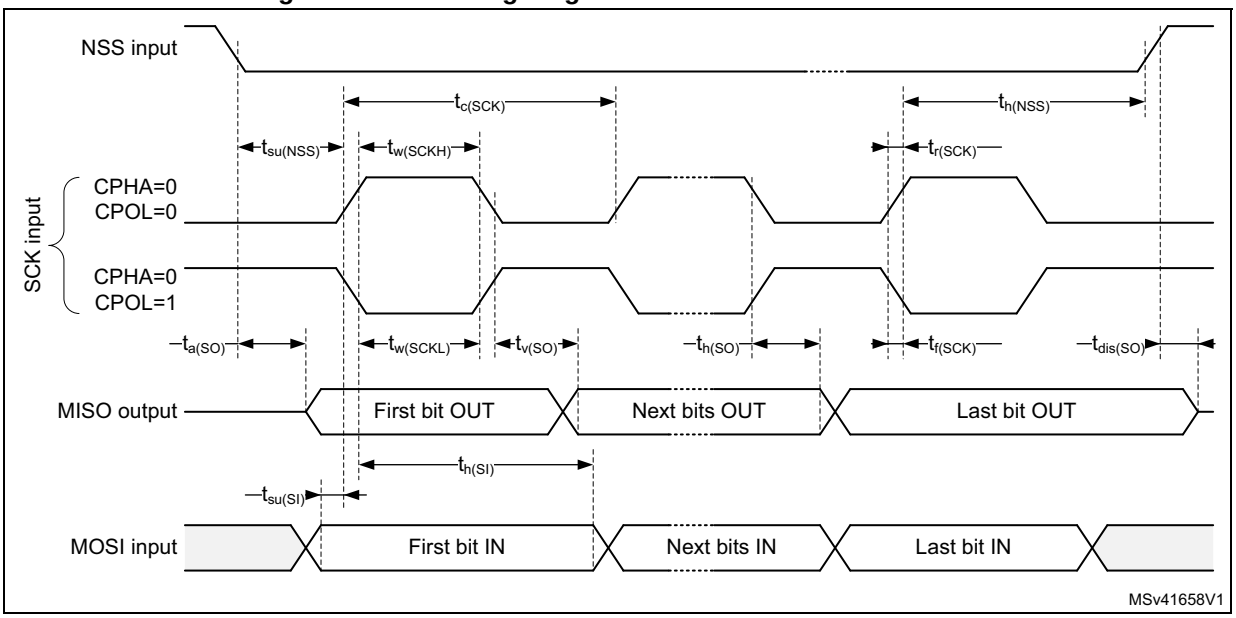
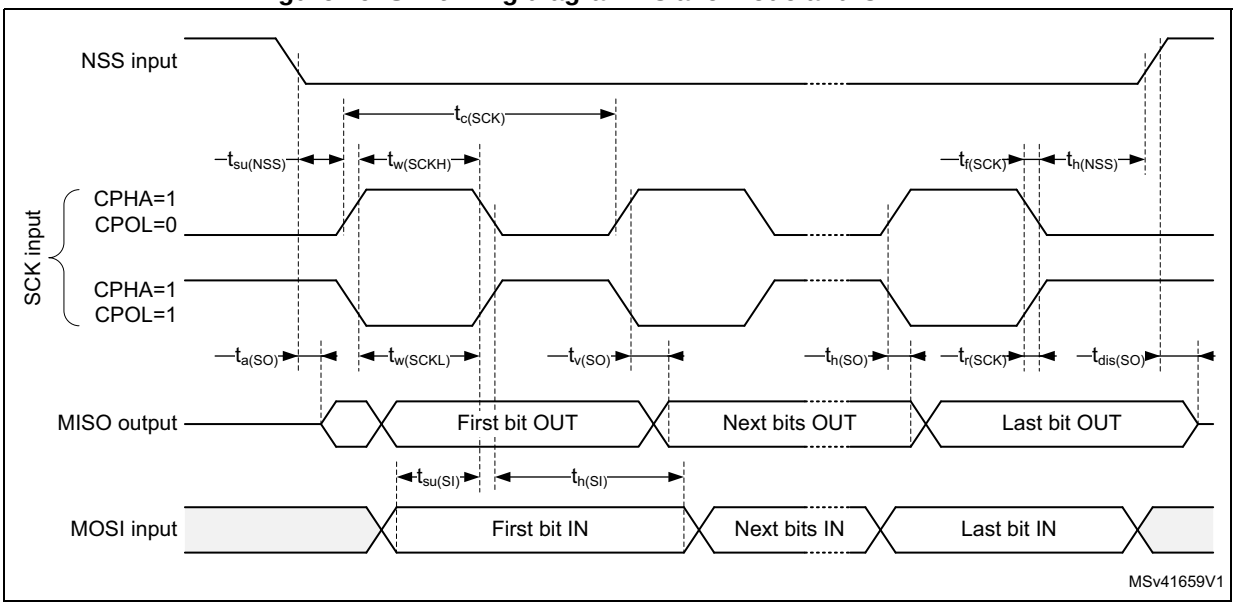


Figure 29. SPI timing diagram - slave mode and CPHA = 1



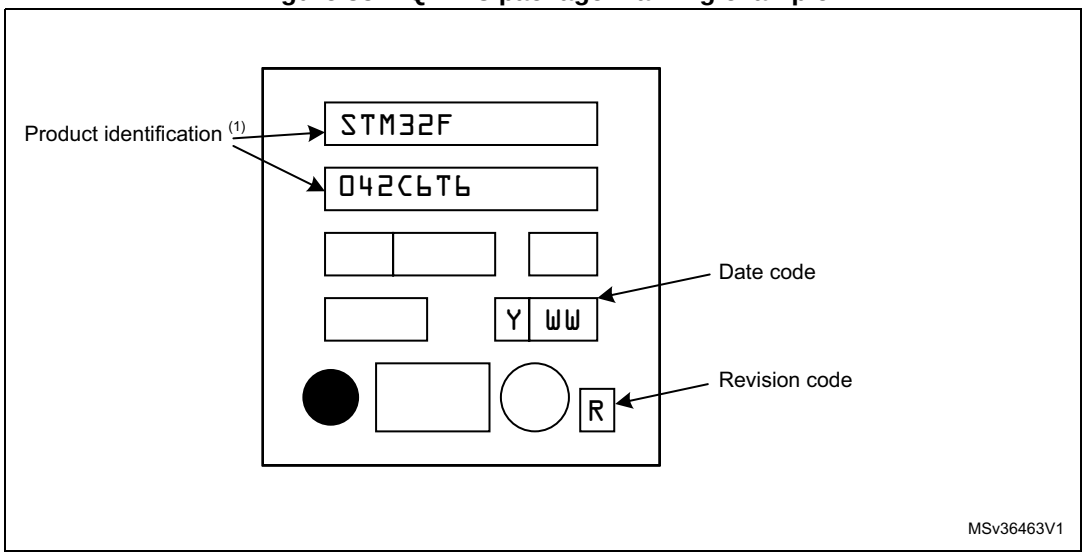
1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 35. LQFP48 package marking example

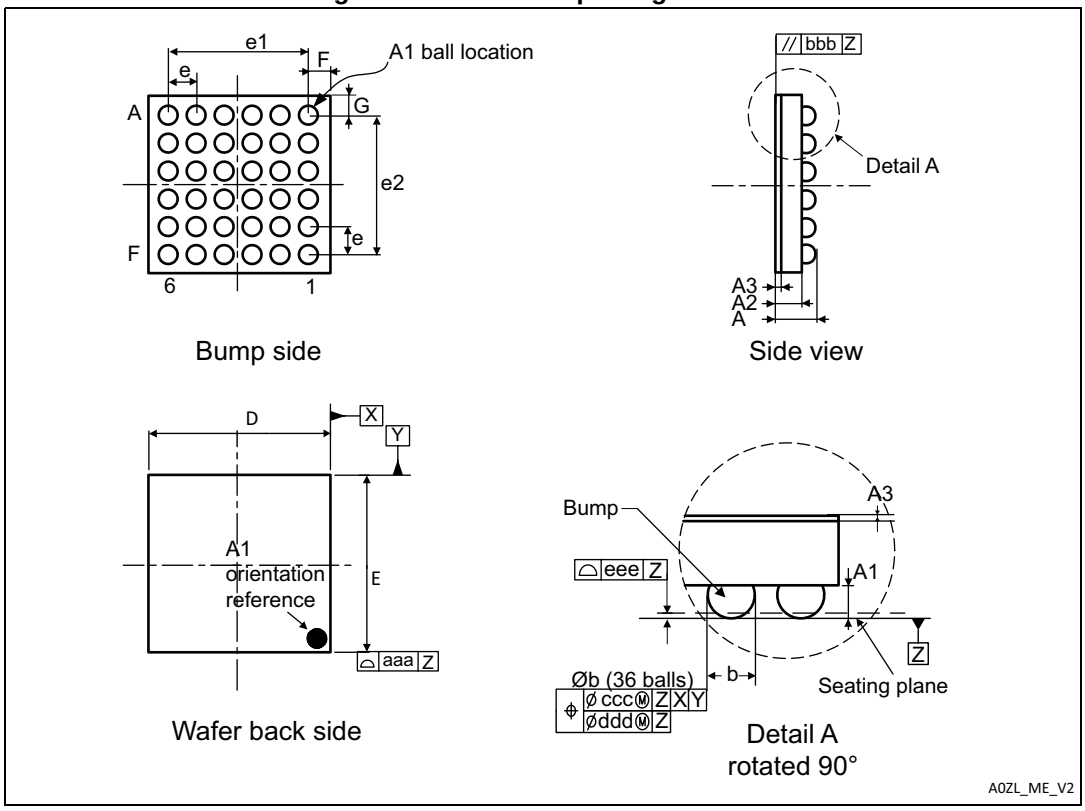


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 WLCSP36 package information

WLCSP36 is a 36-ball, 2.605 x 2.703 mm, 0.4 mm pitch wafer-level chip-scale package.

Figure 39. WLCSP36 package outline



1. Drawing is not to scale.

Table 68. WLCSP36 package mechanical data

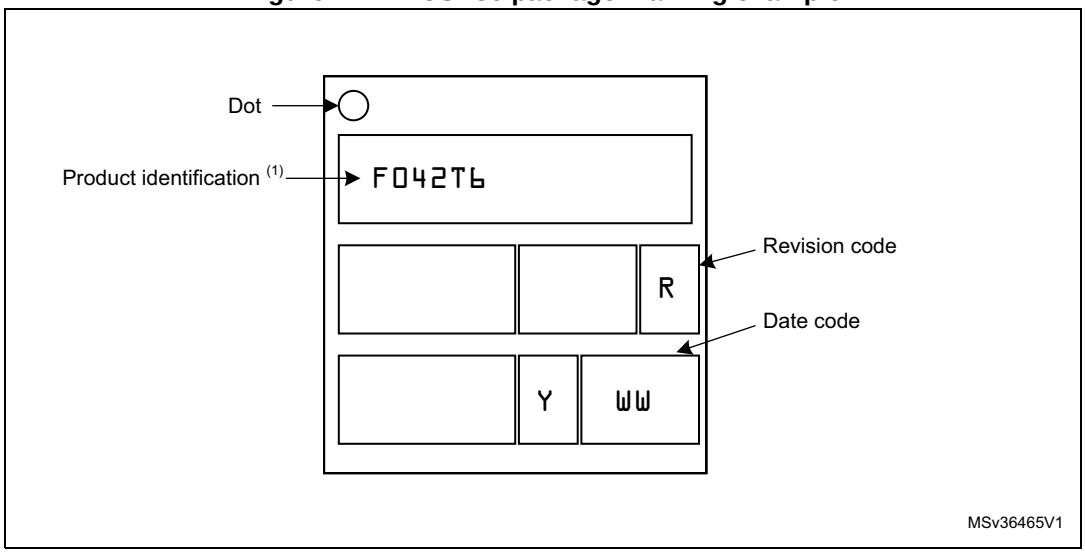
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3[2]	-	0.025	-	-	0.0010	-
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.570	2.605	2.640	0.1012	0.1026	0.1039
E	2.668	2.703	2.738	0.1050	0.1064	0.1078
e	-	0.400	-	-	0.0157	-
e1	-	2.000	-	-	0.0787	-
e2	-	2.000	-	-	0.0787	-

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 41. WLCSP36 package marking example

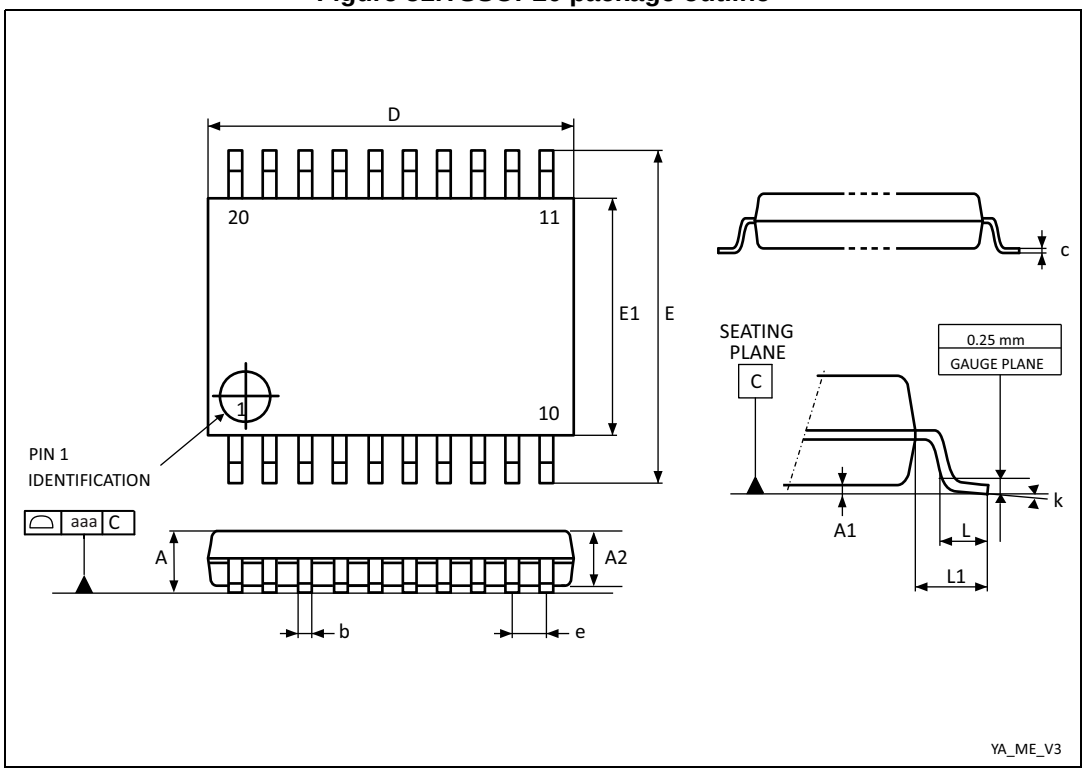


1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.7 TSSOP20 package information

TSSOP20 is a 20-lead thin shrink small-outline, 6.5 x 4.4 mm, 0.65 mm pitch, package.

Figure 51.TSSOP20 package outline



1. Drawing is not to scale.

Table 73. TSSOP20 package mechanical data

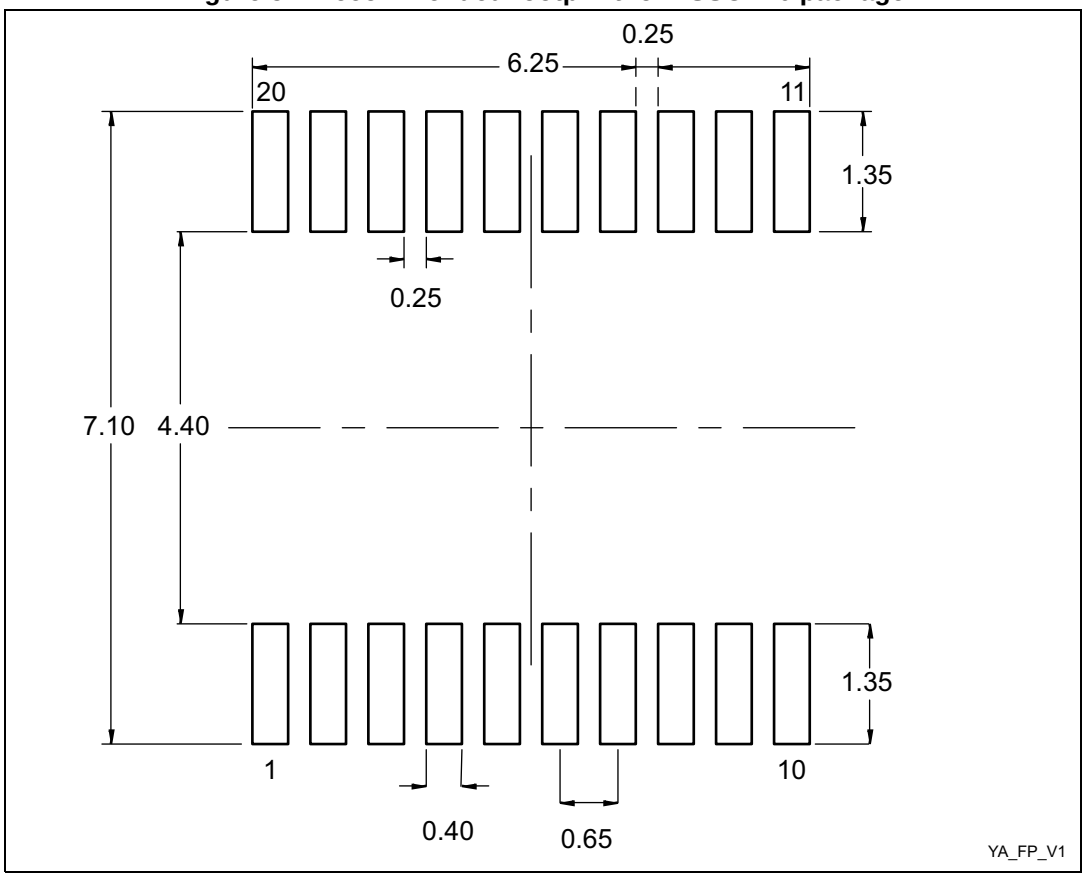
Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.050	-	0.150	0.0020	-	0.0059
A2	0.800	1.000	1.050	0.0315	0.0394	0.0413
b	0.190	-	0.300	0.0075	-	0.0118
c	0.090	-	0.200	0.0035	-	0.0079
D[2]	6.400	6.500	6.600	0.2520	0.2559	0.2598
E	6.200	6.400	6.600	0.2441	0.2520	0.2598
E1[3]	4.300	4.400	4.500	0.1693	0.1732	0.1772
e	-	0.650	-	-	0.0256	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295

Table 73. TSSOP20 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 52. Recommended footprint for TSSOP20 package



1. Dimensions are expressed in millimeters.

7.8 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 21: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 74. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP48 - 7 mm x 7 mm	55	°C/W
	Thermal resistance junction-ambient UFQFPN48 - 7 mm x 7 mm	33	
	Thermal resistance junction-ambient WLCSP36 2.6 mm x 2.7 mm	64	
	Thermal resistance junction-ambient LQFP32 - 7 mm x 7 mm	57	
	Thermal resistance junction-ambient UFQFPN32 - 5 mm x 5 mm	38	
	Thermal resistance junction-ambient UFQFPN28 - 4 mm x 4 mm	118	
	Thermal resistance junction-ambient TSSOP20 - 6.5 mm x 6.4 mm	76	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

9 Revision history

Table 76. Document revision history

Date	Revision	Changes
25-Feb-2014	1	Initial release.
03-Apr-2014	2	Added the sample engineering sections for all the packages in the chapter Package information: **Updated tables:** – STM32F042x4/x6 USART implementation: added one table footnote. – STM32F042x pin definitions, – Current characteristics, – Typical and maximum current consumption from VDD supply at VDD = 3.6 V, – Typical and maximum current consumption from the VDDA supply, – Typical and maximum consumption in Stop and Standby modes, – Typical and maximum current consumption from the VBAT supply, – Typical current consumption, code executing from Flash, running from HSE 8 MHz crystal, – Flash memory characteristics, – I/O static characteristics, – I/O current injection susceptibility, – EMS characteristics, – EMI characteristics, **Updated figures:** – UFQFPN32 32-pin package pinout, – UQFPN28 28-pin package, – Power supply scheme, – TC and TTa I/O input characteristics, – Five volt tolerant (FT and FTf) I/O input characteristics. – LQFP48 marking example (package top view), – UFQFPN48 marking example (package top view), – WLCSP36 marking example (package top view), – LQFP32 marking example (package top view), – UFQFPN28 marking example (package top view), – UFQFPN32 marking example (package top view), – TSSOP20 marking example (package top view)
26-Oct-2015	3	**Cover page:** number of I/Os and timers updated. **Updates in *Section 2: Description*:** – updated *Figure 1: Block diagram* **Updates in *Section 3: Functional overview:*** – updated *Figure 2: Clock tree* – addition of the number of complementary outputs for the advanced control timer and for TIM16, TIM17 general purpose timers in *Table 7: Timer feature comparison* – removal of USART2 from *Figure 3.5.4: Low-power modes*