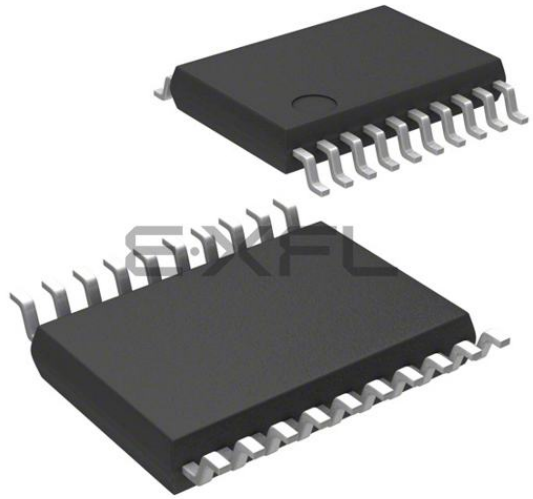

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	16
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f042f6p6

3 Functional overview

Figure 1 shows the general block diagram of the STM32F042x4/x6 devices.

3.1 ARM®-Cortex®-M0 core

The ARM® Cortex®-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM® Cortex®-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F042x4/x6 devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 6 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
  - 16 to 32 Kbytes of embedded Flash memory for programs and data
  - Option bytes

  The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:
  - Level 0: no readout protection
  - Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
  - Level 2: chip readout protection, debug features (Cortex®-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bits are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot pin is shared with the standard GPIO and can be disabled through the boot selector option bits. The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15, or PA9/PA10 or I^2C on pins PB6/PB7 or through the USB DFU interface.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 38 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 10 external and 3 internal (temperature

The RTC is an independent BCD timer/counter. Its main features are the following:

- calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- automatic correction for 28, 29 (leap year), 30, and 31 day of the month
- programmable alarm with wake up from Stop and Standby mode capability
- on-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock
- digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy
- two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection
- timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection
- reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision

The RTC clock sources can be:

- a 32.768 kHz external crystal
- a resonator or oscillator
- the internal low-power RC oscillator (typical frequency of 40 kHz)
- the high-speed external clock divided by 32

3.14 Inter-integrated circuit interface (I^2C)

The I^2C interface (I2C1) can operate in multimaster or slave modes. It can support Standard mode (up to 100 kbit/s), Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

It supports 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). It also includes programmable analog and digital noise filters.

Table 8. Comparison of I^2C analog and digital filters

Aspect	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2Cx peripheral clocks
Benefits	Available in Stop mode	–Extra filtering capability vs. standard requirements –Stable length
Drawbacks	Variations depending on temperature, voltage, process	Wakeup from Stop on address match is not available when digital filter is enabled.

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent

Table 10. STM32F042x4/x6 USART implementation (continued)

USART modes/features(1)	USART1	USART2
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X = supported.

3.16 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I^2S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F042x4/x6 SPI/I^2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I^2S mode	X	-
TI mode	X	X

1. X = supported.

3.17 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.18 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames

with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

3.19 Universal serial bus (USB)

The STM32F042x4/x6 embeds a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB (the last 256 byte are used for CAN peripheral if enabled) and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use an HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal-less operation.

3.20 Clock recovery system (CRS)

The STM32F042x4/x6 embeds a special block which allows automatic trimming of the internal 48 MHz oscillator to guarantee its optimal accuracy over the whole device operational range. This automatic trimming is based on the external synchronization signal, which could be either derived from USB SOF signalization, from LSE oscillator, from an external signal on CRS_SYNC pin or generated by user software. For faster lock-in during startup it is also possible to combine automatic trimming with manual trimming action.

3.21 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}$(1)	Power on/power down reset threshold	Falling edge(2)	1.80	1.88	1.96(3)	V
		Rising edge	1.84(3)	1.92	2.00	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}$(4)	Reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD}.
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

Table 24. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 26* to *Table 28* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 26. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled(1)				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from Flash memory	HSI48	48 MHz	20.3	23.2	23.4	24.6	12.7	14.4	14.4	14.7	mA
		HSE bypass, PLL on	48 MHz	20.2	22.9	23.0	23.9	12.6	14.1	14.3	14.4	
			32 MHz	14.0	16.0	16.1	16.7	8.7	9.5	9.7	10.3	
			24 MHz	11.0	13.5	13.7	13.8	6.9	7.6	7.8	8.2	
		HSE bypass, PLL off	8 MHz	3.9	5.2	5.3	5.6	2.6	3.1	3.2	3.3	
			1 MHz	0.9	1.3	1.5	1.8	0.7	1.0	1.1	1.3	
		HSI clock, PLL on	48 MHz	20.5	23.1	23.3	23.6	12.8	14.6	14.6	15.0	
			32 MHz	14.3	15.6	15.9	17.0	8.6	9.5	9.7	10.0	
			24 MHz	11.2	13.6	13.8	14.8	6.9	7.4	7.5	7.7	
		HSI clock, PLL off	8 MHz	4.1	5.2	5.3	5.6	2.6	3.1	3.1	3.3	

Table 26. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled(1)				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from RAM	HSI48	48 MHz	19.3	21.9	22.1	23.7	11.9	13.4	13.6	13.7	mA
		HSE bypass, PLL on	48 MHz	19.2	21.8(3)	22.0	22.1(3)	11.7	13.3(3)	13.5	13.7(3)	
			32 MHz	13.4	15.8	15.9	16.0	7.9	8.8	8.9	9.7	
			24 MHz	10.3	12.6	13.0	13.4	6.2	8.0	8.2	8.3	
		HSE bypass, PLL off	8 MHz	3.6	4.1	4.3	4.4	2.0	2.1	2.1	2.5	
			1 MHz	0.8	0.9	0.9	1.1	0.4	0.5	0.6	0.8	
		HSI clock, PLL on	48 MHz	19.5	22.0	22.1	22.5	11.8	13.6	13.8	13.9	
			32 MHz	13.5	16.3	16.4	16.6	8.0	8.8	9.1	9.9	
			24 MHz	10.5	12.8	13.0	13.8	6.5	8.0	8.1	8.4	
		HSI clock, PLL off	8 MHz	3.7	4.7	5.0	5.3	2.1	2.3	2.4	3.0	
	Supply current in Sleep mode	HSI48	48 MHz	12.4	15.1	16.3	16.7	3.0	3.2	3.3	3.4	
		HSE bypass, PLL on	48 MHz	12.3	15.0(3)	16.0	16.2(3)	2.9	3.2(3)	3.3	3.4(3)	
			32 MHz	8.5	10.6	11.2	11.7	1.9	2.1	2.2	2.5	
			24 MHz	6.5	8.1	8.5	8.7	1.6	1.8	1.8	1.9	
		HSE bypass, PLL off	8 MHz	2.3	3.0	3.1	3.2	0.7	0.8	0.8	0.9	
			1 MHz	0.4	0.4	0.4	0.6	0.1	0.3	0.3	0.4	
		HSI clock, PLL on	48 MHz	12.4	15.3	15.7	15.9	3.0	3.0	3.2	3.4	
			32 MHz	8.6	10.7	11.3	11.6	2.1	2.2	2.2	2.5	
			24 MHz	6.6	8.4	8.7	8.9	1.6	1.6	1.7	1.9	
		HSI clock, PLL off	8 MHz	2.4	3.2	3.4	3.6	0.6	0.8	0.9	1.0	

1. USB is kept disabled as this IP functions only with a 48 MHz clock.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 32*. The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in *Table 18: Voltage characteristics*

Table 32. Peripheral current consumption

Peripheral		Typical consumption at 25 °C	Unit
AHB	BusMatrix(1)	2.2	µA/MHz
	CRC	1.9	
	DMA	5.1	
	Flash memory interface	15.0	
	GPIOA	8.2	
	GPIOB	7.7	
	GPIOC	2.1	
	GPIOF	1.8	
	SRAM	1.1	
	TSC	4.9	
	All AHB peripherals	**49.8**	

High-speed internal 48 MHz (HSI48) RC oscillator

Table 40. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	Frequency	-	-	48	-	MHz
TRIM	HSI48 user-trimming step	-	0.09(2)	0.14	0.2(2)	%
$DuCy_{(HSI48)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI48}	Accuracy of the HSI48 oscillator (factory calibrated)	T_A = –40 to 105 °C	-4.9(3)	-	4.7(3)	%
		T_A = –10 to 85 °C	-4.1(3)	-	3.7(3)	%
		T_A = 0 to 70 °C	-3.8(3)	-	3.4(3)	%
		T_A = 25 °C	-2.8	-	2.9	%
$t_{su(HSI48)}$	HSI48 oscillator startup time	-	-	-	6(2)	µs
$I_{DDA(HSI48)}$	HSI48 oscillator power consumption	-	-	312	350(2)	µA

1. V_{DDA} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 21. HSI48 oscillator accuracy characterization results

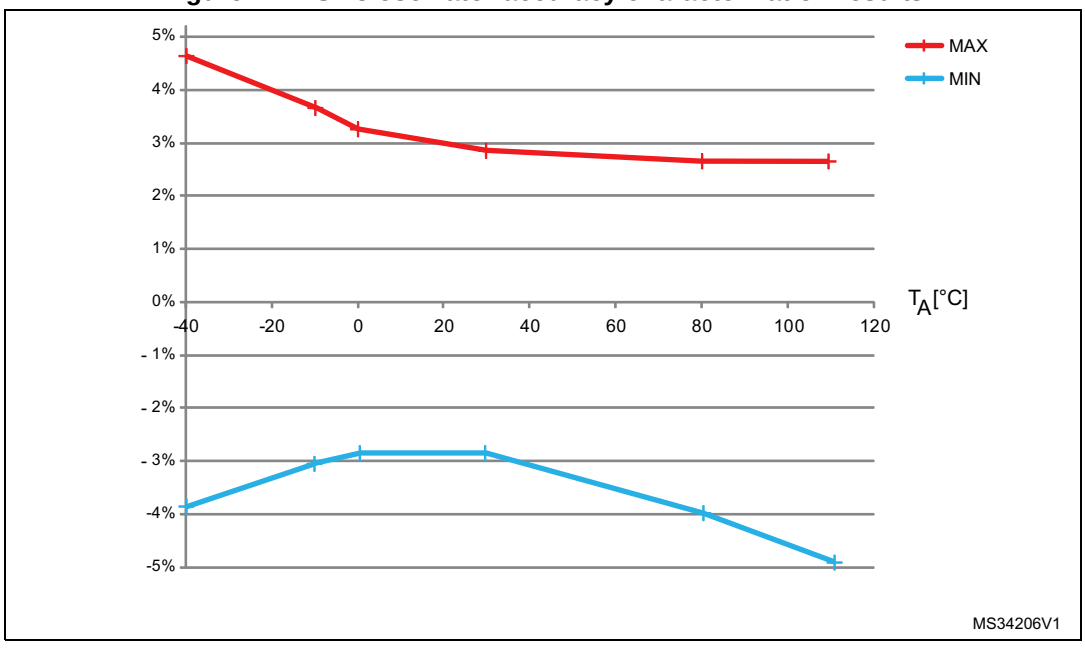


Table 50. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PD}	Weak pull-down equivalent resistor(3)	V_{IN} = - V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 49: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Table 54. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TRIG} (2)	External trigger frequency	f_{ADC} = 14 MHz, 12-bit resolution	-	-	823	kHz
		12-bit resolution	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range	-	0	-	V_{DDA}	V
R_{AIN} (2)	External input impedance	See *Equation 1* and *Table 55* for details	-	-	50	kΩ
R_{ADC} (2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC} (2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL} (2)(3)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
$W_{LATENCY}$ (2)(4)	ADC_DR register ready latency	ADC clock = HSI14	1.5 ADC cycles + 2 f_{PCLK} cycles	-	1.5 ADC cycles + 3 f_{PCLK} cycles	-
		ADC clock = PCLK/2	-	4.5	-	f_{PCLK} cycle
		ADC clock = PCLK/4	-	8.5	-	f_{PCLK} cycle
t_{latr} (2)	Trigger conversion latency	$f_{ADC} = f_{PCLK}/2 = 14$ MHz	0.196			µs
		$f_{ADC} = f_{PCLK}/2$	5.5			$1/f_{PCLK}$
		$f_{ADC} = f_{PCLK}/4 = 12$ MHz	0.219			µs
		$f_{ADC} = f_{PCLK}/4$	10.5			$1/f_{PCLK}$
		$f_{ADC} = f_{HSI14}$ = 14 MHz	0.179	-	0.250	µs
$Jitter_{ADC}$	ADC jitter on trigger conversion	$f_{ADC} = f_{HSI14}$	-	1	-	$1/f_{HSI14}$
t_S (2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB} (2)	Stabilization time	-	14			$1/f_{ADC}$
t_{CONV} (2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz, 12-bit resolution	1	-	18	µs
		12-bit resolution	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_{DDA} and 60 µA on I_{DD} should be taken into account.
2. Guaranteed by design, not tested in production.
3. Specified value includes only ADC timing. It does not include the latency of the register access.
4. This parameter specify latency for transfer of the conversion result to the ADC_DR register. EOC flag is set at this time.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 55. R_{AIN} max for f_{ADC} = 14 MHz

T_S (cycles)	t_S (µs)	R_{AIN} max (kΩ)(1)
1.5	0.11	0.4
7.5	0.54	5.9
13.5	0.96	11.4
28.5	2.04	25.2
41.5	2.96	37.2
55.5	3.96	50
71.5	5.11	NA
239.5	17.1	NA

1. Guaranteed by design, not tested in production.

Table 56. ADC accuracy(1)(2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 3 V to 3.6 V T_A = 25 °C	±1.3	±2	LSB
EO	Offset error		±1	±1.5	
EG	Gain error		±0.5	±1.5	
ED	Differential linearity error		±0.7	±1	
EL	Integral linearity error		±0.8	±1.5	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.7 V to 3.6 V T_A = - 40 to 105 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	
ET	Total unadjusted error	f_{PCLK} = 48 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ V_{DDA} = 2.4 V to 3.6 V T_A = 25 °C	±3.3	±4	LSB
EO	Offset error		±1.9	±2.8	
EG	Gain error		±2.8	±3	
ED	Differential linearity error		±0.7	±1.3	
EL	Integral linearity error		±1.2	±1.7	

1. ADC DC accuracy values are measured after internal calibration.

6.3.17 Temperature sensor characteristics

Table 57. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	± 1	± 2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{30}	Voltage at 30 °C (± 5 °C)(2)	1.34	1.43	1.52	V
t_{START}(1)	ADC_IN16 buffer startup time	-	-	10	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	4	-	-	µs

1. Guaranteed by design, not tested in production.
2. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 3: Temperature sensor calibration values*.

6.3.18 V_{BAT} monitoring characteristics

Table 58. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	2 x 50	-	kΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	–1	-	+1	%
t_{S_vbat}(1)	ADC sampling time when reading the V_{BAT}	4	-	-	µs

1. Guaranteed by design, not tested in production.

6.3.19 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 59. TIMx characteristics

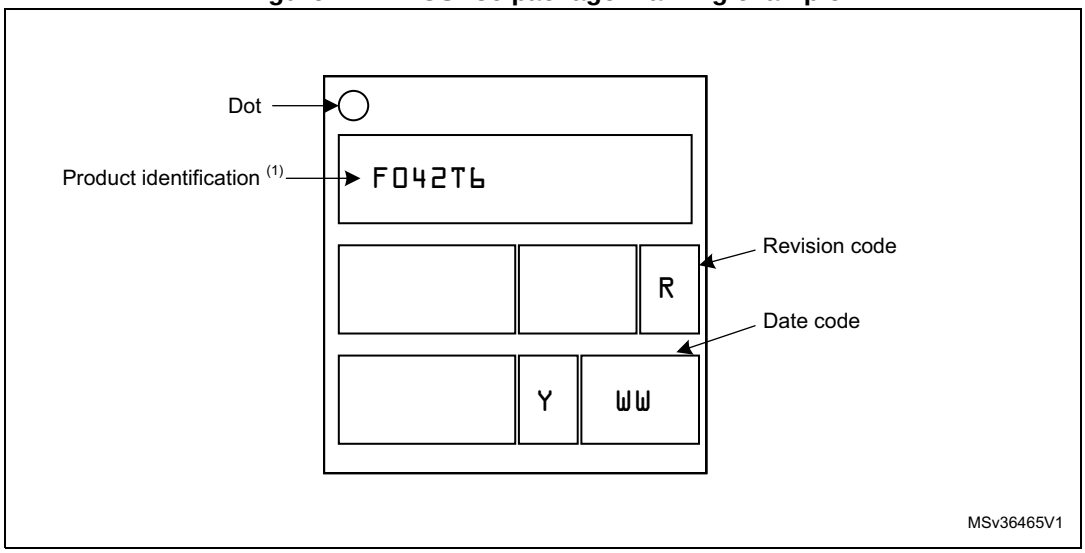
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	-	MHz
t_{MAX_COUNT}	16-bit timer maximum period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	1365	-	µs
	32-bit counter maximum period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	-	s

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 41. WLCSP36 package marking example



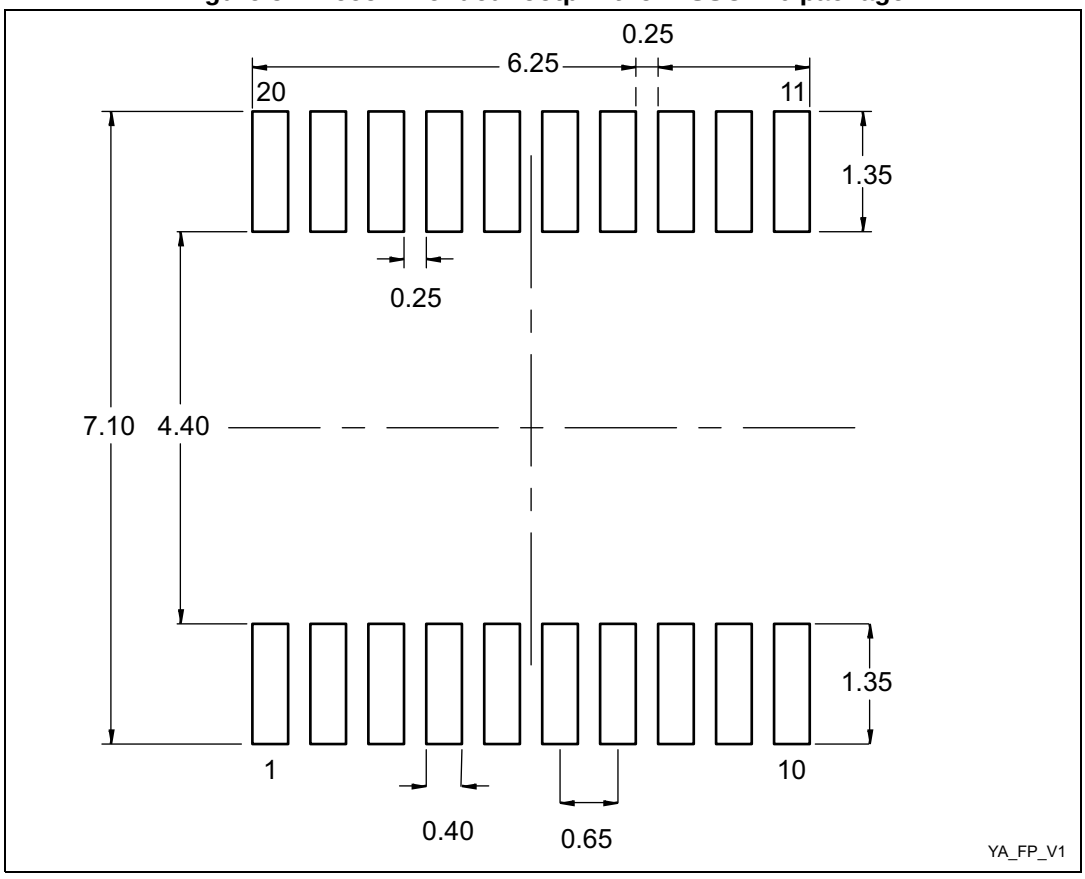
1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

Table 73. TSSOP20 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
L1	-	1.000	-	-	0.0394	-
k	0°	-	8°	0°	-	8°
aaa	-	-	0.100	-	-	0.0039

1. Values in inches are converted from mm and rounded to four decimal digits.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
3. Dimension “E1” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.

Figure 52. Recommended footprint for TSSOP20 package



1. Dimensions are expressed in millimeters.

7.8 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 21: General operating conditions*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 74. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LQFP48 - 7 mm x 7 mm	55	°C/W
	Thermal resistance junction-ambient UFQFPN48 - 7 mm x 7 mm	33	
	Thermal resistance junction-ambient WLCSP36 2.6 mm x 2.7 mm	64	
	Thermal resistance junction-ambient LQFP32 - 7 mm x 7 mm	57	
	Thermal resistance junction-ambient UFQFPN32 - 5 mm x 5 mm	38	
	Thermal resistance junction-ambient UFQFPN28 - 4 mm x 4 mm	118	
	Thermal resistance junction-ambient TSSOP20 - 6.5 mm x 6.4 mm	76	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Section 8: Ordering information*.

9 Revision history

Table 76. Document revision history

Date	Revision	Changes
25-Feb-2014	1	Initial release.
03-Apr-2014	2	Added the sample engineering sections for all the packages in the chapter Package information: **Updated tables:** – STM32F042x4/x6 USART implementation: added one table footnote. – STM32F042x pin definitions, – Current characteristics, – Typical and maximum current consumption from VDD supply at VDD = 3.6 V, – Typical and maximum current consumption from the VDDA supply, – Typical and maximum consumption in Stop and Standby modes, – Typical and maximum current consumption from the VBAT supply, – Typical current consumption, code executing from Flash, running from HSE 8 MHz crystal, – Flash memory characteristics, – I/O static characteristics, – I/O current injection susceptibility, – EMS characteristics, – EMI characteristics, **Updated figures:** – UFQFPN32 32-pin package pinout, – UQFPN28 28-pin package, – Power supply scheme, – TC and TTa I/O input characteristics, – Five volt tolerant (FT and FTf) I/O input characteristics. – LQFP48 marking example (package top view), – UFQFPN48 marking example (package top view), – WLCSP36 marking example (package top view), – LQFP32 marking example (package top view), – UFQFPN28 marking example (package top view), – UFQFPN32 marking example (package top view), – TSSOP20 marking example (package top view)
26-Oct-2015	3	**Cover page:** number of I/Os and timers updated. **Updates in *Section 2: Description*:** – updated *Figure 1: Block diagram* **Updates in *Section 3: Functional overview:*** – updated *Figure 2: Clock tree* – addition of the number of complementary outputs for the advanced control timer and for TIM16, TIM17 general purpose timers in *Table 7: Timer feature comparison* – removal of USART2 from *Figure 3.5.4: Low-power modes*

Table 76. Document revision history (continued)

Date	Revision	Changes
26-Oct-2015	3	– *Table 9: STM32F042x4/x6 I^2C implementation* - adding 20 mA **Updates in *Section 4: Pinouts and pin descriptions*** – *Table 12: Legend/abbreviations used in the pinout table* - removing “I” pin type **Updates in *Section 5: Memory mapping*:** – *Figure 10: STM32F042x6 memory map*, x4 difference described in text **Updates in *Section 6: Electrical characteristics*:** – the condition “Regulator in run mode, all oscillators OFF” in *Table 28: Typical and maximum consumption in Stop and Standby modes*, – footnote for V_{IN} max value in *Table 18: Voltage characteristics,* – footnote for max V_{IN} in *Table 21: General operating conditions*, – t_{START} parameter definition in *Table 25: Embedded internal reference voltage* – addition of t_{START} parameter in *Table 25: Embedded internal reference voltage,* removal of -40°C to 85°C condition and the associated footnote – *Table 26: Typical and maximum current consumption from VDD supply at VDD = 3.6 V:* removing “code executing from Flash or RAM” – removal of the min value for t_{START} parameter in *Table 57: TS characteristics* – the typical value for R parameter in *Table 58: VBAT monitoring characteristics* – removal of Res_{TM} parameter line from *Table 59: TIMx characteristics* and putting all values in new Typ column, substitution of $t_{COUNTER}$ with $t_{MAX\_COUNT,}$ values defined as powers of two – $V_{ESD(CDM)}$ class in *Table 47: ESD absolute maximum ratings* – reorganization of *Table 64: I^2S characteristics* and filling max value of $t_{v(SD\_ST)}$ – adding definition of levels in *Figure 32: I^2S master timing diagram (Philips protocol)* **Updates in *Section 7: Package information***: – heading and display of columns in *Table 68: WLCSP36 package mechanical data*., – *Figure 38: UFQFPN48 package marking example* – *Figure 41: WLCSP36 package marking example* – *Figure 50: UFQFPN28 package marking example* – *Figure 41: WLCSP36 package marking example* – *Figure 51: TSSOP20 package outline* - correcting GAGE to GAUGE – removing “die 445” from *Table 74: Package thermal characteristics* **Updates in *Section 8: Part numbering*:** – adding tray packing to options