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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	28-UFQFN
Supplier Device Package	28-UFQFPN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f042g6u7

Figure 49. Recommended footprint for UFQFPN28 package 106

Figure 50. UFQFPN28 package marking example 107

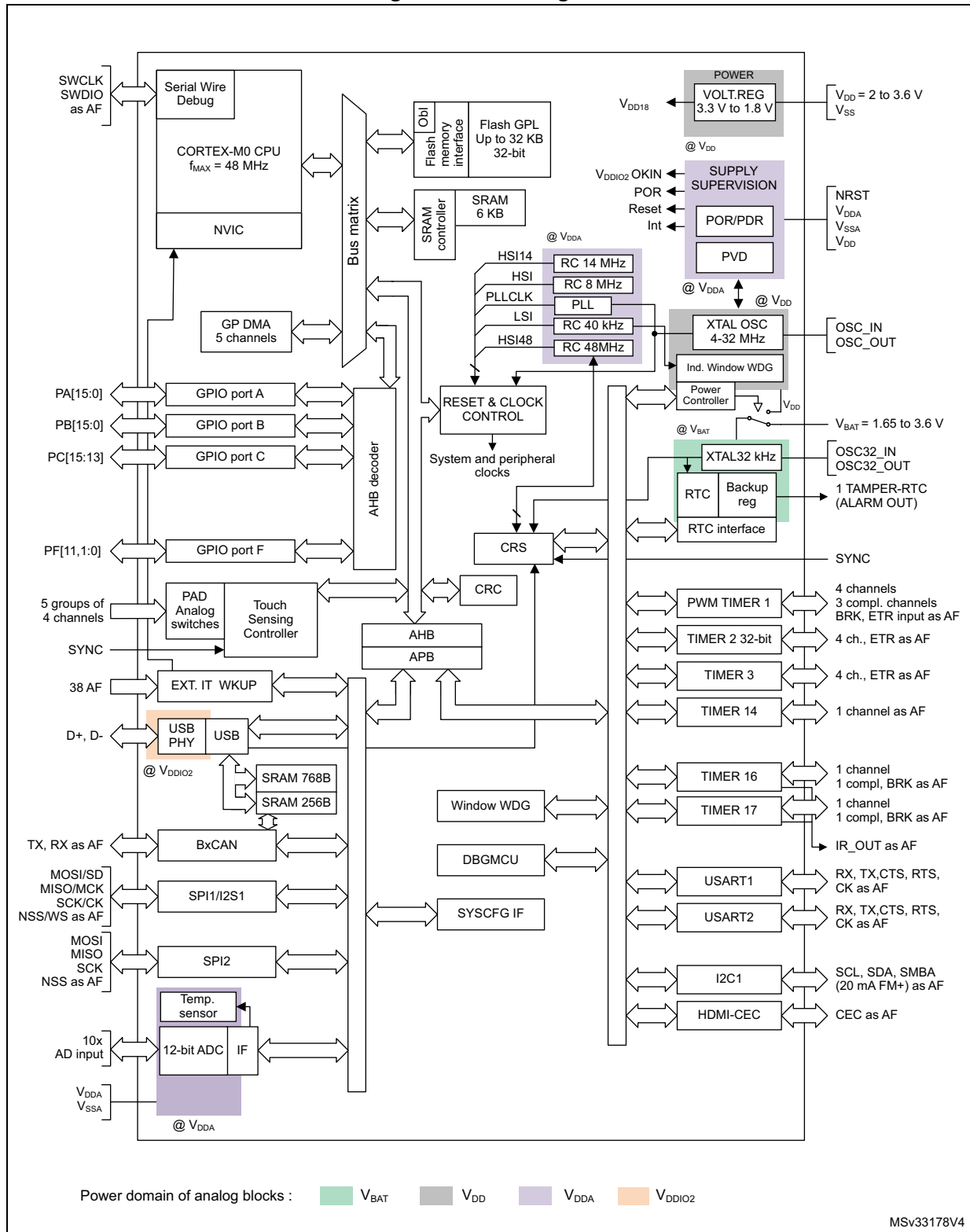
Figure 51. TSSOP20 package outline 108

Figure 52. Recommended footprint for TSSOP20 package 109

Figure 53. TSSOP20 package marking example. 110



Figure 1. Block diagram



3 Functional overview

Figure 1 shows the general block diagram of the STM32F042x4/x6 devices.

3.1 ARM[®]-Cortex[®]-M0 core

The ARM[®] Cortex[®]-M0 is a generation of ARM 32-bit RISC processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M0 processors feature exceptional code-efficiency, delivering the high performance expected from an ARM core, with memory sizes usually associated with 8- and 16-bit devices.

The STM32F042x4/x6 devices embed ARM core and are compatible with all ARM tools and software.

3.2 Memories

The device has the following features:

- 6 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
 - 16 to 32 Kbytes of embedded Flash memory for programs and data
 - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bits are used to select one of the three boot options:

- boot from User Flash memory
- boot from System Memory
- boot from embedded SRAM

The boot pin is shared with the standard GPIO and can be disabled through the boot selector option bits. The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15, or PA9/PA10 or I²C on pins PB6/PB7 or through the USB DFU interface.

can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- input capture
- output compare
- PWM generation (edge or center-aligned modes)
- one-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.12.2 General-purpose timers (TIM2, 3, 14, 16, 17)

There are five synchronizable general-purpose timers embedded in the STM32F042x4/x6 devices (see [Table 7](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F042x4/x6 devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM16 and TIM17

Both timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

They each have a single channel for input capture/output compare, PWM or one-pulse mode output.

4 Pinouts and pin descriptions

Figure 3. LQFP48 package pinout

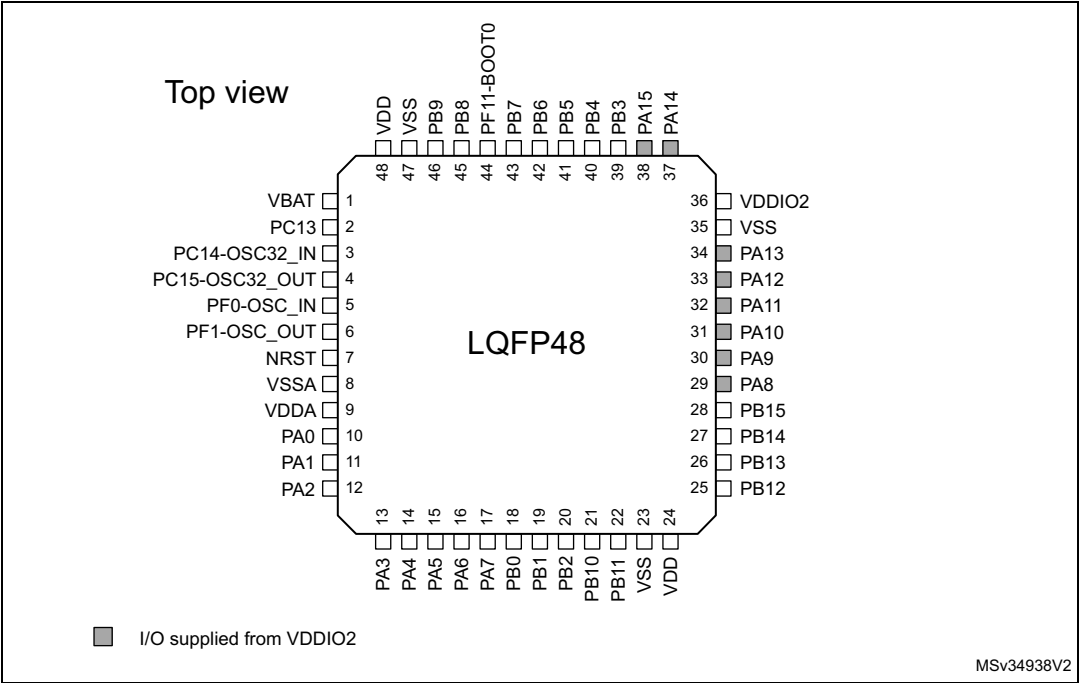


Figure 4. UFQFPN48 package pinout

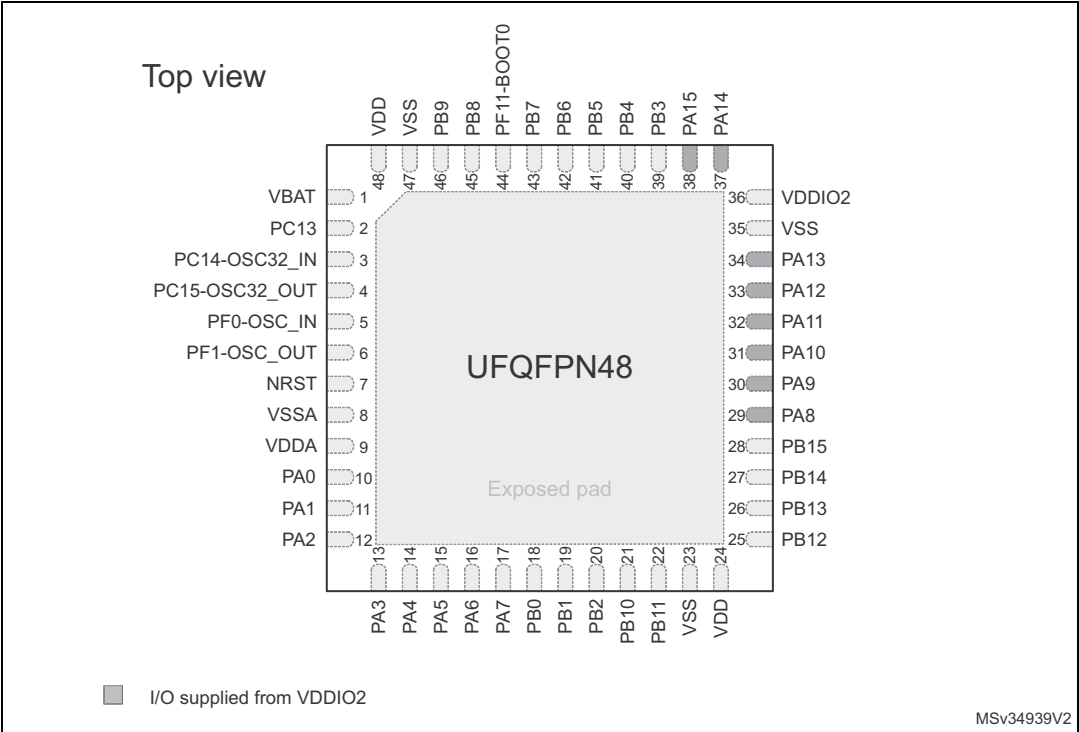


Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
14	C3	10	10	10	10	PA4	I/O	TTa	-	SPI1_NSS, I2S1_WS, TIM14_CH1, TSC_G2_IO1, USART2_CK USB_NOE	ADC_IN4
15	D3	11	11	11	11	PA5	I/O	TTa	-	SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2	ADC_IN5
16	E3	12	12	12	12	PA6	I/O	TTa	-	SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, TSC_G2_IO3, EVENTOUT	ADC_IN6
17	F4	13	13	13	13	PA7	I/O	TTa	-	SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, TSC_G2_IO4, EVENTOUT	ADC_IN7
18	F3	14	14	14	-	PB0	I/O	TTa	-	TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT	ADC_IN8
19	F2	15	15	15	14	PB1	I/O	TTa	-	TIM3_CH4, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3	ADC_IN9
20	D2	-	16	-	-	PB2	I/O	FT	-	TSC_G3_IO4	-
21	-	-	-	-	-	PB10	I/O	FTf	-	SPI2_SCK, CEC, TSC_SYNC, TIM2_CH3, I2C1_SCL	-
22	-	-	-	-	-	PB11	I/O	FTf	-	TIM2_CH4, EVENTOUT, I2C1_SDA	-
23	F1	16	0	16	15	VSS	S	-	-	Ground	
24	-	-	-	17	16	VDD	S	-	-	Digital power supply	
25	-	-	-	-	-	PB12	I/O	FT	-	TIM1_BKIN, SPI2_NSS, EVENTOUT	-

Table 17. STM32F042x4/x6 peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	Reserved
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6800 - 0x4000 6BFF0	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	BxCAN
	0x4000 6000 - 0x4000 63FF	1 KB	USB/CAN RAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 0800 - 0x4000 1FFF	6 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

Table 29. Typical and maximum current consumption from the V_{BAT} supply

Symbol	Parameter	Conditions	Typ @ V _{BAT}						Max ⁽¹⁾			Unit
			1.65 V	1.8 V	2.4 V	2.7 V	3.3 V	3.6 V	T _A = 25 °C	T _A = 85 °C	T _A = 105 °C	
I _{DD_VBAT}	RTC domain supply current	LSE & RTC ON; "Xtal mode": lower driving capability; LSEDRV[1:0] = '00'	0.5	0.5	0.6	0.7	0.9	1.1	1.2	1.5	2.0	μA
		LSE & RTC ON; "Xtal mode" higher driving capability; LSEDRV[1:0] = '11'	0.8	0.9	1.1	1.2	1.4	1.5	1.6	2.0	2.6	

1. Data based on characterization results, not tested in production.

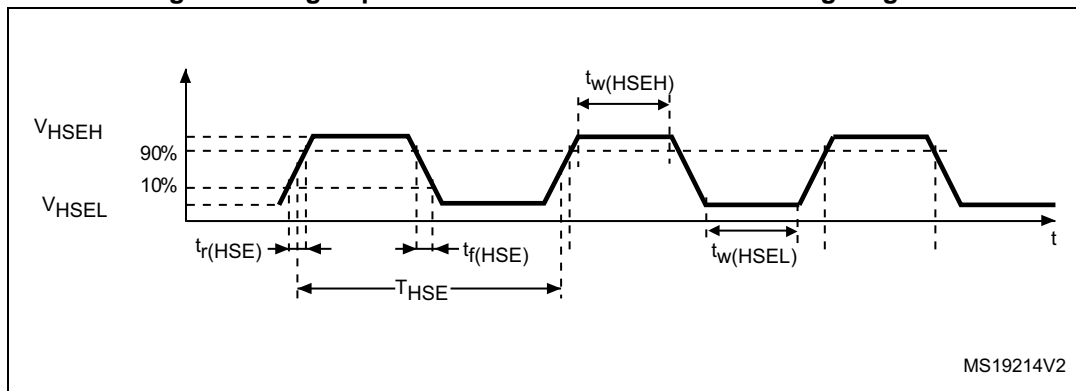
Typical current consumption

The MCU is placed under the following conditions:

- V_{DD} = V_{DDA} = 3.3 V
- All I/O pins are in analog input configuration
- The Flash memory access time is adjusted to f_{HCLK} frequency:
 - 0 wait state and Prefetch OFF from 0 to 24 MHz
 - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, f_{PCLK} = f_{HCLK}
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

1. Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

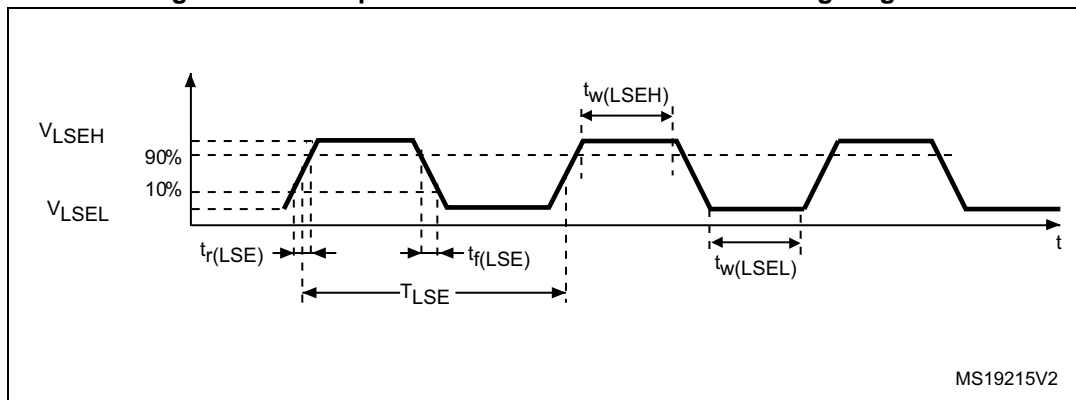
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 16](#).

Table 35. Low-speed external user clock characteristics

Symbol	Parameter ⁽¹⁾	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage	$0.7 V_{DDIOx}$	-	V_{DDIOx}	V
V_{LSEL}	OSC32_IN input pin low level voltage	V_{SS}	-	$0.3 V_{DDIOx}$	
$t_{w(LSEH)}$ $t_{w(LSEL)}$	OSC32_IN high or low time	450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time	-	-	50	

1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram



Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (for example control registers)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 46. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]	Unit
				8/48 MHz	
S_{EMI}	Peak level	$V_{DD} = 3.6\text{ V}$, $T_A = 25\text{ }^{\circ}\text{C}$, LQFP48 package compliant with IEC 61967-2	0.1 to 30 MHz	-9	dB μ V
			30 to 130 MHz	9	
			130 MHz to 1 GHz	17	
			EMI Level	3	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts \times (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Figure 22. TC and TTa I/O input characteristics

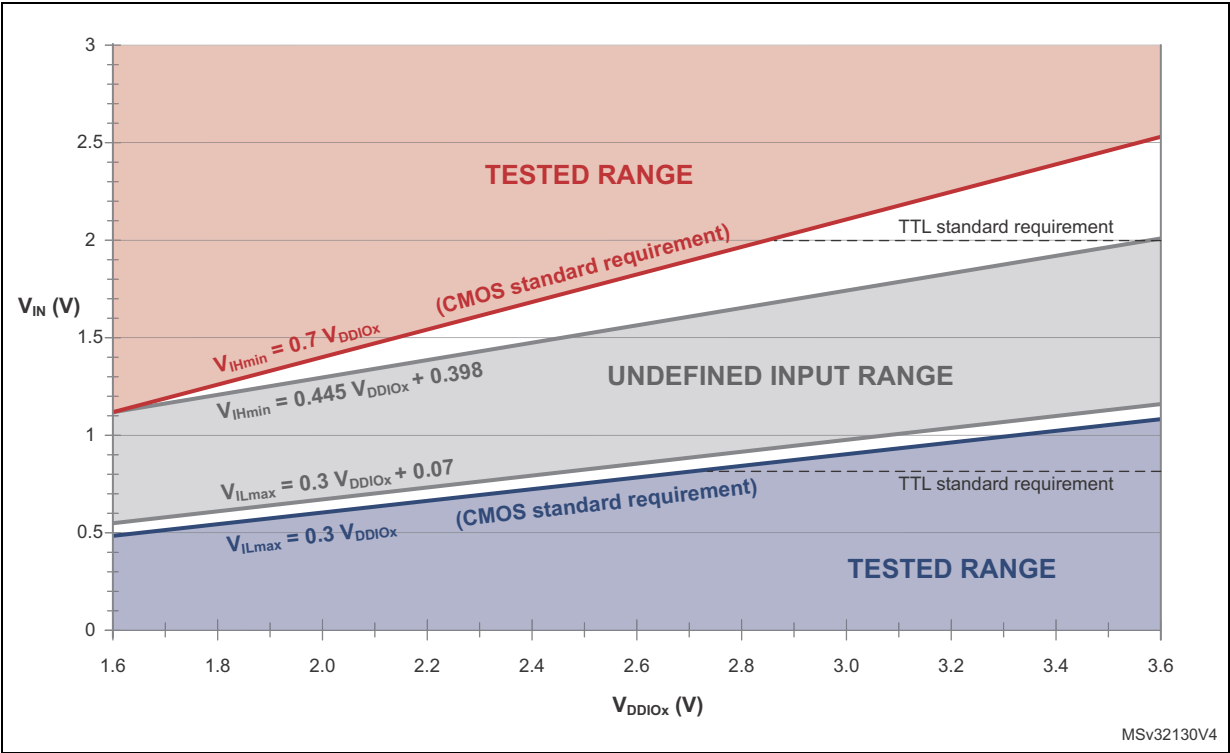


Figure 23. Five volt tolerant (FT and FTf) I/O input characteristics

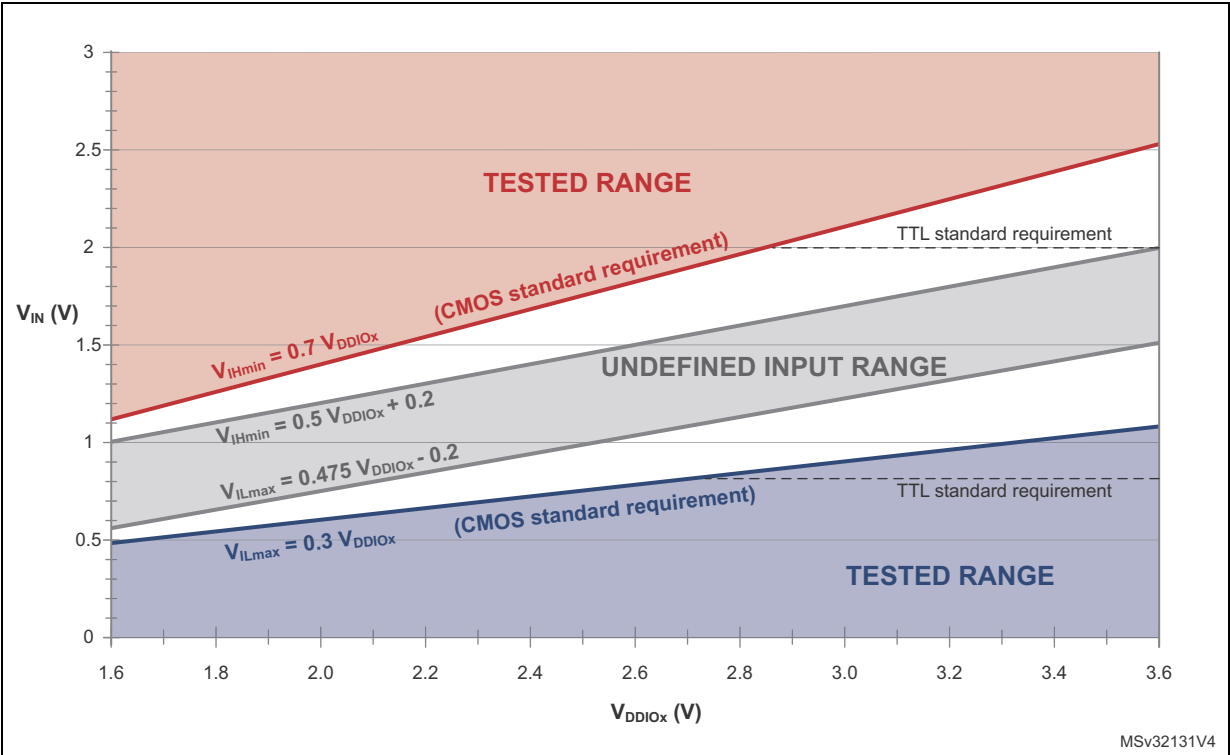
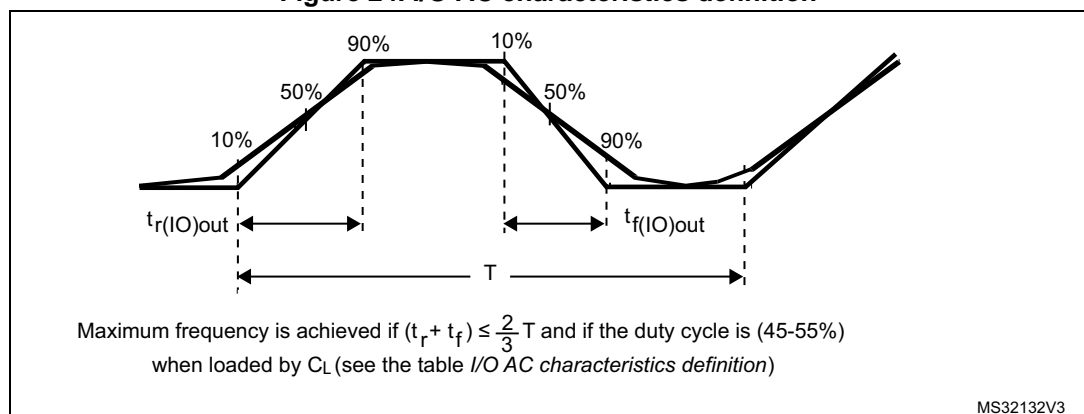


Table 52. I/O AC characteristics⁽¹⁾⁽²⁾ (continued)

OSPEEDRx[1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
Fm+ configuration ⁽⁴⁾	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{\text{DDIOx}} \geq 2 \text{ V}$	-	2	MHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	12	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	34	
	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{\text{DDIOx}} < 2 \text{ V}$	-	0.5	MHz
	$t_{f(\text{IO})\text{out}}$	Output fall time		-	16	ns
	$t_{r(\text{IO})\text{out}}$	Output rise time		-	44	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in [Figure 24](#).
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

Figure 24. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} .

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 53. NRST pin characteristics

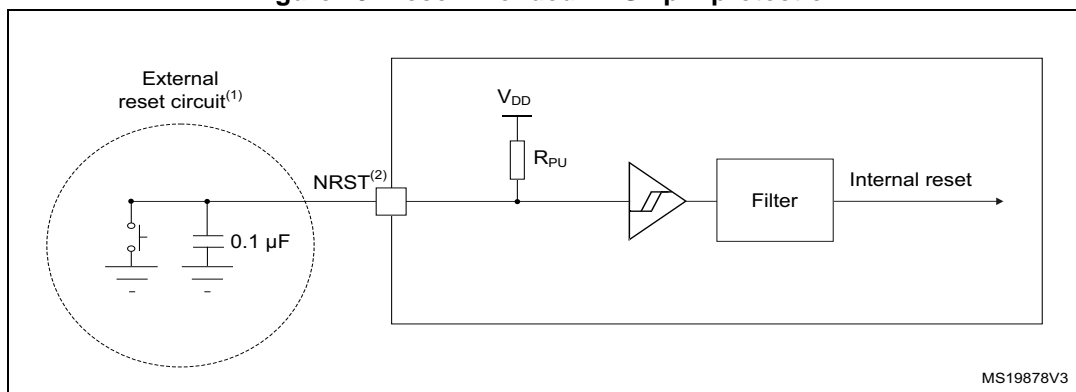
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{IL}(\text{NRST})}$	NRST input low level voltage	-	-	-	$0.3 V_{\text{DD}} + 0.07^{(1)}$	V
$V_{\text{IH}(\text{NRST})}$	NRST input high level voltage	-	$0.445 V_{\text{DD}} + 0.398^{(1)}$	-	-	

Table 53. NRST pin characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{hys(NRST)}}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor ⁽²⁾	$V_{\text{IN}} = V_{\text{SS}}$	25	40	55	k Ω
$V_{\text{F(NRST)}}$	NRST input filtered pulse	-	-	-	100 ⁽¹⁾	ns
$V_{\text{NF(NRST)}}$	NRST input not filtered pulse	$2.7 < V_{\text{DD}} < 3.6$	300 ⁽³⁾	-	-	ns
		$2.0 < V_{\text{DD}} < 3.6$	500 ⁽³⁾	-	-	

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).
3. Data based on design simulation only. Not tested in production.

Figure 25. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{\text{IL(NRST)}}$ max level specified in [Table 53: NRST pin characteristics](#). Otherwise the reset will not be taken into account by the device.

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 54](#) are derived from tests performed under the conditions summarized in [Table 21: General operating conditions](#).

Note: *It is recommended to perform a calibration after each power-up.*

Table 54. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for ADC ON	-	2.4	-	3.6	V
$I_{\text{DDA (ADC)}}$	Current consumption of the ADC ⁽¹⁾	$V_{\text{DDA}} = 3.3 \text{ V}$	-	0.9	-	mA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
$f_{\text{S}}^{(2)}$	Sampling rate	12-bit resolution	0.043	-	1	MHz

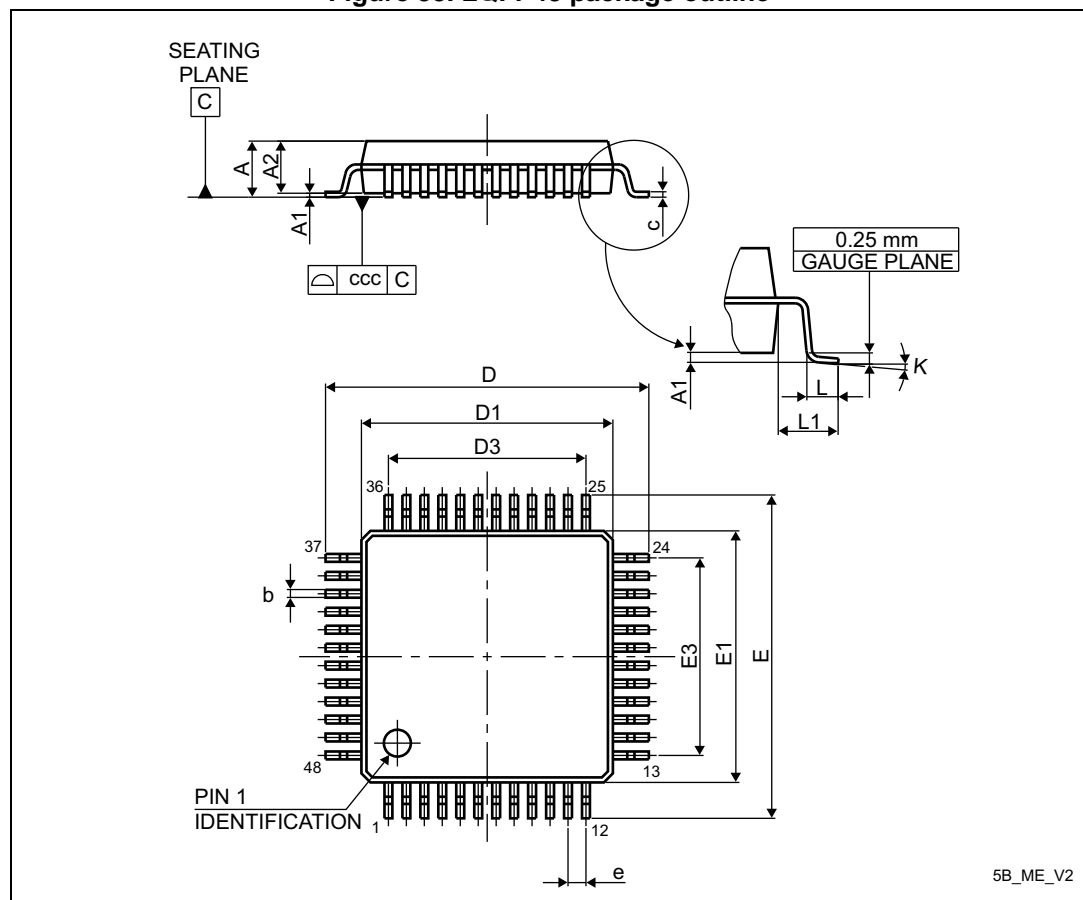
7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.

Figure 33. LQFP48 package outline



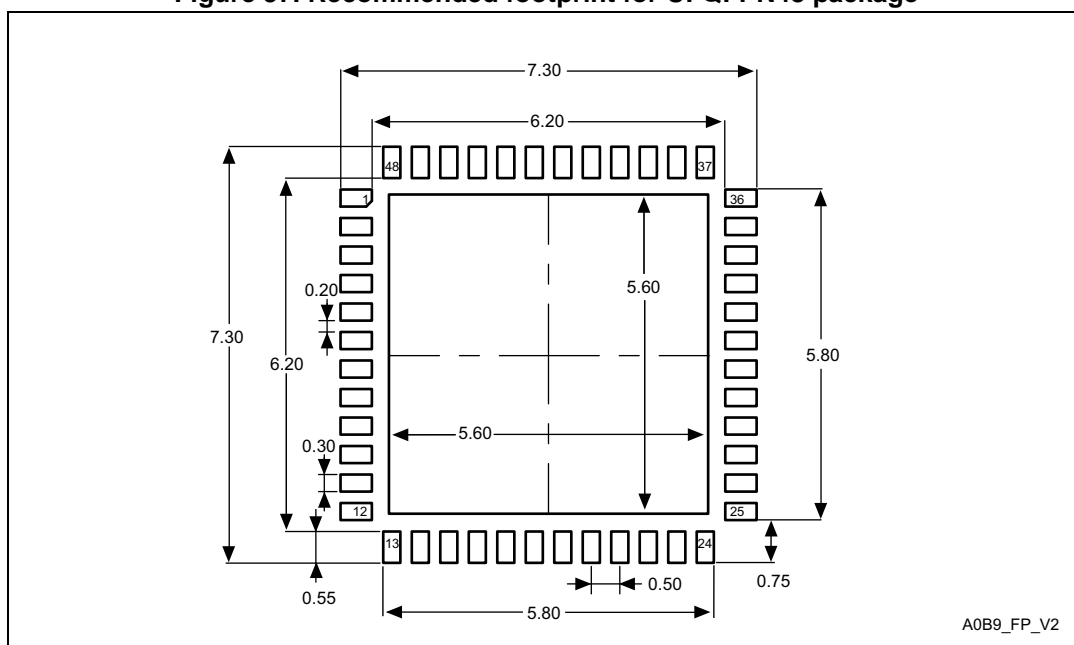
1. Drawing is not to scale.

Table 67. UFQFPN48 package mechanical data

Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 37. Recommended footprint for UFQFPN48 package

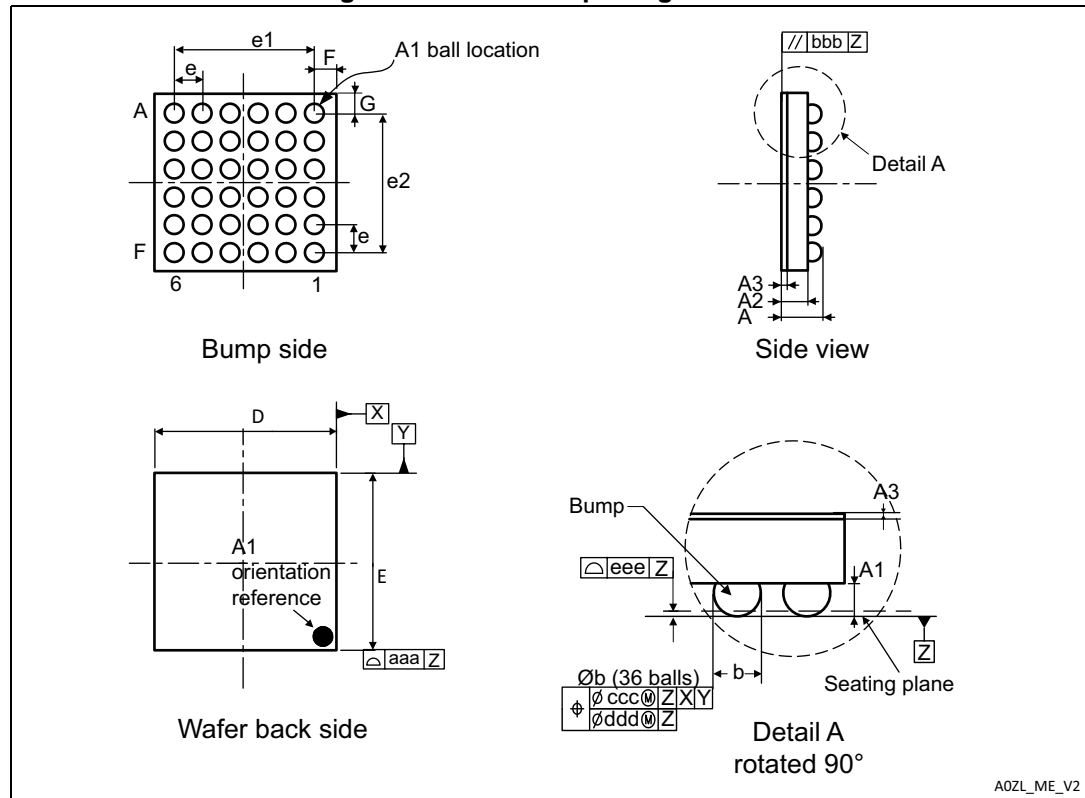


1. Dimensions are expressed in millimeters.

7.3 WLCSP36 package information

WLCSP36 is a 36-ball, 2.605 x 2.703 mm, 0.4 mm pitch wafer-level chip-scale package.

Figure 39. WLCSP36 package outline



A0ZL_ME_V2

1. Drawing is not to scale.

Table 68. WLCSP36 package mechanical data

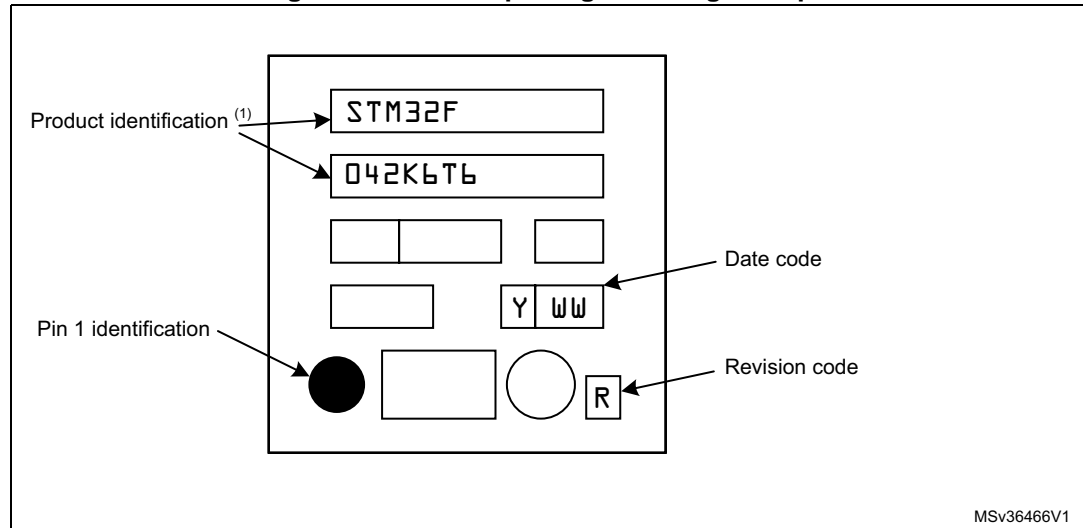
Symbol	millimeters			inches ⁽¹⁾		
	Min	Typ	Max	Min	Typ	Max
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1	-	0.175	-	-	0.0069	-
A2	-	0.380	-	-	0.0150	-
A3 ⁽²⁾	-	0.025	-	-	0.0010	-
b ⁽³⁾	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.570	2.605	2.640	0.1012	0.1026	0.1039
E	2.668	2.703	2.738	0.1050	0.1064	0.1078
e	-	0.400	-	-	0.0157	-
e1	-	2.000	-	-	0.0787	-
e2	-	2.000	-	-	0.0787	-

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which identify the parts throughout supply chain operations, are not indicated below.

Figure 44. LQFP32 package marking example



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

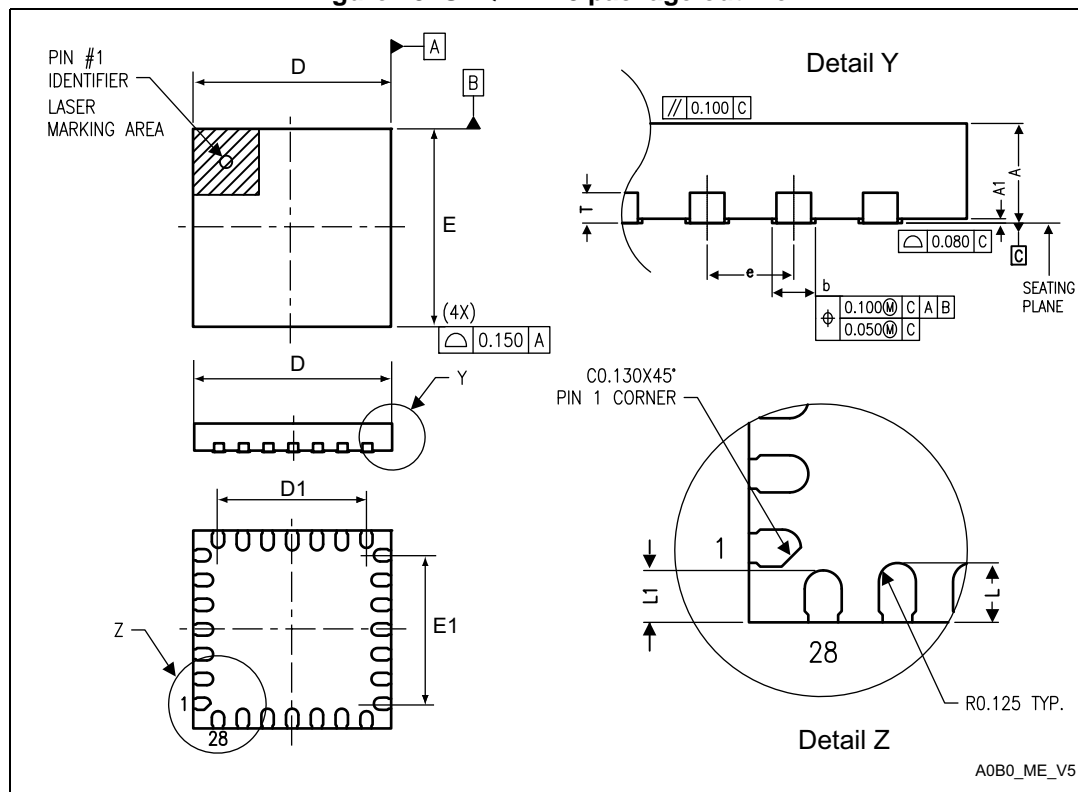
7.5 UFQFPN32 package information

UFQFPN32 is a 32-pin, 5x5 mm, 0.5 mm pitch ultra-thin fine-pitch quad flat package.

7.6 UFQFPN28 package information

UFQFPN28 is a 28-lead, 4x4 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 48. UFQFPN28 package outline



1. Drawing is not to scale.

Table 72. UFQFPN28 package mechanical data⁽¹⁾

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

7.8 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 21: General operating conditions](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max ($P_D \text{ max} = P_{INT} \text{ max} + P_{I/O} \text{ max}$),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 74. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient LQFP48 - 7 mm x 7 mm	55	°C/W
	Thermal resistance junction-ambient UFQFPN48 - 7 mm x 7 mm	33	
	Thermal resistance junction-ambient WLCSP36 2.6 mm x 2.7 mm	64	
	Thermal resistance junction-ambient LQFP32 - 7 mm x 7 mm	57	
	Thermal resistance junction-ambient UFQFPN32 - 5 mm x 5 mm	38	
	Thermal resistance junction-ambient UFQFPN28 - 4 mm x 4 mm	118	
	Thermal resistance junction-ambient TSSOP20 - 6.5 mm x 6.4 mm	76	

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Ordering information](#).

Table 76. Document revision history (continued)

Date	Revision	Changes
26-Oct-2015	3	<ul style="list-style-type: none"> – Table 9: STM32F042x4/x6 I^2C implementation - adding 20 mA Updates in Section 4: Pinouts and pin descriptions – Table 12: Legend/abbreviations used in the pinout table - removing “I” pin type Updates in Section 5: Memory mapping: – Figure 10: STM32F042x6 memory map, x4 difference described in text Updates in Section 6: Electrical characteristics: – the condition “Regulator in run mode, all oscillators OFF” in Table 28: Typical and maximum consumption in Stop and Standby modes, – footnote for V_{IN} max value in Table 18: Voltage characteristics, – footnote for max V_{IN} in Table 21: General operating conditions, – t_{START} parameter definition in Table 25: Embedded internal reference voltage – addition of t_{START} parameter in Table 25: Embedded internal reference voltage, removal of $-40^{\circ}C$ to $85^{\circ}C$ condition and the associated footnote – Table 26: Typical and maximum current consumption from VDD supply at $VDD = 3.6 V$: removing “code executing from Flash or RAM” – removal of the min value for t_{START} parameter in Table 57: TS characteristics – the typical value for R parameter in Table 58: VBAT monitoring characteristics – removal of Res_{TM} parameter line from Table 59: TIMx characteristics and putting all values in new Typ column, substitution of $t_{COUNTER}$ with t_{MAX_COUNT}, values defined as powers of two – $V_{ESD(CDM)}$ class in Table 47: ESD absolute maximum ratings – reorganization of Table 64: I^2S characteristics and filling max value of $t_{V(SD_ST)}$ – adding definition of levels in Figure 32: I^2S master timing diagram (Philips protocol) Updates in Section 7: Package information: – heading and display of columns in Table 68: WLCSP36 package mechanical data., – Figure 38: UFQFPN48 package marking example – Figure 41: WLCSP36 package marking example – Figure 50: UFQFPN28 package marking example – Figure 41: WLCSP36 package marking example – Figure 51: TSSOP20 package outline - correcting GAGE to GAUGE – removing “die 445” from Table 74: Package thermal characteristics Updates in Section 8: Part numbering: – adding tray packing to options