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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I ² C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I ² S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f042k6u6

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2 Description

The STM32F042x4/x6 microcontrollers incorporate the high-performance ARM® Cortex®-M0 32-bit RISC core operating at up to 48 MHz frequency, high-speed embedded memories (up to 32 Kbytes of Flash memory and 6 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (one I²C, two SPIs/one I²S, one HDMI CEC and two USARTs), one USB Full-speed device (crystal-less), one CAN, one 12-bit ADC, four 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F042x4/x6 microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F042x4/x6 microcontrollers include devices in seven different packages ranging from 20 pins to 48 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included.

These features make the STM32F042x4/x6 microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms and HVACs.

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- $V_{DD} = V_{DDIO1} = 2.0$ to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC is used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- $V_{DDIO2} = 1.65$ to 3.6 V: external power supply for marked I/Os. V_{DDIO2} is provided externally through the VDDIO2 pin. The V_{DDIO2} voltage level is completely independent from V_{DD} or V_{DDA} , but it must not be provided without a valid supply on V_{DD} . The V_{DDIO2} supply is monitored and compared with the internal reference voltage (V_{REFINT}). When the V_{DDIO2} is below this threshold, all the I/Os supplied from this rail are disabled by hardware. The output of this comparator is connected to EXTI line 31 and it can be used to generate an interrupt. Refer to the pinout diagrams or tables for concerned I/Os list.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to [Figure 13: Power supply scheme](#).

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD} .
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD} .

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} .

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Additionally, also the internal RC 48 MHz oscillator can be selected for system clock or PLL input source. This oscillator can be automatically fine-trimmed by the means of the CRS peripheral using the external synchronization.

sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{\text{DDA}} = 3.3$ V (± 10 mV)	0x1FFF F7B8 - 0x1FFF F7B9
TS_CAL2	TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{\text{DDA}} = 3.3$ V (± 10 mV)	0x1FFF F7C2 - 0x1FFF F7C3

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT_CAL	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{\text{DDA}} = 3.3$ V (± 10 mV)	0x1FFF F7BA - 0x1FFF F7BB

TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.12.3 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.12.4 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.12.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- a 24-bit down counter
- autoreload capability
- maskable system interrupt generation when the counter reaches 0
- programmable clock source (HCLK or HCLK/8)

3.13 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or at wake up from Standby mode.

Table 13. STM32F042x pin definitions

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
1	-	-	-	-	-	VBAT	S	-	-	Backup power supply	
2	A6	-	-	-	-	PC13	I/O	TC	(1) (2)	-	WKUP2, RTC_TAMP1, RTC_TS, RTC_OUT
3	B6	-	-	-	-	PC14- OSC32_IN (PC14)	I/O	TC	(1) (2)	-	OSC32_IN
4	C6	-	-	-	-	PC15- OSC32_OUT (PC15)	I/O	TC	(1) (2)	-	OSC32_OUT
5	B5	2	2	2	2	PF0-OSC_IN (PF0)	I/O	FTf	-	CRS_SYNC I2C1_SDA	OSC_IN
6	C5	3	3	3	3	PF1-OSC_OUT (PF1)	I/O	FTf	-	I2C1_SCL	OSC_OUT
7	D5	4	4	4	4	NRST	I/O	RST	-	Device reset input / internal reset output (active low)	
8	D6	32	0	16	15	VSSA	S		(3)	Analog ground	
9	E5	5	5	5	5	VDDA	S		-	Analog power supply	
10	F6	6	6	6	6	PA0	I/O	TTa	-	USART2_CTS, TIM2_CH1_ETR, TSC_G1_IO1	RTC_ TAMP2, WKUP1, ADC_IN0,
11	D4	7	7	7	7	PA1	I/O	TTa	-	USART2_RTS, TIM2_CH2, TSC_G1_IO2, EVENTOUT	ADC_IN1
12	E4	8	8	8	8	PA2	I/O	TTa	-	USART2_TX, TIM2_CH3, TSC_G1_IO3	ADC_IN2, WKUP4
13	F5	9	9	9	9	PA3	I/O	TTa	-	USART2_RX, TIM2_CH4, TSC_G1_IO4	ADC_IN3

Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSPOP20					Alternate function	Additional functions
38	A2	25	25	23	-	PA15	I/O	FT	(4)	SPI1_NSS, I2S1_WS, USART2_RX, TIM2_CH1_ETR, EVENTOUT, USB_NOE	-
39	B3	26	26	24	-	PB3	I/O	FT	-	SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT	-
40	A3	27	27	25	-	PB4	I/O	FT	-	SPI1_MISO, I2S1_MCK, TIM17_BKIN, TIM3_CH1, TSC_G5_IO2, EVENTOUT	-
41	E6	28	28	26	-	PB5	I/O	FT	-	SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2	WKUP6
42	C4	29	29	27	-	PB6	I/O	FTf	-	I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_IO3	-
43	A4	30	30	28	-	PB7	I/O	FTf	-	I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4	-
44	-	-	31	-	-	PF11-BOOT0	I/O	FT	-	-	Boot memory selection
-	B4	31	-	1	1	PB8-BOOT0	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	Boot memory selection
45	-	-	32	-	-	PB8	I/O	FTf	-	I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC, CAN_RX	-

Table 13. STM32F042x pin definitions (continued)

Pin numbers						Pin name (function upon reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48/UFQFPN48	WLCSP36	LQFP32	UFQFPN32	UFQFPN28	TSSOP20					Alternate function	Additional functions
46	-	-	-	-	-	PB9	I/O	FTf	-	SPI2_NSS, I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT, CAN_TX	-
47	-	32	0	-	-	VSS	S	-	-	Ground	
48	A5	1	1	-	-	VDD	S	-	-	Digital power supply	

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF.
 - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.
3. Distinct VSSA pin is only available on 48-pin packages. On all other packages, the pin number corresponds to the VSS pin to which VSSA pad of the silicon die is connected.
4. PA8, PA9, PA10, PA11, PA12, PA13, PA14 and PA15 I/Os are supplied by VDDIO2.
5. Pin pair PA11/12 can be remapped in place of pin pair PA9/10 using SYSCFG_CFGR1 register.
6. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

Table 14. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	TIM2_CH1_ETR	TSC_G1_IO1	-	-	-	-
PA1	EVENTOUT	USART2_RTS	TIM2_CH2	TSC_G1_IO2	-	-	-	-
PA2	-	USART2_TX	TIM2_CH3	TSC_G1_IO3	-	-	-	-
PA3	-	USART2_RX	TIM2_CH4	TSC_G1_IO4	-	-	-	-
PA4	SPI1_NSS, I2S1_WS	USART2_CK	USB_NOE	TSC_G2_IO1	TIM14_CH1	-	-	-
PA5	SPI1_SCK, I2S1_CK	CEC	TIM2_CH1_ETR	TSC_G2_IO2	-	-	-	-
PA6	SPI1_MISO, I2S1_MCK	TIM3_CH1	TIM1_BKIN	TSC_G2_IO3	-	TIM16_CH1	EVENTOUT	-
PA7	SPI1_MOSI, I2S1_SD	TIM3_CH2	TIM1_CH1N	TSC_G2_IO4	TIM14_CH1	TIM17_CH1	EVENTOUT	-
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	CRS_SYNC	-	-	-
PA9	-	USART1_TX	TIM1_CH2	TSC_G4_IO1	I2C1_SCL	MCO	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	TSC_G4_IO2	I2C1_SDA	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	TSC_G4_IO3	CAN_RX	I2C1_SCL	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	TSC_G4_IO4	CAN_TX	I2C1_SDA	-	-
PA13	SWDIO	IR_OUT	USB_NOE	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS, I2S1_WS	USART2_RX	TIM2_CH1_ETR	EVENTOUT	-	USB_NOE	-	-

Table 17. STM32F042x4/x6 peripheral register boundary addresses (continued)

Bus	Boundary address	Size	Peripheral
APB	0x4000 7C00 - 0x4000 7FFF	1 KB	Reserved
	0x4000 7800 - 0x4000 7BFF	1 KB	CEC
	0x4000 7400 - 0x4000 77FF	1 KB	Reserved
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	CRS
	0x4000 6800 - 0x4000 6BFF0	1 KB	Reserved
	0x4000 6400 - 0x4000 67FF	1 KB	BxCAN
	0x4000 6000 - 0x4000 63FF	1 KB	USB/CAN RAM
	0x4000 5C00 - 0x4000 5FFF	1 KB	USB
	0x4000 5800 - 0x4000 5BFF	1 KB	Reserved
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4800 - 0x4000 53FF	3 KB	Reserved
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 3C00 - 0x4000 43FF	2 KB	Reserved
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC
	0x4000 2400 - 0x4000 27FF	1 KB	Reserved
	0x4000 2000 - 0x4000 23FF	1 KB	TIM14
	0x4000 0800 - 0x4000 1FFF	6 KB	Reserved
	0x4000 0400 - 0x4000 07FF	1 KB	TIM3
	0x4000 0000 - 0x4000 03FF	1 KB	TIM2

Table 22. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	$\mu\text{s/V}$
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 23](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 23. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}^{(1)}$	Power on/power down reset threshold	Falling edge ⁽²⁾	1.80	1.88	1.96 ⁽³⁾	V
		Rising edge	1.84 ⁽³⁾	1.92	2.00	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}^{(4)}$	Reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD} .
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

Table 24. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V

trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see [Table 32: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

6.3.6 Wakeup time from low-power mode

The wakeup times given in [Table 33](#) are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop or Standby mode, SYSCCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode. The wakeup source from Standby mode is the WKUP1 pin (PA0).

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions..](#)

Table 33. Low-power mode wakeup timings

Symbol	Parameter	Conditions	Typ @VDD = VDDA					Max	Unit
			= 2.0 V	= 2.4 V	= 2.7 V	= 3 V	= 3.3 V		
t _{WUSTOP}	Wakeup from Stop mode	Regulator in run mode	3.2	3.1	2.9	2.9	2.8	5	μs
		Regulator in low power mode	7.0	5.8	5.2	4.9	4.6	9	
t _{WUSTANDBY}	Wakeup from Standby mode	-	60.4	55.6	53.5	52	51	-	
t _{WUSLEEP}	Wakeup from Sleep mode	-	4 SYSCCLK cycles					-	

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

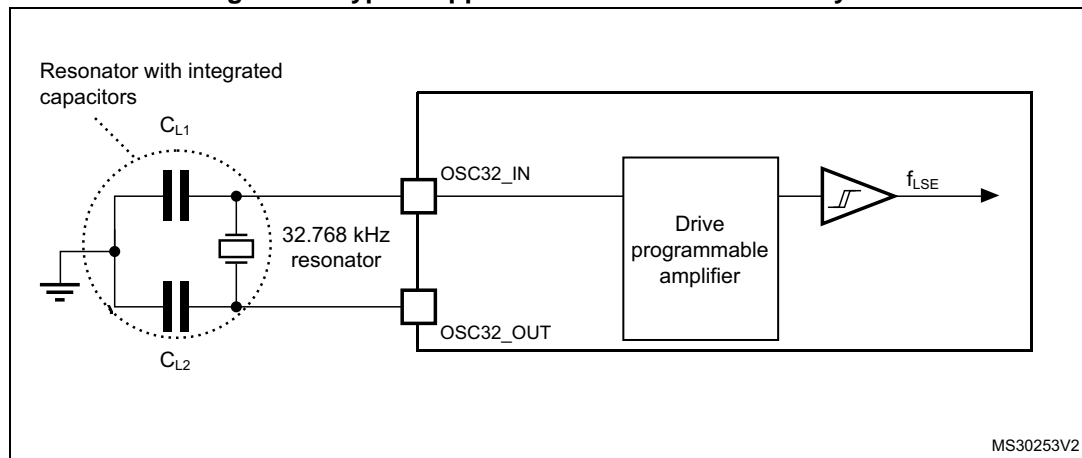
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 15: High-speed external clock source AC timing diagram](#).

Table 34. High-speed external user clock characteristics

Symbol	Parameter ⁽¹⁾	Min	Typ	Max	Unit
f _{HSE_ext}	User external clock source frequency	-	8	32	MHz
V _{HSEH}	OSC_IN input pin high level voltage	0.7 V _{DDIOx}	-	V _{DDIOx}	V
V _{HSEL}	OSC_IN input pin low level voltage	V _{SS}	-	0.3 V _{DDIOx}	
t _{w(HSEH)} t _{w(HSEL)}	OSC_IN high or low time	15	-	-	ns
t _{r(HSE)} t _{f(HSE)}	OSC_IN rise or fall time	-	-	20	

Note: For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between $OSC32_IN$ and $OSC32_OUT$ and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in [Table 38](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#). The provided curves are characterization results, not tested in production.

Figure 22. TC and TTa I/O input characteristics

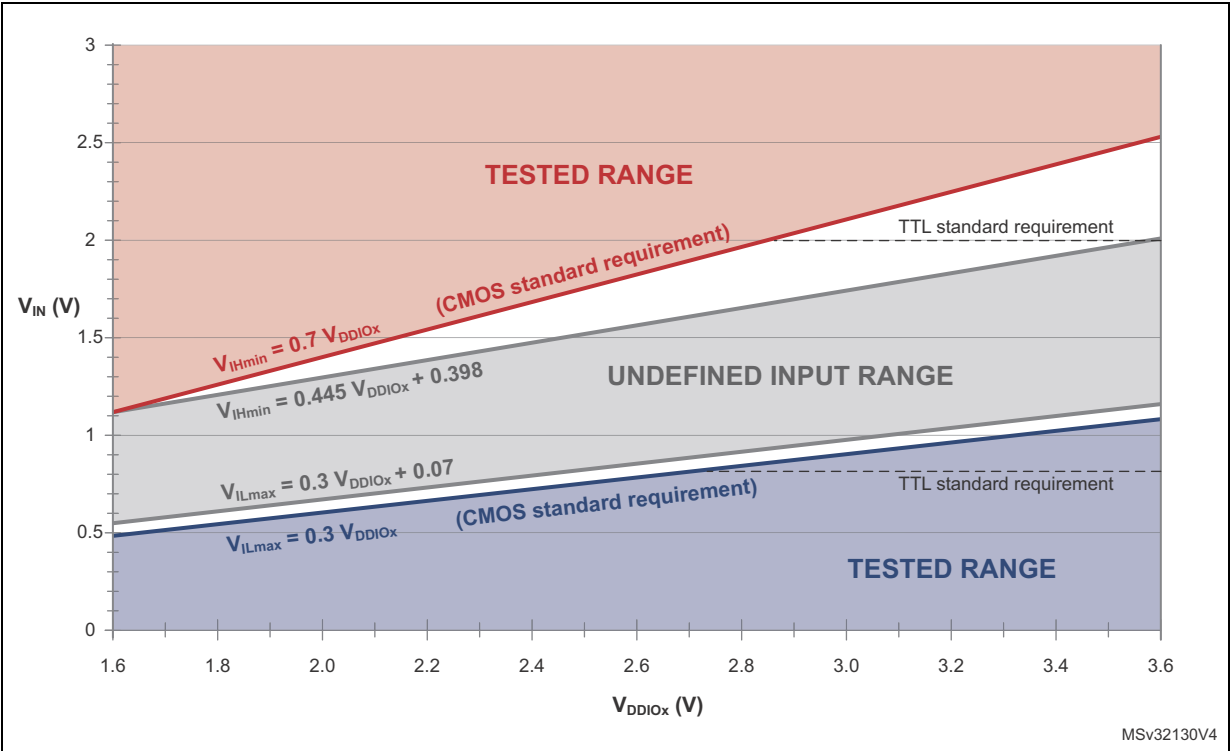
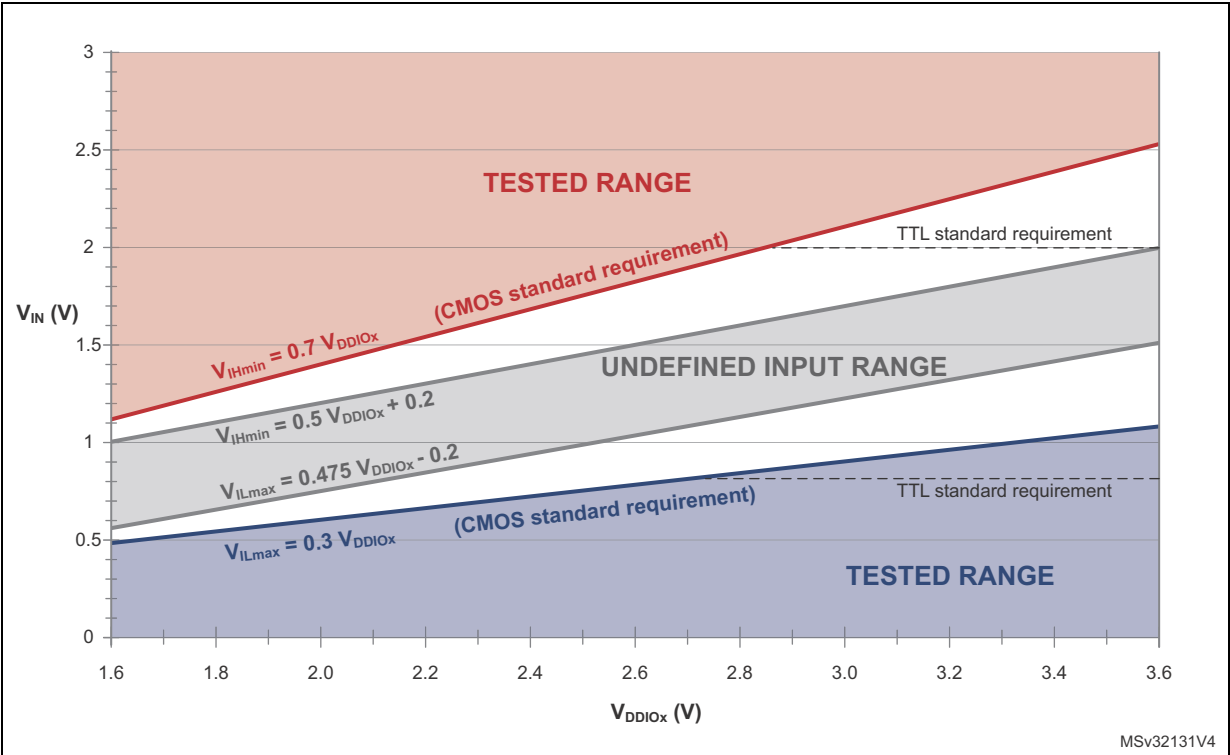


Figure 23. Five volt tolerant (FT and FTf) I/O input characteristics



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 24](#) and [Table 52](#), respectively. Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 21: General operating conditions](#).

Table 52. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Max	Unit
x0	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2 \text{ V}$	-	2	MHz
	$t_{\text{f}(\text{IO})\text{out}}$	Output fall time		-	125	ns
	$t_{\text{r}(\text{IO})\text{out}}$	Output rise time		-	125	
	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2 \text{ V}$	-	1	MHz
	$t_{\text{f}(\text{IO})\text{out}}$	Output fall time		-	125	ns
	$t_{\text{r}(\text{IO})\text{out}}$	Output rise time		-	125	
01	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2 \text{ V}$	-	10	MHz
	$t_{\text{f}(\text{IO})\text{out}}$	Output fall time		-	25	ns
	$t_{\text{r}(\text{IO})\text{out}}$	Output rise time		-	25	
	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2 \text{ V}$	-	4	MHz
	$t_{\text{f}(\text{IO})\text{out}}$	Output fall time		-	62.5	ns
	$t_{\text{r}(\text{IO})\text{out}}$	Output rise time		-	62.5	
11	$f_{\max(\text{IO})\text{out}}$	Maximum frequency ⁽³⁾	$C_L = 30 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	50	MHz
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	30	
			$C_L = 50 \text{ pF}, 2 \text{ V} \leq V_{\text{DDIOx}} < 2.7 \text{ V}$	-	20	
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2 \text{ V}$	-	10	
	$t_{\text{f}(\text{IO})\text{out}}$	Output fall time	$C_L = 30 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	5	ns
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	8	
			$C_L = 50 \text{ pF}, 2 \text{ V} \leq V_{\text{DDIOx}} < 2.7 \text{ V}$	-	12	
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2 \text{ V}$	-	25	
	$t_{\text{r}(\text{IO})\text{out}}$	Output rise time	$C_L = 30 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	5	
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$	-	8	
			$C_L = 50 \text{ pF}, 2 \text{ V} \leq V_{\text{DDIOx}} < 2.7 \text{ V}$	-	12	
			$C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2 \text{ V}$	-	25	

USB characteristics

The STM32F042x4/x6 USB interface is fully compliant with the USB specification version 2.0 and is USB-IF certified (for Full-speed device operation).

Table 65. USB electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
V_{DDIO2}	USB transceiver operating voltage	-	3.0 ⁽¹⁾	-	3.6	V
$t_{STARTUP}^{(2)}$	USB transceiver startup time	-	-	-	1.0	μs
R_{PUI}	Embedded USB_DP pull-up value during idle	-	1.1	1.26	1.5	kΩ
R_{PUR}	Embedded USB_DP pull-up value during reception	-	2.0	2.26	2.6	
$Z_{DRV}^{(2)}$	Output driver impedance ⁽³⁾	Driving high and low	28	40	44	Ω

1. The STM32F042x4/x6 USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics which are degraded in the 2.7-to-3.0 V voltage range.
2. Guaranteed by design, not tested in production.
3. No external termination series resistors are required on USB_DP (D+) and USB_DM (D-); the matching impedance is already included in the embedded driver.

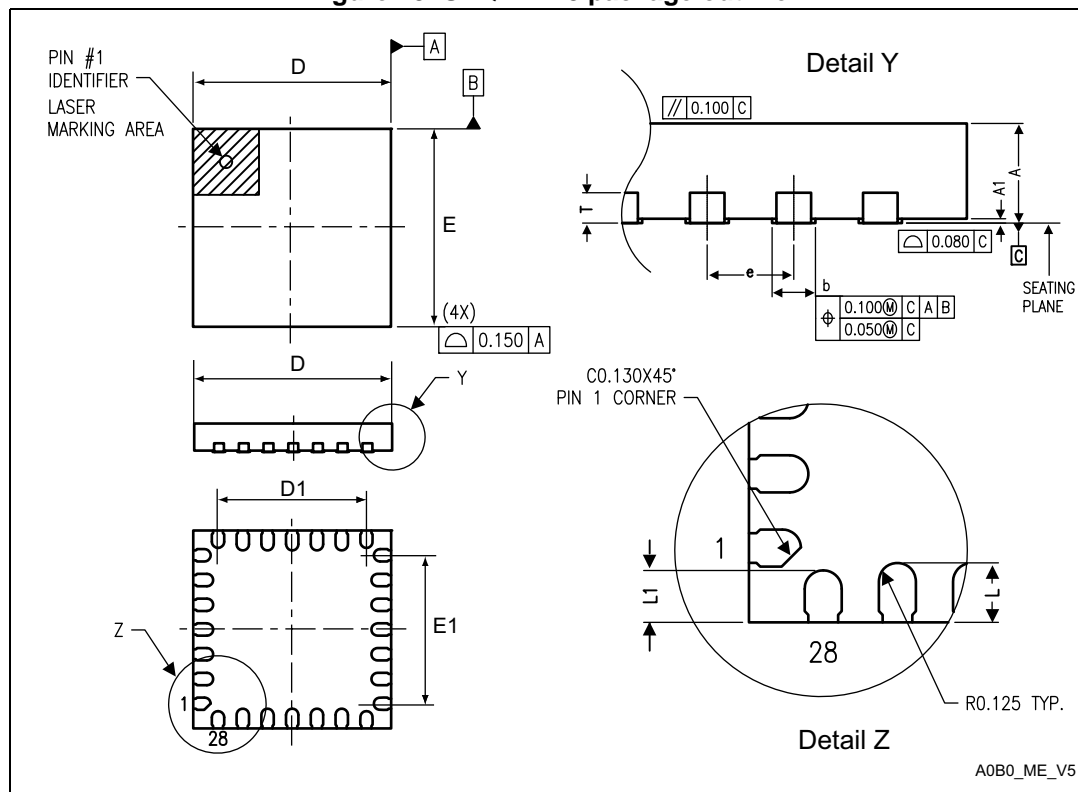
CAN (controller area network) interface

Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

7.6 UFQFPN28 package information

UFQFPN28 is a 28-lead, 4x4 mm, 0.5 mm pitch, ultra-thin fine-pitch quad flat package.

Figure 48. UFQFPN28 package outline



1. Drawing is not to scale.

Table 72. UFQFPN28 package mechanical data⁽¹⁾

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	-	0.000	0.050	-	0.0000	0.0020
D	3.900	4.000	4.100	0.1535	0.1575	0.1614
D1	2.900	3.000	3.100	0.1142	0.1181	0.1220
E	3.900	4.000	4.100	0.1535	0.1575	0.1614
E1	2.900	3.000	3.100	0.1142	0.1181	0.1220
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
L1	0.250	0.350	0.450	0.0098	0.0138	0.0177
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-

8 Ordering information

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 75. Ordering information scheme

Example:	STM32	F	042	C	6	T	6	xxx								
Device family																
STM32 = ARM-based 32-bit microcontroller																
Product type																
F = General-purpose																
Sub-family																
042 = STM32F042xx																
Pin count																
F = 20 pins																
G = 28 pins																
K = 32 pins																
T = 36 pins																
C = 48 pins																
User code memory size																
4 = 16 Kbyte																
6 = 32 Kbyte																
Package																
P = TSSOP																
T = LQFP																
U = UFQFPN																
Y = WLCSP																
Temperature range																
6 = −40 to 85 °C																
7 = −40 to 105 °C																
Options																
xxx = code ID of programmed parts (includes packing type)																
TR = tape and reel packing																
blank = tray packing																