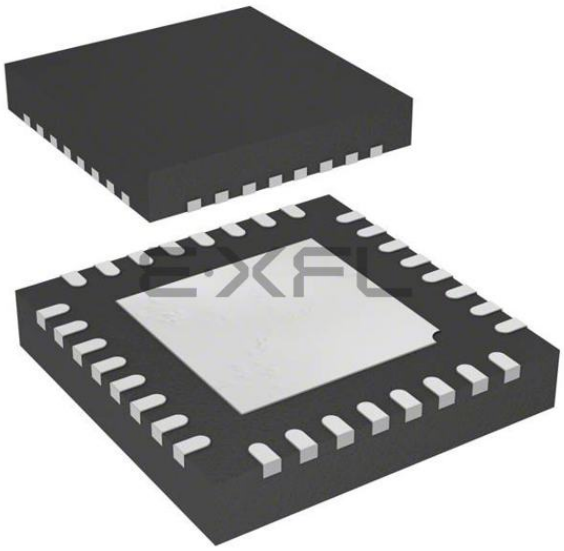

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, HDMI-CEC, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 3.6V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-UFQFPN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f042k6u6tr

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPIx, I2Sx, I2Cx, USARTx, all TIMx timers (except TIM14) and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 38 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog-to-digital converter (ADC)

The 12-bit analog-to-digital converter has up to 10 external and 3 internal (temperature

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA}, and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Touch sensing controller (TSC)

The STM32F042x4/x6 devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 14 capacitive sensing channels distributed over 5 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists in charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate. For operation, one capacitive sensing GPIO in each group is connected to an external capacitor and cannot be used as effective touch sensing channel.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 5. Capacitive sensing GPIOs available on STM32F042x4/x6 devices

Group	Capacitive sensing signal name	Pin name
1	TSC_G1_IO1	PA0
	TSC_G1_IO2	PA1
	TSC_G1_IO3	PA2
	TSC_G1_IO4	PA3
2	TSC_G2_IO1	PA4
	TSC_G2_IO2	PA5
	TSC_G2_IO3	PA6
	TSC_G2_IO4	PA7
3	TSC_G3_IO2	PB0
	TSC_G3_IO3	PB1
	TSC_G3_IO4	PB2
4	TSC_G4_IO1	PA9
	TSC_G4_IO2	PA10
	TSC_G4_IO3	PA11
	TSC_G4_IO4	PA12
5	TSC_G5_IO1	PB3
	TSC_G5_IO2	PB4
	TSC_G5_IO3	PB6
	TSC_G5_IO4	PB7

from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C peripheral can be served by the DMA controller.

Table 9. STM32F042x4/x6 I²C implementation

I²C features(1)	I2C1
7-bit addressing mode	X
10-bit addressing mode	X
Standard mode (up to 100 kbit/s)	X
Fast mode (up to 400 kbit/s)	X
Fast Mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)	X
Independent clock	X
SMBus	X
Wakeup from STOP	X

1. X = supported.

3.15 Universal synchronous/asynchronous receiver/transmitter (USART)

The device embeds two universal synchronous/asynchronous receivers/transmitters (USART1, USART2) which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent of the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

Table 10. STM32F042x4/x6 USART implementation

USART modes/features(1)	USART1	USART2
Hardware flow control for modem	X	X
Continuous communication using DMA	X	X
Multiprocessor communication	X	X
Synchronous mode	X	X
Smartcard mode	X	-
Single-wire half-duplex communication	X	X
IrDA SIR ENDEC block	X	-
LIN mode	X	-
Dual clock domain and wakeup from Stop mode	X	-
Receiver timeout interrupt	X	-

Table 10. STM32F042x4/x6 USART implementation (continued)

USART modes/features(1)	USART1	USART2
Modbus communication	X	-
Auto baud rate detection	X	-
Driver Enable	X	X

1. X = supported.

3.16 Serial peripheral interface (SPI) / Inter-integrated sound interface (I^2S)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I^2S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F042x4/x6 SPI/I^2S implementation

SPI features(1)	SPI1	SPI2
Hardware CRC calculation	X	X
Rx/Tx FIFO	X	X
NSS pulse mode	X	X
I^2S mode	X	-
TI mode	X	X

1. X = supported.

3.17 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.18 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames

Figure 7. UFQFPN32 package pinout

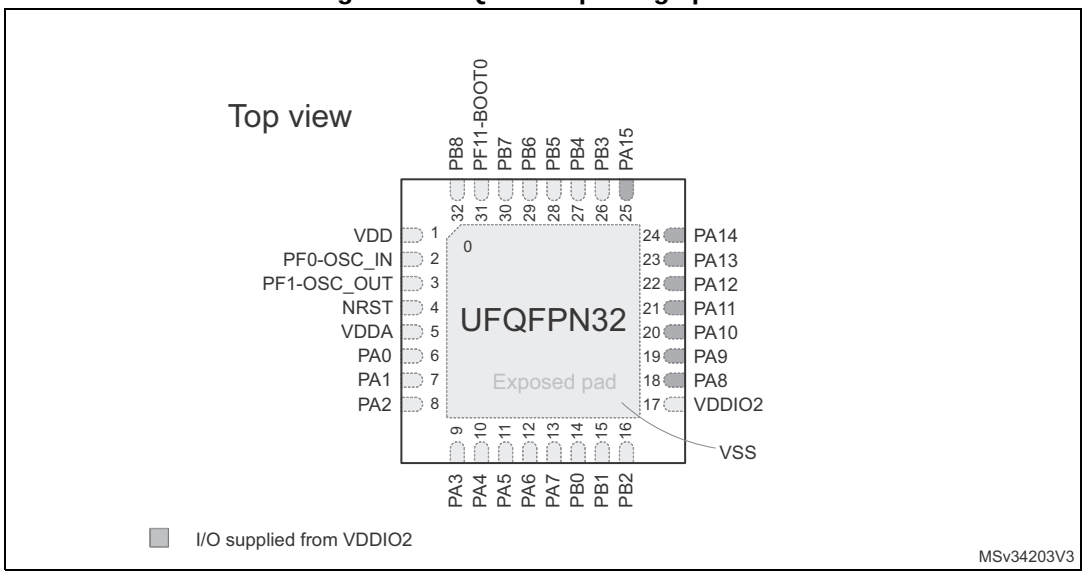
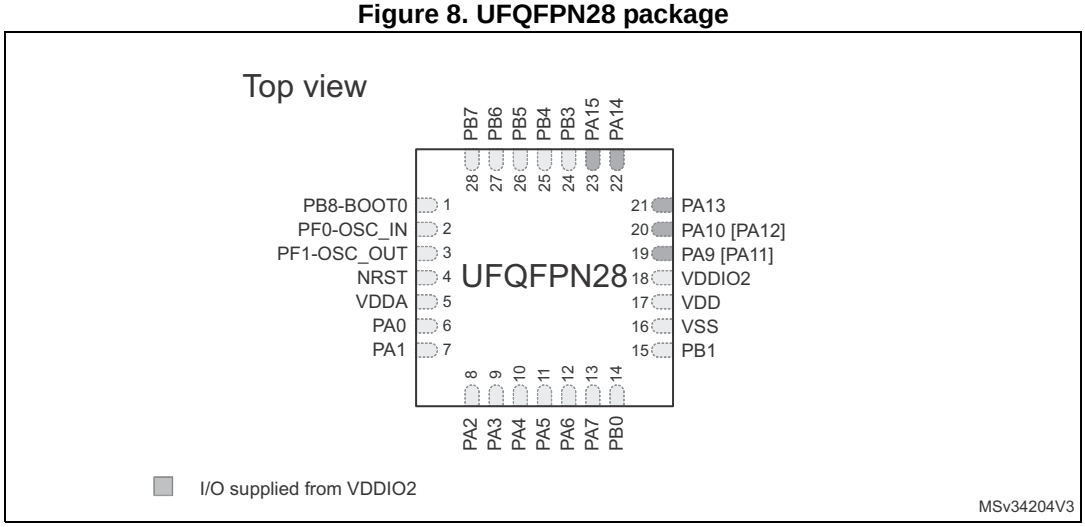


Figure 8. UFQFPN28 package



1. Pin pair PA11/12 can be remapped in place of pin pair PA9/10 using the SYSCFG_CFGR1 register.

6.3 Operating conditions

6.3.1 General operating conditions

Table 21. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2.0	3.6	V
V_{DDIO2}	I/O supply voltage	Must not be supplied if V_{DD} is not present	1.65	3.6	V
V_{DDA}	Analog operating voltage (ADC not used)	Must have a potential equal to or higher than V_{DD}	V_{DD}	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	V_{DDIOx}+0.3	V
		TTa I/O	-0.3	V_{DDA}+0.3(1)	
		FT and FTf I/O	-0.3	5.5(1)	
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(2)	LQFP48	-	364	mW
		UFQFPN48	-	606	
		WLCSP36	-	313	
		LQFP32	-	351	
		UFQFPN32	-	526	
		UFQFPN28	-	170	
		TSSOP20	-	263	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low power dissipation(3)	–40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	–40	105	°C
		Low power dissipation(3)	–40	125	
T_J	Junction temperature range	Suffix 6 version	–40	105	°C
		Suffix 7 version	–40	125	

1. For operation with a voltage higher than V_{DDIOx} + 0.3 V, the internal pull-up resistor must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax}. See *Section 7.8: Thermal characteristics*.
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.8: Thermal characteristicsSection 7.8: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 22* are derived from tests performed under the ambient temperature condition summarized in *Table 21*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency:
  - 0 wait state and Prefetch OFF from 0 to 24 MHz
  - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 26* to *Table 28* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 26. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V

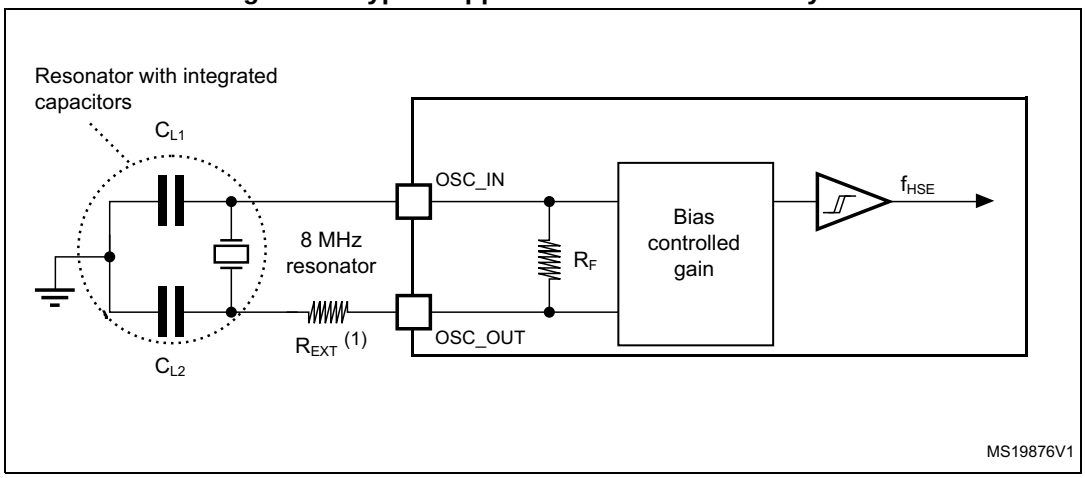
Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled(1)				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from Flash memory	HSI48	48 MHz	20.3	23.2	23.4	24.6	12.7	14.4	14.4	14.7	mA
		HSE bypass, PLL on	48 MHz	20.2	22.9	23.0	23.9	12.6	14.1	14.3	14.4	
			32 MHz	14.0	16.0	16.1	16.7	8.7	9.5	9.7	10.3	
			24 MHz	11.0	13.5	13.7	13.8	6.9	7.6	7.8	8.2	
		HSE bypass, PLL off	8 MHz	3.9	5.2	5.3	5.6	2.6	3.1	3.2	3.3	
			1 MHz	0.9	1.3	1.5	1.8	0.7	1.0	1.1	1.3	
		HSI clock, PLL on	48 MHz	20.5	23.1	23.3	23.6	12.8	14.6	14.6	15.0	
			32 MHz	14.3	15.6	15.9	17.0	8.6	9.5	9.7	10.0	
			24 MHz	11.2	13.6	13.8	14.8	6.9	7.4	7.5	7.7	
		HSI clock, PLL off	8 MHz	4.1	5.2	5.3	5.6	2.6	3.1	3.1	3.3	

Table 26. Typical and maximum current consumption from V_{DD} supply at V_{DD} = 3.6 V (continued)

Symbol	Parameter	Conditions	f_{HCLK}	All peripherals enabled(1)				All peripherals disabled				Unit
				Typ	Max @ T_A(2)			Typ	Max @ T_A(2)			
					25 °C	85 °C	105 °C		25 °C	85 °C	105 °C	
I_{DD}	Supply current in Run mode, code executing from RAM	HSI48	48 MHz	19.3	21.9	22.1	23.7	11.9	13.4	13.6	13.7	mA
		HSE bypass, PLL on	48 MHz	19.2	21.8(3)	22.0	22.1(3)	11.7	13.3(3)	13.5	13.7(3)	
			32 MHz	13.4	15.8	15.9	16.0	7.9	8.8	8.9	9.7	
			24 MHz	10.3	12.6	13.0	13.4	6.2	8.0	8.2	8.3	
		HSE bypass, PLL off	8 MHz	3.6	4.1	4.3	4.4	2.0	2.1	2.1	2.5	
			1 MHz	0.8	0.9	0.9	1.1	0.4	0.5	0.6	0.8	
		HSI clock, PLL on	48 MHz	19.5	22.0	22.1	22.5	11.8	13.6	13.8	13.9	
			32 MHz	13.5	16.3	16.4	16.6	8.0	8.8	9.1	9.9	
			24 MHz	10.5	12.8	13.0	13.8	6.5	8.0	8.1	8.4	
		HSI clock, PLL off	8 MHz	3.7	4.7	5.0	5.3	2.1	2.3	2.4	3.0	
	Supply current in Sleep mode	HSI48	48 MHz	12.4	15.1	16.3	16.7	3.0	3.2	3.3	3.4	
		HSE bypass, PLL on	48 MHz	12.3	15.0(3)	16.0	16.2(3)	2.9	3.2(3)	3.3	3.4(3)	
			32 MHz	8.5	10.6	11.2	11.7	1.9	2.1	2.2	2.5	
			24 MHz	6.5	8.1	8.5	8.7	1.6	1.8	1.8	1.9	
		HSE bypass, PLL off	8 MHz	2.3	3.0	3.1	3.2	0.7	0.8	0.8	0.9	
			1 MHz	0.4	0.4	0.4	0.6	0.1	0.3	0.3	0.4	
		HSI clock, PLL on	48 MHz	12.4	15.3	15.7	15.9	3.0	3.0	3.2	3.4	
			32 MHz	8.6	10.7	11.3	11.6	2.1	2.2	2.2	2.5	
			24 MHz	6.6	8.4	8.7	8.9	1.6	1.6	1.7	1.9	
		HSI clock, PLL off	8 MHz	2.4	3.2	3.4	3.6	0.6	0.8	0.9	1.0	

1. USB is kept disabled as this IP functions only with a 48 MHz clock.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 37. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)

Symbol	Parameter	Conditions(1)	Min(2)	Typ	Max(2)	Unit
I_{DD}	LSE current consumption	low drive capability	-	0.5	0.9	µA
		medium-low drive capability	-	-	1	
		medium-high drive capability	-	-	1.3	
		high drive capability	-	-	1.6	
g_m	Oscillator transconductance	low drive capability	5	-	-	µA/V
		medium-low drive capability	8	-	-	
		medium-high drive capability	15	-	-	
		high drive capability	25	-	-	
$t_{SU(LSE)}$(3)	Startup time	V_{DDIOx} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Table 44. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min(1)	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycle
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Year
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycle(2) at T_A = 55 °C	20	

1. Data based on characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports). the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB**: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in *Table 45*. They are based on the EMS levels and classes defined in application note AN1709.

Table 45. EMS characteristics

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-2	3B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP48, T_A = +25°C, f_{HCLK} = 48 MHz, conforming to IEC 61000-4-4	4B

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Table 49. I/O current injection susceptibility

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
I_{INJ}	Injected current on PA12 pin	-0	+5	mA
	Injected current on PA9, PB3, PB13, PF11 pins with induced leakage current on adjacent pins less than 50 µA	-5	NA	
	Injected current on PB0, PB1 and all other FT and FTf pins	-5	NA	
	Injected current on all other TC, TTa and RST pins	-5	+5	

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under the conditions summarized in *Table 21: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Table 50. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	TC and TTa I/O	-	-	$0.3\ V_{DDIOx}+0.07$(1)	V
		FT and FTf I/O	-	-	$0.475\ V_{DDIOx}-0.2$(1)	
		All I/Os	-	-	$0.3\ V_{DDIOx}$	
V_{IH}	High level input voltage	TC and TTa I/O	$0.445\ V_{DDIOx}+0.398$(1)	-	-	V
		FT and FTf I/O	$0.5\ V_{DDIOx}+0.2$(1)	-	-	
		All I/Os	$0.7\ V_{DDIOx}$	-	-	
V_{hys}	Schmitt trigger hysteresis	TC and TTa I/O	-	200(1)	-	mV
		FT and FTf I/O	-	100(1)	-	
I_{lkg}	Input leakage current(2)	TC, FT and FTf I/O TTa in digital mode $V_{SS} \le V_{IN} \le V_{DDIOx}$	-	-	± 0.1	µA
		TTa in digital mode $V_{DDIOx} \le V_{IN} \le V_{DDA}$	-	-	1	
		TTa in analog mode $V_{SS} \le V_{IN} \le V_{DDA}$	-	-	± 0.2	
		FT and FTf I/O $V_{DDIOx} \le V_{IN} \le 5$ V	-	-	10	
R_{PU}	Weak pull-up equivalent resistor (3)	$V_{IN} = V_{SS}$	25	40	55	kΩ

Table 50. I/O static characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PD}	Weak pull-down equivalent resistor(3)	V_{IN} = - V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Data based on design simulation only. Not tested in production.
2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to *Table 49: I/O current injection susceptibility*.
3. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 22* for standard I/Os, and in *Figure 23* for 5 V-tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 22. TC and TTa I/O input characteristics

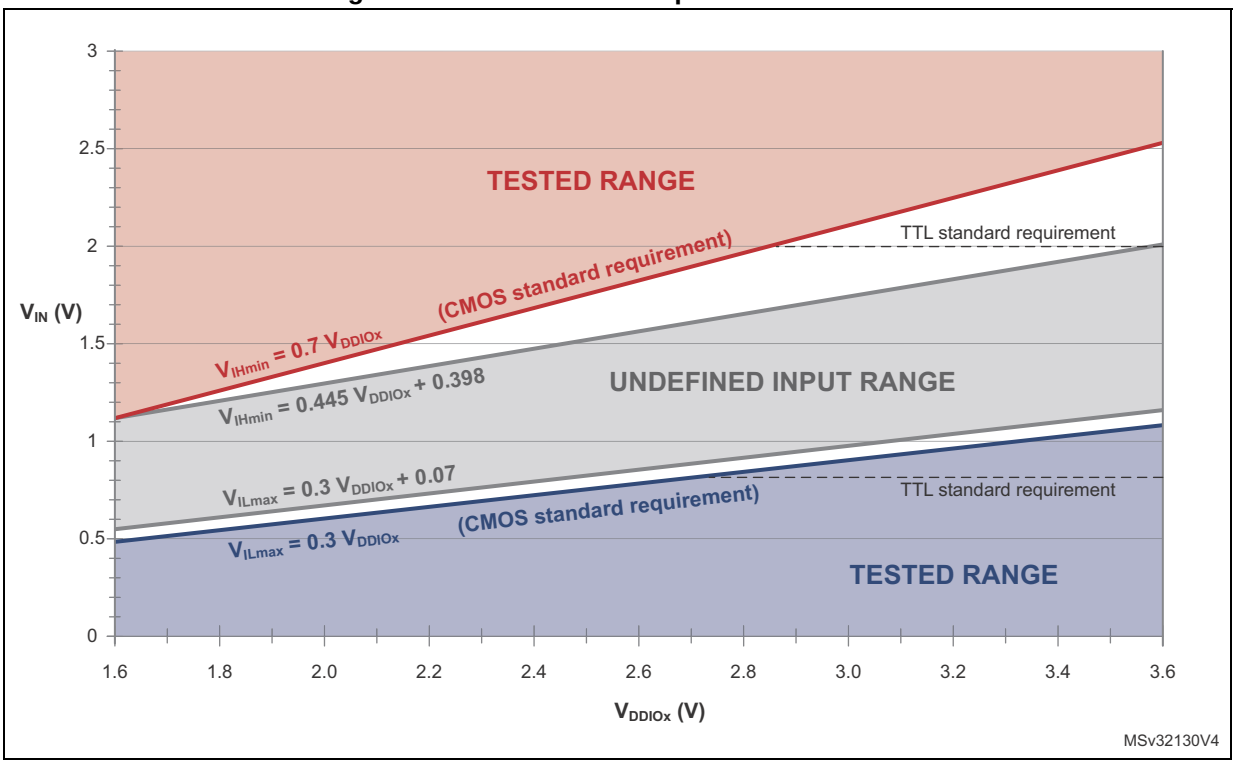


Figure 23. Five volt tolerant (FT and FTf) I/O input characteristics

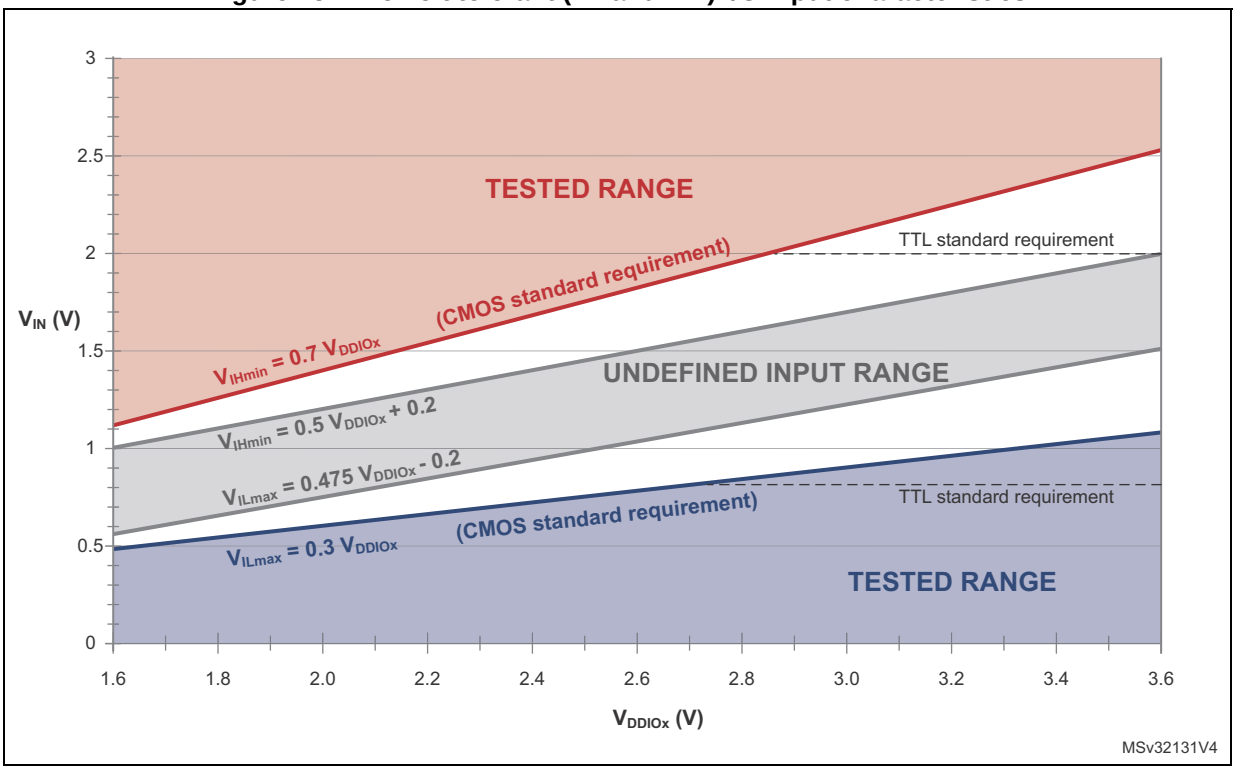
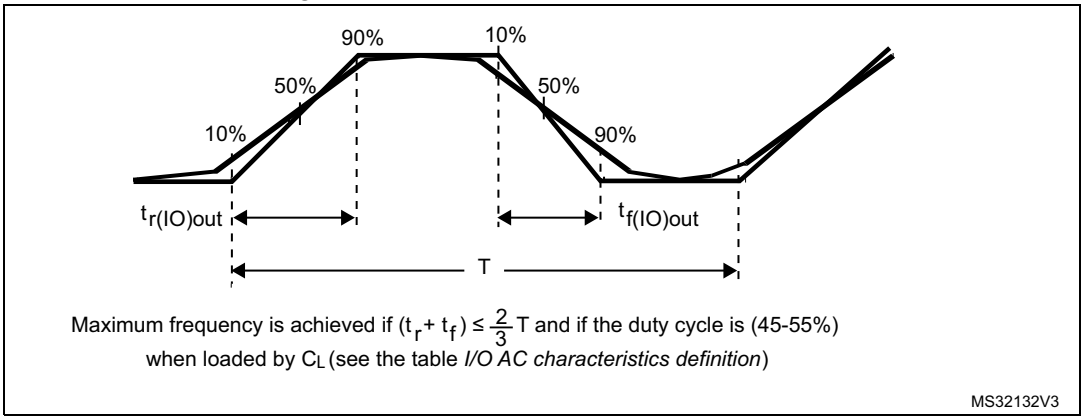


Table 52. I/O AC characteristics(1)(2) (continued)

OSPEEDRy [1:0] value(1)	Symbol	Parameter	Conditions	Min	Max	Unit
Fm+ configuration (4)	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} \geq 2$ V	-	2	MHz
	$t_{f(IO)out}$	Output fall time		-	12	ns
	$t_{r(IO)out}$	Output rise time		-	34	
	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, $V_{DDIOx} < 2$ V	-	0.5	MHz
	$t_{f(IO)out}$	Output fall time		-	16	ns
	$t_{r(IO)out}$	Output rise time		-	44	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in *Figure 24*.
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

Figure 24. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU}.

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 21: General operating conditions*.

Table 53. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	-	-	-	$0.3\ V_{DD}+0.07$(1)	V
$V_{IH(NRST)}$	NRST input high level voltage	-	$0.445\ V_{DD}+0.398$(1)	-	-	

6.3.17 Temperature sensor characteristics

Table 57. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	± 1	± 2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{30}	Voltage at 30 °C (± 5 °C)(2)	1.34	1.43	1.52	V
t_{START}(1)	ADC_IN16 buffer startup time	-	-	10	µs
t_{S_temp}(1)	ADC sampling time when reading the temperature	4	-	-	µs

1. Guaranteed by design, not tested in production.
2. Measured at V_{DDA} = 3.3 V ± 10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 3: Temperature sensor calibration values*.

6.3.18 V_{BAT} monitoring characteristics

Table 58. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	2 x 50	-	kΩ
Q	Ratio on V_{BAT} measurement	-	2	-	-
Er(1)	Error on Q	–1	-	+1	%
t_{S_vbat}(1)	ADC sampling time when reading the V_{BAT}	4	-	-	µs

1. Guaranteed by design, not tested in production.

6.3.19 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to *Section 6.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 59. TIMx characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	20.8	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	-	$f_{TIMxCLK}/2$	-	MHz
		$f_{TIMxCLK}$ = 48 MHz	-	24	-	MHz
t_{MAX_COUNT}	16-bit timer maximum period	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	1365	-	µs
	32-bit counter maximum period	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 48 MHz	-	89.48	-	s

Table 60. IWDG min/max timeout period at 40 kHz (LSI)(1)

Prescaler divider	PR[2:0] bits	Min timeout RL[11:0]= 0x000	Max timeout RL[11:0]= 0xFFF	Unit
/4	0	0.1	409.6	ms
/8	1	0.2	819.2	
/16	2	0.4	1638.4	
/32	3	0.8	3276.8	
/64	4	1.6	6553.6	
/128	5	3.2	13107.2	
/256	6 or 7	6.4	26214.4	

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 61. WWDG min/max timeout value at 48 MHz (PCLK)

Prescaler	WDGTB	Min timeout value	Max timeout value	Unit
1	0	0.0853	5.4613	ms
2	1	0.1706	10.9226	
4	2	0.3413	21.8453	
8	3	0.6826	43.6906	

6.3.20 Communication interfaces

I^2C interface characteristics

The I^2C interface meets the timings requirements of the I^2C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I^2C timings requirements are guaranteed by design when the I2Cx peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to *Section 6.3.14: I/O port characteristics* for the I^2C I/Os characteristics.

All I^2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 68. WLCSP36 package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
F	-	0.3025	-	-	0.0119	-
G	-	0.3515	-	-	0.0138	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 40. Recommended pad footprint for WLCSP36 package

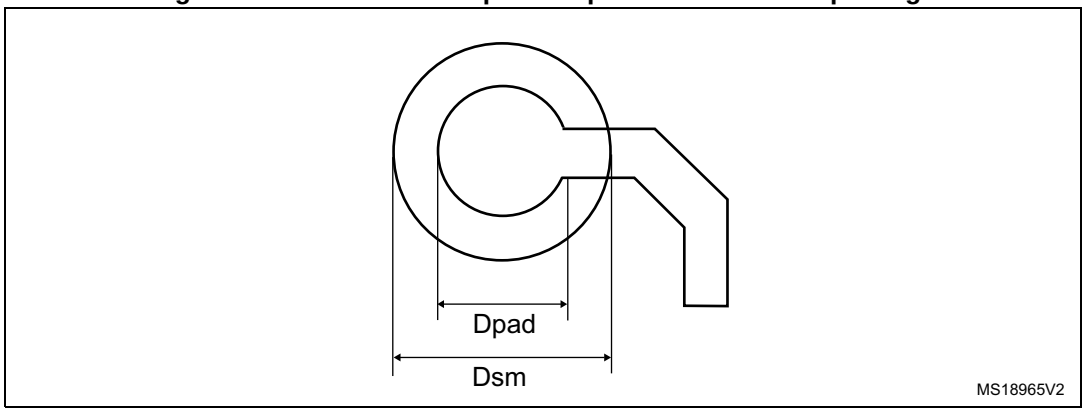


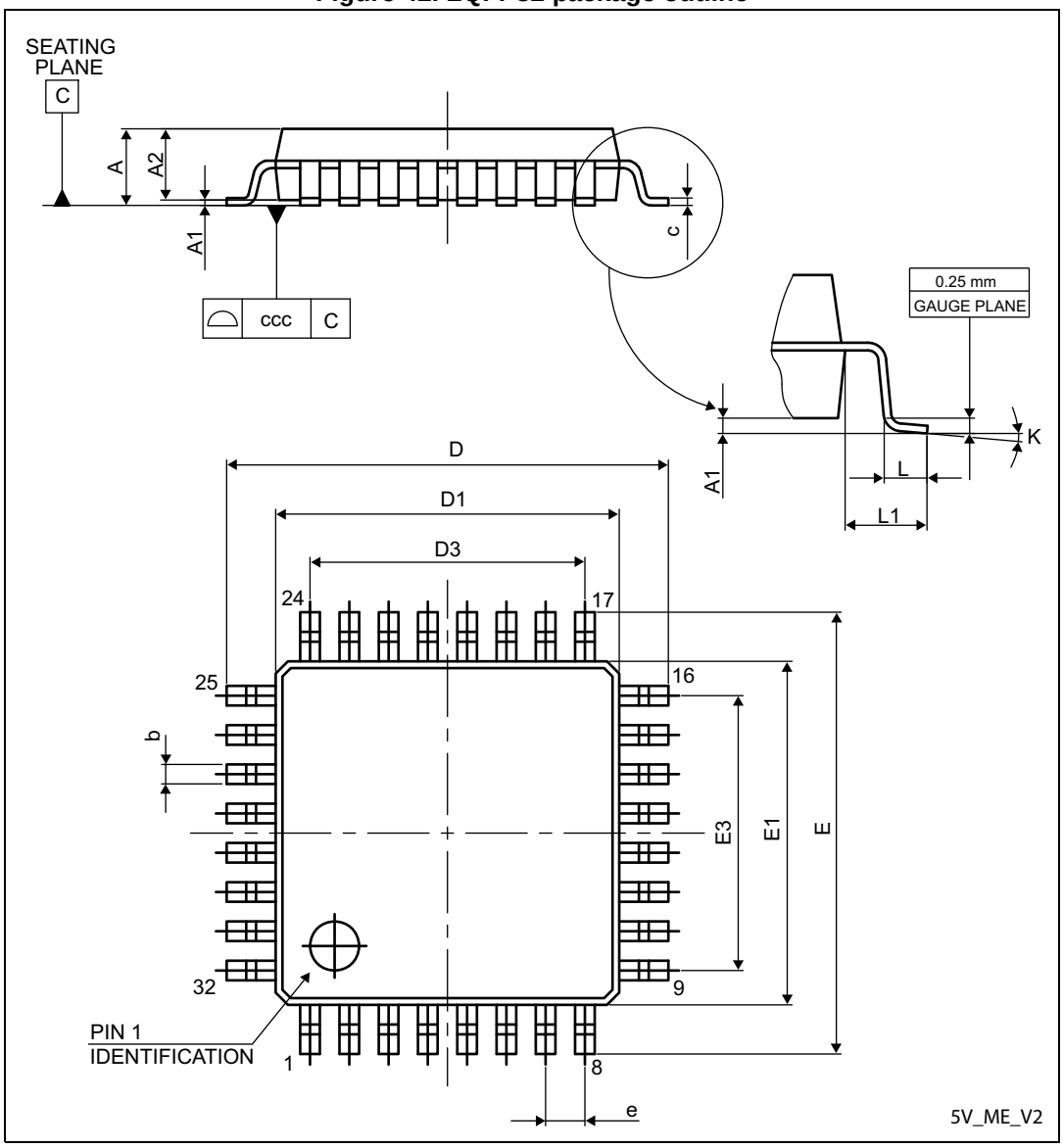
Table 69. WLCSP36 recommended PCB design rules

Dimension	Recommended values
Pitch	0.4 mm
Dpad	260 µm max. (circular) 220 µm recommended
Dsm	300 µm min. (for 260 µm diameter pad)
PCB pad design	Non-solder mask defined via underbump allowed

7.4 LQFP32 package information

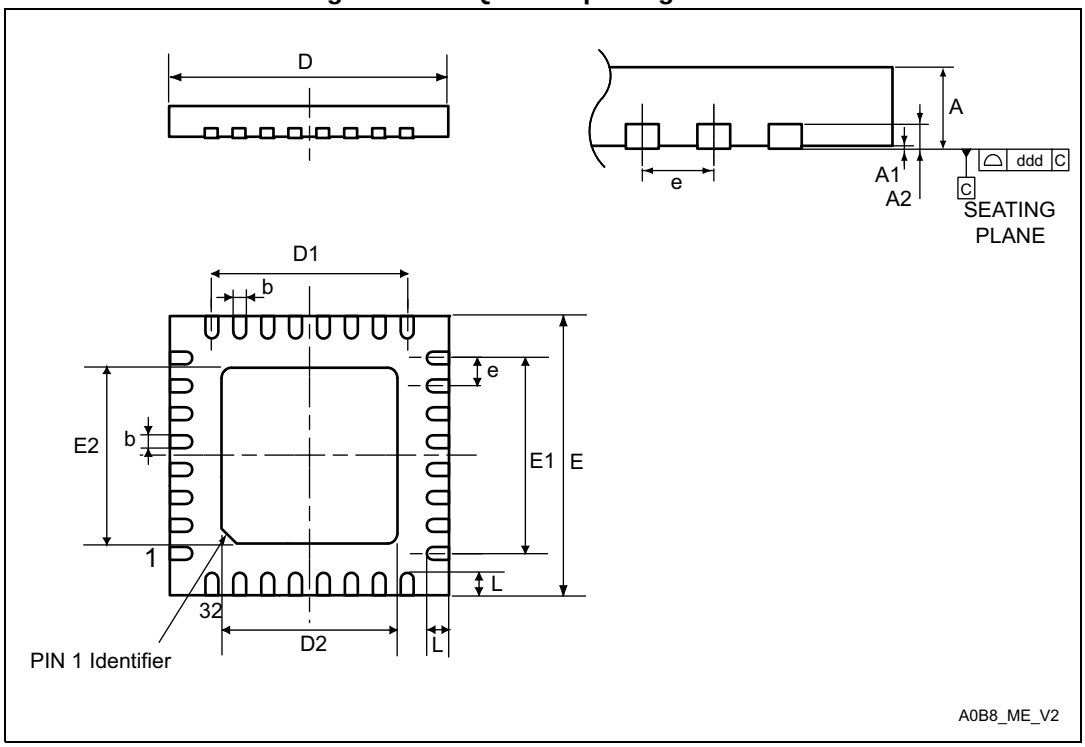
LQFP32 is a 32-pin, 7 x 7 mm low-profile quad flat package.

Figure 42. LQFP32 package outline



1. Drawing is not to scale.

Figure 45. UFQFPN32 package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. This pad is used for the device ground and must be connected. It is referred to as pin 0 in *Table: Pin definitions*.

9 Revision history

Table 76. Document revision history

Date	Revision	Changes
25-Feb-2014	1	Initial release.
03-Apr-2014	2	Added the sample engineering sections for all the packages in the chapter Package information: **Updated tables:** – STM32F042x4/x6 USART implementation: added one table footnote. – STM32F042x pin definitions, – Current characteristics, – Typical and maximum current consumption from VDD supply at VDD = 3.6 V, – Typical and maximum current consumption from the VDDA supply, – Typical and maximum consumption in Stop and Standby modes, – Typical and maximum current consumption from the VBAT supply, – Typical current consumption, code executing from Flash, running from HSE 8 MHz crystal, – Flash memory characteristics, – I/O static characteristics, – I/O current injection susceptibility, – EMS characteristics, – EMI characteristics, **Updated figures:** – UFQFPN32 32-pin package pinout, – UQFPN28 28-pin package, – Power supply scheme, – TC and TTa I/O input characteristics, – Five volt tolerant (FT and FTf) I/O input characteristics. – LQFP48 marking example (package top view), – UFQFPN48 marking example (package top view), – WLCSP36 marking example (package top view), – LQFP32 marking example (package top view), – UFQFPN28 marking example (package top view), – UFQFPN32 marking example (package top view), – TSSOP20 marking example (package top view)
26-Oct-2015	3	**Cover page:** number of I/Os and timers updated. **Updates in *Section 2: Description*:** – updated *Figure 1: Block diagram* **Updates in *Section 3: Functional overview:*** – updated *Figure 2: Clock tree* – addition of the number of complementary outputs for the advanced control timer and for TIM16, TIM17 general purpose timers in *Table 7: Timer feature comparison* – removal of USART2 from *Figure 3.5.4: Low-power modes*